

SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

S.R.M NAGAR, KATTANKULATHUR - 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LABORATORY MANUAL



ACADEMIC YEAR: 2026 - 2027 Odd Semester

EC3367 - ELECTRONICS CIRCUITS DESIGN LABORATORY

Year: II

Semester: III

Prepared by

Dr. S. Senthilmurugan, Assistant Professor (Sel.G)/ECE

Dr. A. Pandian, Assistant Professor (Sr.G)/ECE

Mr. S. Mari Rajan, Assistant Professor (Sr.G)/ECE



SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203.



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION OF THE INSTITUTE

Educate to excel in social transformation

MISSION OF THE INSTITUTE

- ❖ To contribute to the development of human resources in the form of professional engineers and managers of international excellence and competence with high motivation and dynamism, who besides serving as ideal citizen of our country will contribute substantially to the economic development and advancement in their chosen areas of specialization.
- ❖ To build the institution with international repute in education in several areas at several levels with specific emphasis to promote higher education and research through strong institute-industry interaction and consultancy.

VISION OF THE DEPARTMENT

To excel in the field of electronics and communication engineering and to develop highly competent technocrats with global intellectual qualities.

MISSION OF THE DEPARTMENT

M1: To train the students with the state-of-art technologies and to develop innovative solutions to cater to the societal needs.

M2: To orient the students towards global career with universal moral values and professional ethics.



SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203.



PROGRAM OUTCOMES

- 1. Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- 2. Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- 3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- 4. Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
- 6. The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- 8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PROGRAM SPECIFIC OUTCOME (PSOs)

PSO1: Ability to apply the acquired knowledge of basic skills, mathematical foundations, principles of electronics, modeling and design of electronics based systems in solving engineering problems.

PSO2: Ability to understand and analyze the interdisciplinary problems for developing innovative sustained solutions with environmental concerns.

OBJECTIVES:

The objectives of this laboratory course are to enable students:

- To examine the characteristics of a PN junction diode.
- To analyze the characteristics of a Zener diode.
- To investigate the operation of rectifier and filter circuits.
- To evaluate the performance of BJT and FET amplifiers through testing.
- To explore the working principles of power amplifiers.
- To design and implement simple analog electronic circuits.

LIST OF EXPERIMENTS

1. Characteristics of PN Junction Diode and Zener diode.
2. Full Wave Rectifier with Filters.
3. Design of Zener diode Regulator.
4. BJT Common Emitter input-output Characteristics.
5. FET Drain current and Transfer Characteristics.
6. Frequency response of CE and CS amplifiers.
7. Frequency response of CC and CD amplifiers
8. Frequency response of Cascade amplifier.
9. CMRR measurement of Differential amplifier.
10. Class A Power Amplifier.
11. Class C Power Amplifier.

TOPIC BEYOND SYLLABUS

12. Darlington amplifier.

COURSE OUTCOMES:

On completion of the course, the student will be able to

- Study the characteristics of a PN junction diode.
- Understand the operation of a Zener diode.
- Design and test a full-wave rectifier with filters.
- Evaluate the AC parameters of BJT and FET amplifiers.
- Understand the operation of power amplifiers.
- Develop simple analog application circuits.

COURSE OUTCOMES - PROGRAM OUTCOMES MATRIX

CO	PO											PSO	
	1	2	3	4	5	6	7	8	9	10	11	1	2
EC3367.1	3	3	2	3	2	1	-	-	3	-	-	2	1
EC3367.2	3	3	2	3	2	1	-	-	3	-	-	2	1
EC3367.3	3	2	2	3	1	1	-	2	3	-	-	3	2
EC3367.4	3	3	2	3	3	2	2	2	3	-	-	3	2
EC3367.5	3	2	2	3	2	2	2	2	3	-	-	3	2
EC3367.6	3	2	3	3	3	2	2	2	3	3	2	3	3
AVG	3	3	2	3	2	2	2	2	3	3	2	3	2

LAB Requirements for a Batch of 30 students

1. CRO/DSO (30 MHz) – 15 Nos.
2. Signal Generators / Function Generators (3 MHz) – 15 Nos.
3. Dual Generator Power Supplies (0-30 V) – 15 Nos.
4. Bread Board – 15 Nos.
5. SPICE simulator.

LIST OF EXPERIMENTS

CYCLE I

1. Characteristics of PN Junction Diode and Zener diode.
2. Full Wave Rectifier with Filters.
3. Design of Zener diode Regulator.
4. BJT Common Emitter input-output Characteristics.
5. FET Drain current and Transfer Characteristics.

CYCLE II

6. Frequency response of CE and CS amplifiers.
7. Frequency response of CC and CD amplifiers.
8. Frequency response of Cascade amplifier.
9. CMRR measurement of Differential amplifier.
10. Class A Power amplifier.
11. Class C Power amplifier.

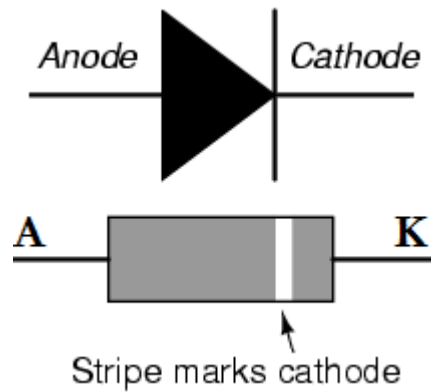
TOPIC BEYOND SYLLABUS

12. Darlington amplifier.

INDEX

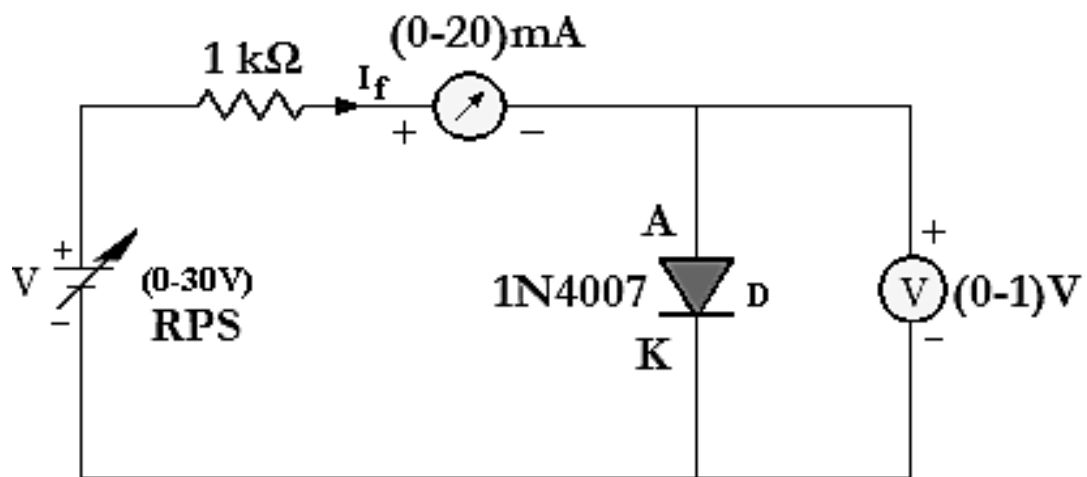
S.No.	Name of the Experiments		
1.	Characteristics of PN Junction Diode and Zener diode.		
2.	Full Wave Rectifier with Filters.		
3.	Design of Zener diode Regulator.		
4.	BJT Common Emitter input-output Characteristics.		
5.	FET Drain current and Transfer Characteristics.		
6.	Frequency response of CE and CS amplifiers.		
7.	Frequency response of CC and CD amplifiers.		
8.	Frequency response of Cascade amplifier.		
9.	CMRR measurement of Differential amplifier.		
10.	Class A Power amplifier.		
11.	Class C Power amplifier.		
12.	<u>Topic beyond Syllabus</u> Darlington amplifier.		

SYMBOL & PIN DIAGRAM:

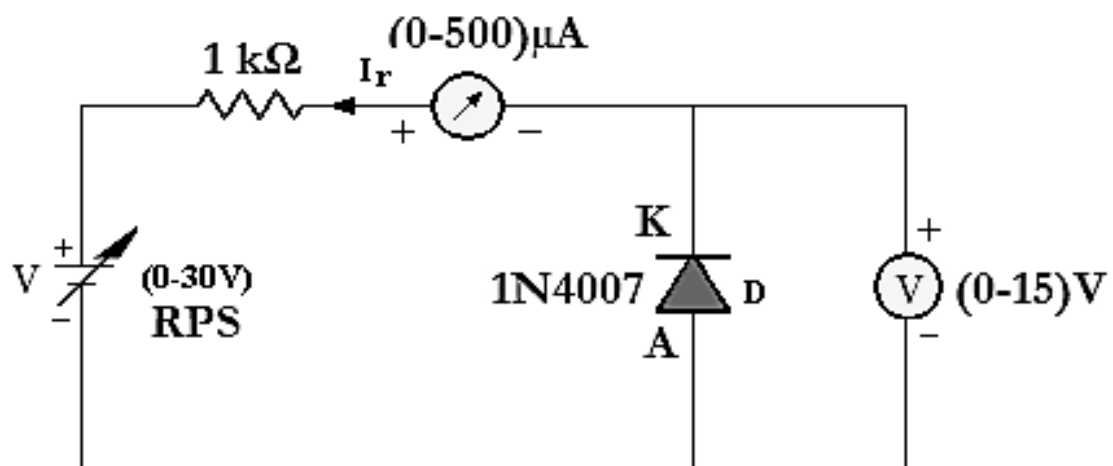


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Ex. No.: 1(a) CHARACTERISTICS OF PN JUNCTION DIODE

AIM:

To Plot the Volt Ampere Characteristics of PN Junction Diode under Forward and Reverse Bias Conditions, and to find the Cut-in voltage, Static Resistance, Dynamic Resistance under Forward and Reverse Bias.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Diode-PN	1N4007	1
2	Resistor	1k Ω	1
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-1)V, (0-15)V	Each One
5	Ammeters	MC (0-500) μ A, (0-20) mA	Each One
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannot cross the junction and the diode does not conduct. But there will be a leakage current due to minority carrier. When diode is forward biased, resistance offered is zero, and when reverse biased resistance offered is infinity. It acts as a perfect switch.

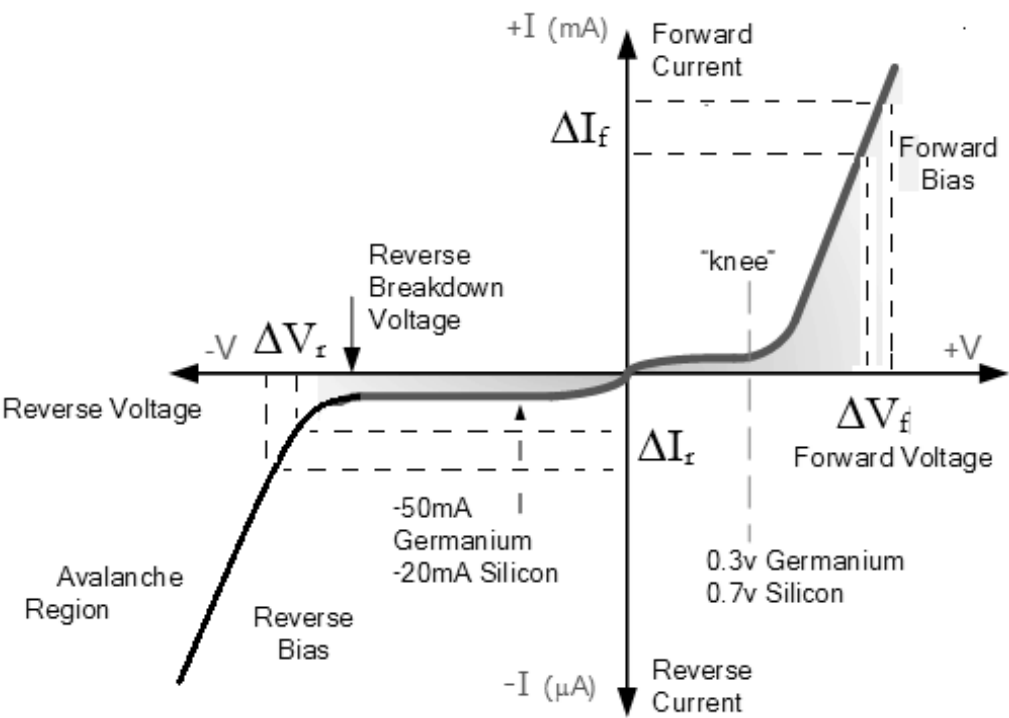
TABULATION:
FORWARD BIAS:

$V_f(\text{volts})$	$I_f(\text{mA})$

REVERSE BIAS:

$V_r(\text{volts})$	$I_r(\text{mA})$

MODEL GRAPH:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f .

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r .

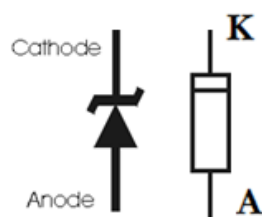
REVIEW QUESTIONS:

1. How a PN junction is formed?
2. In what way the width of depletion region can be varied?
3. What is potential barrier?
4. In forward bias condition the current condition is due to_____
5. What is reverse saturation current I_{co} ?
6. How diodes act as switch?
7. What is Dynamic Resistance?
8. Why it is called as Diode?
9. What are the majority carriers of P-type and N-type semiconductor?
10. What is an ideal diode? How does it differ from a real diode?

RESULT:

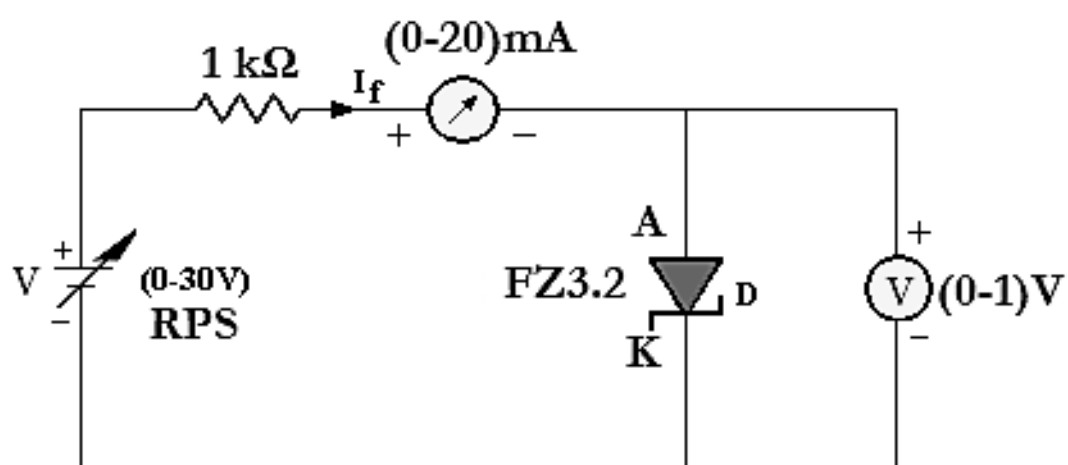
Thus the characteristics of PN diode were drawn and the necessary parameters are calculated from the graph.

SYMBOL & PIN DIAGRAM:

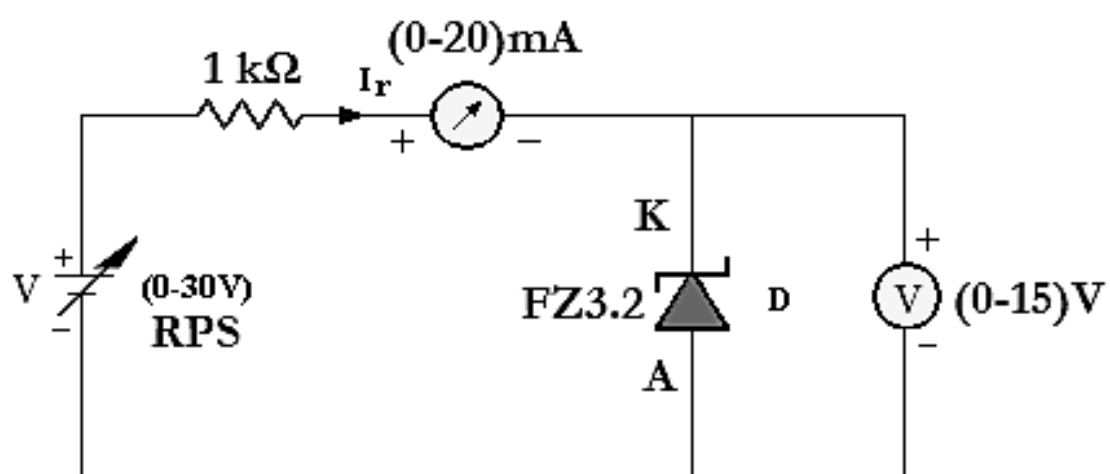


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



Ex. No.: 1 (b) CHARACTERISTICS OF ZENER DIODE

AIM:

To Obtain the Forward Bias and Reverse Bias characteristics of a Zener diode, and to find the Zener Break down Voltage from the Characteristics.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Diode-Zener	FZ3.2	1
2	Resistor	1k Ω	1
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-1)V, (0-10)V	Each One
5	Ammeters	MC (0-20)mA	1
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

TABULATION:

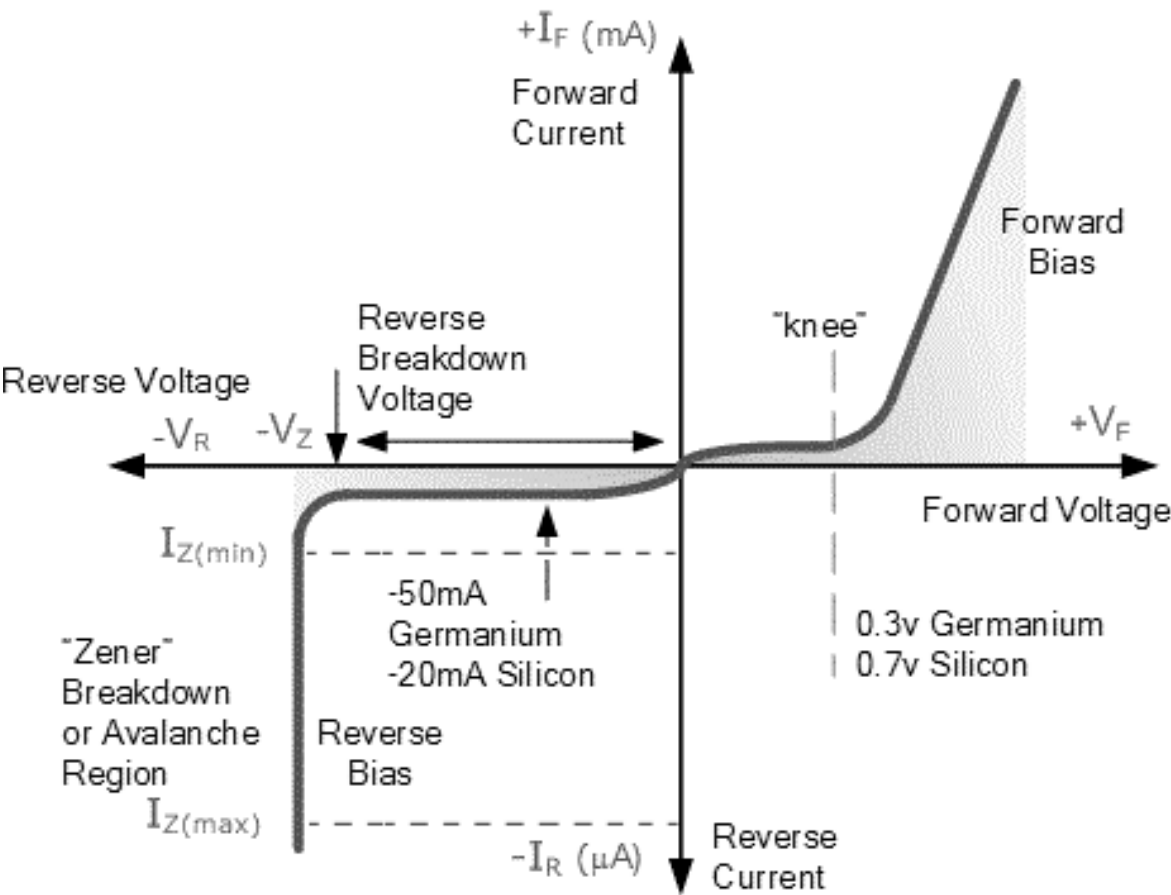
FORWARD BIAS:

$V_f(\text{volts})$	$I_f(\text{mA})$

REVERSE BIAS:

$V_r(\text{volts})$	$I_r(\text{mA})$

MODEL GRAPH:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f .

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r .

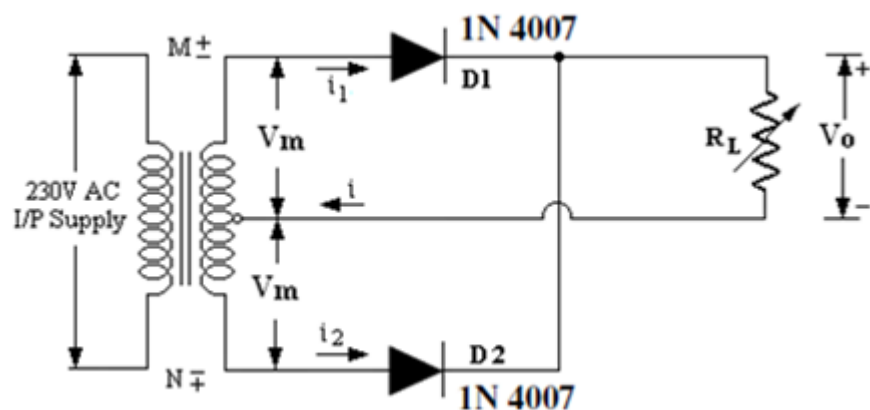
REVIEW QUESTIONS:

1. How Zener diode acts as a voltage regulator?
2. Explain working of a Zener Diode.
3. What is the cut-in voltage of Zener diode?
4. Differentiate between Zener Breakdown and Avalanche breakdown.
5. Why Zener diode is often preferred than PN diode?
6. List the application of Zener diode.
7. Define Zener breakdown voltage.
8. List the other Zener diode with different breakdown voltages.
9. Can we use Zener diode as a switch?
10. What will happen if PN regions are heavily doped in Zener diode?

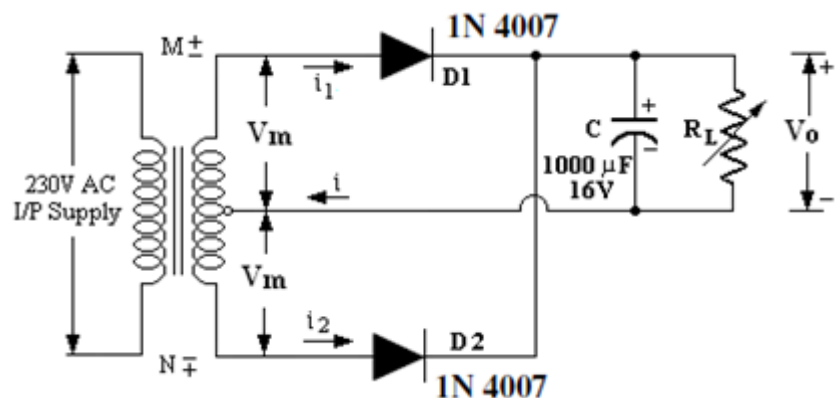
RESULT:

Thus the characteristics of Zener diode were drawn and the necessary parameters are determined from the graph.

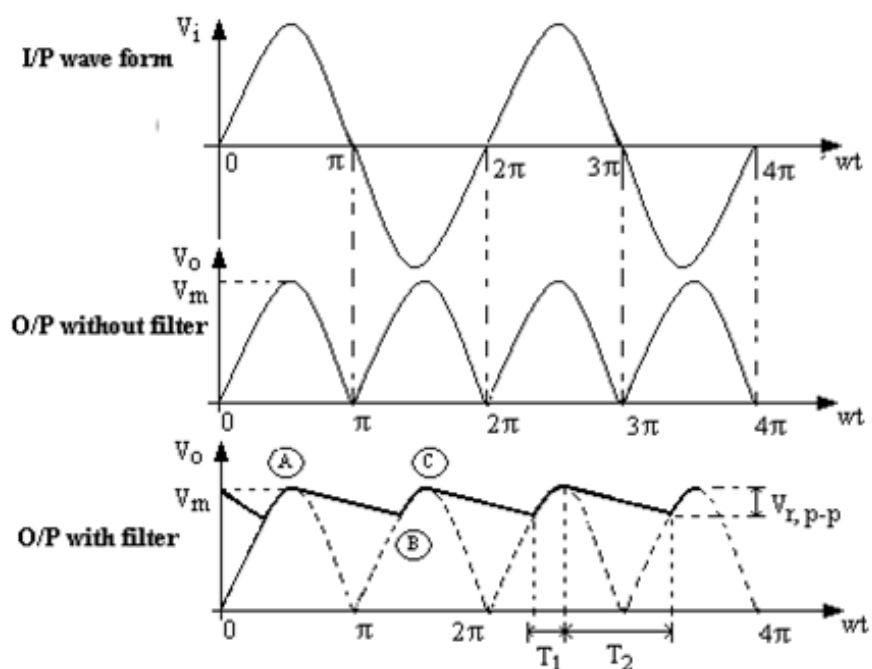
CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITHOUT FILTER:



CIRCUIT DIAGRAM FOR FULL WAVE RECTIFIER WITH FILTER:



FULL-WAVE RECTIFIER WAVEFORMS WITHOUT AND WITH FILTER:



Ex. No.: 2 FULL WAVE RECTIFIER WITH FILTERS

AIM:

To rectify the AC signal and then to find out Ripple factor and percentage of Regulation in Full wave center tapped rectifier with and without Capacitor filter.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Transformer	230V/(12-0-12) V	1
2	Diode	1N4007	2
3	Capacitors	1000 μ F,16V/ 470 μ F,25V	1
4	Decade Resistance Box/ Resistor	/ 10k Ω	1
5	Dual Trace CRO	20MHz	1
6	Multimeter	-	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY

Full wave rectifier utilizes both the cycle of input AC voltage. Two or four diodes are used in full wave rectifier. If full wave rectifier is designed using four diodes it is known as full wave bridge rectifier. Full wave rectifier using two diodes without capacitor is shown in the figure. Center tapped transformer is used in this full wave rectifier. During the positive cycle diode D1 conducts and it is available at the output. During negative cycle diode D1 remains OFF but diode D2 is in forward bias hence it conducts and negative cycle is available as a positive cycle at the output. Note that direction of current in the load resistance is same during both the cycles hence output is only positive cycles.

Advantages of full wave rectifier over half wave rectifier:

- ✓ The rectification efficiency is double than half wave rectifier
- ✓ Ripple factor is less and ripple frequency is double hence easy to filter out.
- ✓ DC output voltage and current is higher hence output power is higher.
- ✓ Better transformer utilization factor
- ✓ There is no DC saturation of core in transformer because the DC currents in two halves of secondary flow in opposite directions.

Disadvantages:

- ✓ Requires center tap transformer
- ✓ Requires two diodes compared to one diode in half wave rectifier.

TABULATION WITHOUT FILTER:

V no load Voltage (Vdc) = V

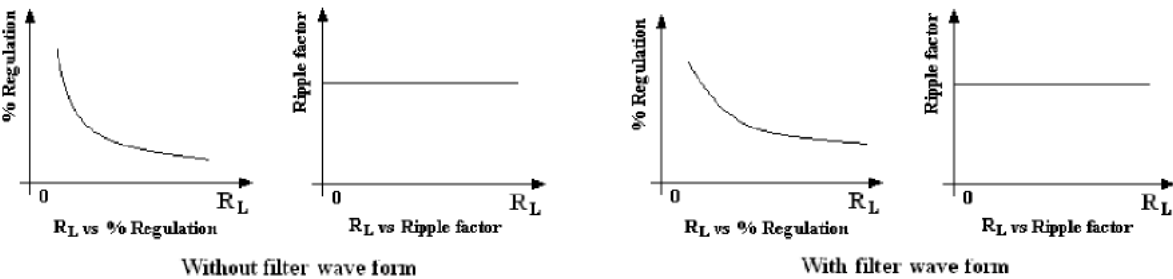
Load Resistance $R_L (\Omega)$	O/P Voltage (Vo)		Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{NL}} * 100\%\right)$
	$V_{ac} (V)$	$V_{dc} (V)$		

TABULATION WITH FILTER:

V no load Voltage (Vdc) = V

Load Resistance $R_L (\Omega)$	O/P Voltage (Vo)		Ripple factor $\left(\gamma = \frac{V_{ac}}{V_{dc}}\right)$	% of Regulation $\left(\frac{V_{NL} - V_{FL}}{V_{NL}} * 100\%\right)$
	$V_{ac} (V)$	$V_{dc} (V)$		

MODEL GRAPH



PROCEDURE:**WITHOUT FILTER:**

1. Connecting the circuit on bread board as per the circuit diagram.
2. Connect the primary of the transformer to main supply i.e. 230V, 50Hz
3. Connect the decade resistance box and set the RL value to 100Ω
4. Connect the Multimeter at output terminals and vary the load resistance (DRB)
5. from 100Ω to 1KΩ and note down the Vac and Vdc as per given tabular form
6. Disconnect load resistance (DRB) and note down no load voltage Vdc (V no load)
7. Connect load resistance at 1kΩ and connect Channel – II of CRO at output terminals and CH – I of CRO at Secondary Input terminals observe and note down the Input and Output Wave form on Graph Sheet.
8. Calculate ripple factor $\gamma = \frac{V_{ac}}{V_{dc}}$
9. Calculate Percentage of Regulation, $\% \eta = \frac{V_{no\ load} - V_{full\ load}}{V_{no\ load}} \times 100\%$

WITH CAPACITOR FILTER:

1. Connecting the circuit as per the circuit Diagram and repeat the above procedure from steps 2 to 8.

CALCULATIONS:

Without Filter:

R_F = Forward resistance of diode = 30Ω

R_L = Load resistance

$$V_{dc} = \frac{V_m R_L}{\pi(R_F + R_L)}$$

$$V_{rms} = \frac{V_m R_L}{2(R_F + R_L)}$$

$$\text{Ripple factor} = r = \frac{(V_{rms}^2 - V_{dc}^2)^{1/2}}{V_{dc}}$$

Average load voltage at no load (V_{NL}) = V_m / π

Average load voltage at full load = $V_{FL} = \frac{V_m R_L}{2(R_F + R_L)}$

With Filter:

$f = 50\text{Hz}$

$$V_{dc} = \frac{V_m R_L}{\frac{1}{4fC} + R_L}$$

$$V_{rms} = \left(\frac{1}{2\sqrt{3}fC}\right)\left(\frac{V_m}{\frac{1}{4fC} + R_L}\right)$$

Ripple factor = $r = V_{rms} / V_{dc}$ (or) $\gamma = \frac{V_{ac}}{V_{dc}}$

Calculate Percentage of Regulation, $\% \eta = \frac{V_{no\ load} - V_{full\ load}}{V_{no\ load}} \times 100\%$

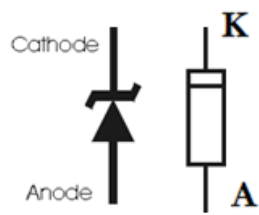
REVIEW QUESTIONS:

1. What is a full wave rectifier?
2. Compare capacitor filter with an inductor filter?
3. What is meant by regulation? Why regulation is poor in the case of inductor filter?
4. What is meant by time constant?
5. What is the frequency of AC component at the output of full wave rectifier? Give reason.
6. What is the difference in DC output voltage in half wave and full wave rectifier for the same AC input?
7. What is the PIV necessary for the diode if transformer of 24-0-24 V is used?
8. What is the mathematical relationship between rms input AC voltage and DC output voltage in half wave rectifier with and without filter capacitor?
9. Compare the efficiency of full wave Bridge Rectifier with Half wave Rectifier.
10. Measure the DC component in the output by varying the C value in the Filter.

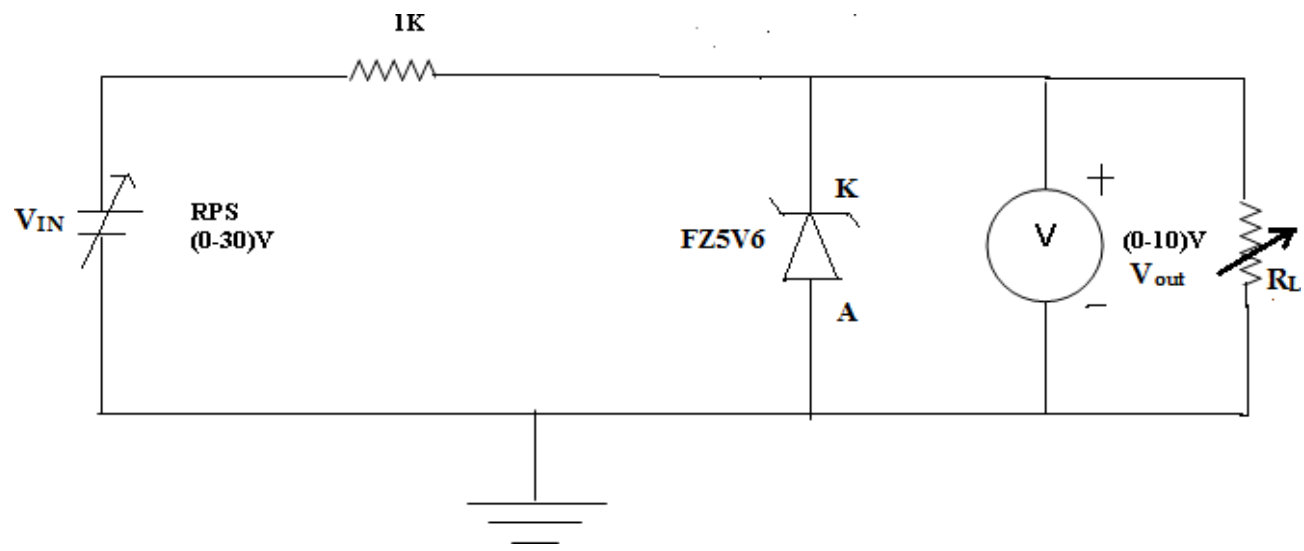
RESULT:

Thus the Full wave rectifier is designed with and without capacitor filter and the corresponding dc output voltages and the ripple factors are measured and verified with the theoretical values.

SYMBOL & PIN DIAGRAM:

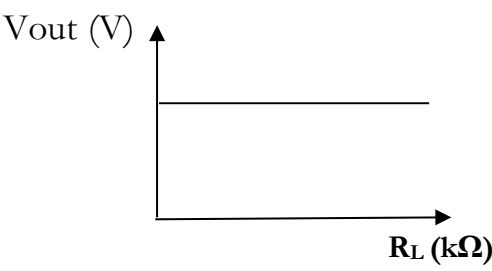


CIRCUIT DIAGRAM:

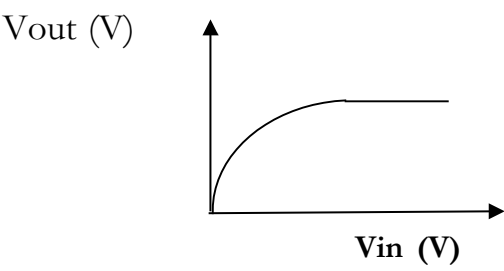


MODEL GRAPH:

LOAD REGULATION



LINE REGULATION



TABULATION:

LOAD REGULATION:

R_L (K Ω)	V_{out} (V)

LINE REGULATION:

V_{in} (V)	V_{out} (V)

Ex. No.: 3 DESIGN OF ZENER DIODE REGULATOR

AIM:

To design a voltage regulator using Zener diode.

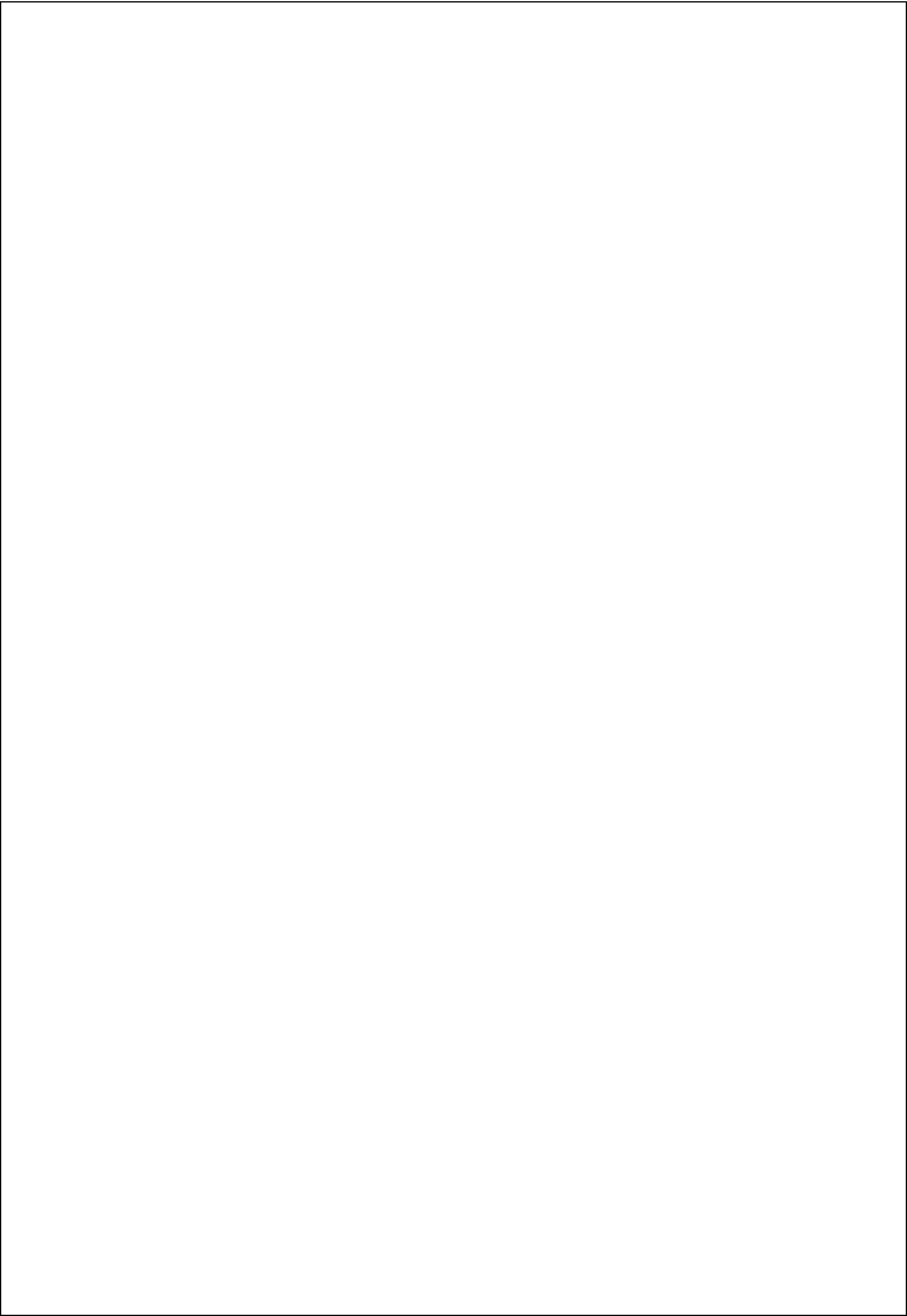
APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1.	Zener diode	FZ 3V2 / FZ 5V6	1
2.	Resistor	1K Ω	1
3.	Ammeter	(0-30) mA	1
4.	Voltmeter	(0-10)V, (0-1)V	Each One
5.	Regulated power supply	(0-30)V	1
6.	Bread Board		1
7.	Connecting wires		Few

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts. In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode.

For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.



PROCEDURE:

1. The connections are made as per the circuit diagram.
2. Keep Load resistance R_L constant.
3. Vary the Input voltage and note down the corresponding output voltage.
4. Now keep voltage constant vary the R_L and note down the voltmeter corresponding reading.
5. Plot the respective regulations graph.

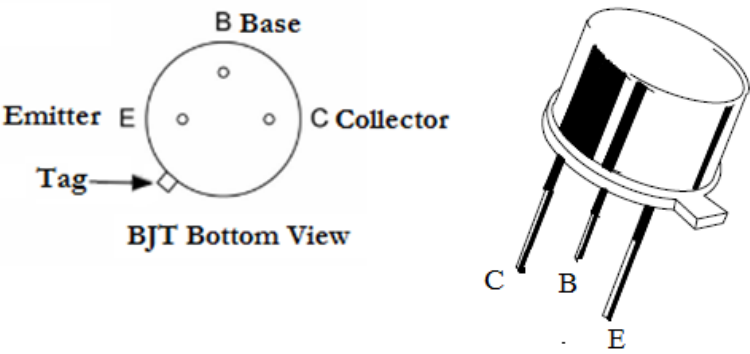
REVIEW QUESTIONS:

1. How does a Zener diode function as a voltage regulator?
2. Explain the working principle of a Zener diode.
3. What is meant by Zener breakdown?
4. What is avalanche breakdown?
5. Differentiate between Zener breakdown and avalanche breakdown.
6. What are the practical applications of a Zener diode?
7. What is a voltage regulator?
8. What is the cut-in voltage of a diode?
9. What is meant by the breakdown voltage of a diode?
10. Draw and explain the forward and reverse bias characteristics of a Zener diode.

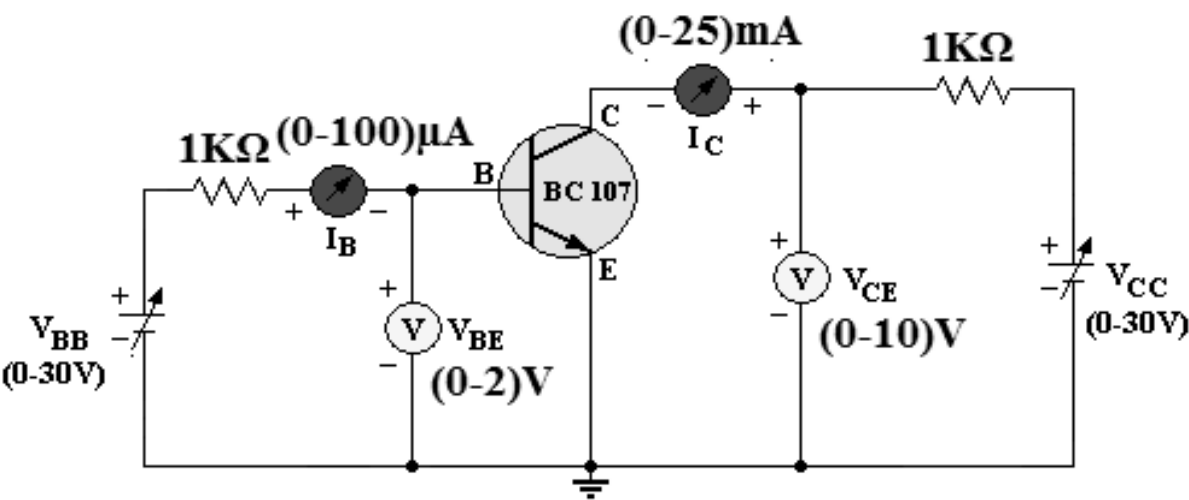
RESULT:

Thus the voltage regulator was designed using Zener diode and the load regulation, line regulation was determined.

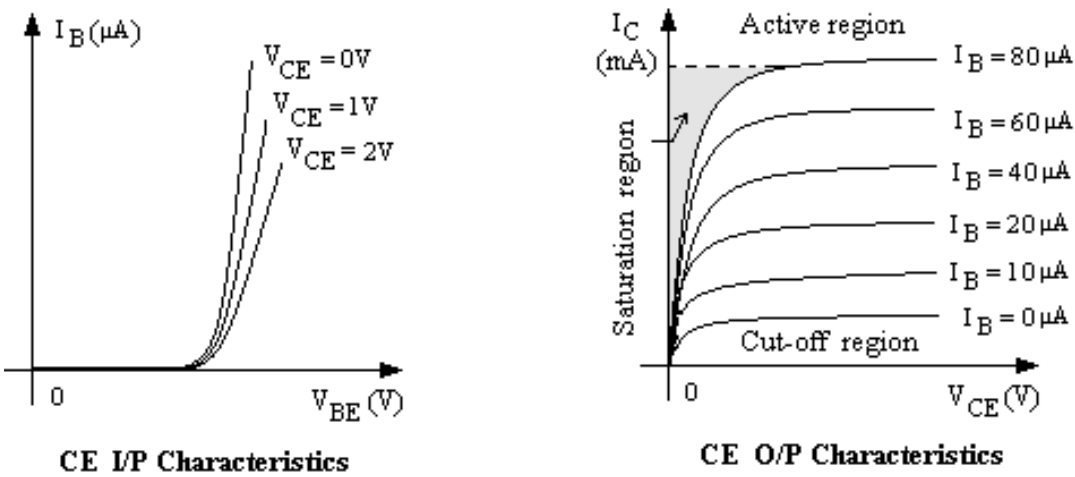
PIN DIAGRAM OF BC107:



CIRCUIT DIAGRAM: COMMON EMITTER CIRCUIT CHARACTERISTICS:



MODEL GRAPH:



Ex. No.: 4 BJT COMMON EMITTER INPUT – OUTPUT CHARACTERISTICS

AIM:

To plot the Input and Output characteristics of a transistor connected in Common Emitter Configuration and to find the dynamic resistance and amplification factor.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Transistor	BC107-Max Rating : 50V 1A, 3W	1
2	Resistors	1k Ω , (or) 470 Ω	2
3	Dual Regulated Power Supply	(0-30)V	1
4	Voltmeters	MC (0-2)V, (0-10)V	Each One
5	Ammeters	MC (0-25)mA, (0-100) μ A	Each One
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

A Bipolar Junction Transistor or BJT is a three terminal device having two PN-junctions connected together in series. Each terminal is given a name to identify it and these are known as the Emitter (E), Base (B) and Collector (C). There are two basic types of bipolar transistor construction, NPN and PNP, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made. Bipolar Transistors are "CURRENT" Amplifying or current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing current applied to their base terminal. The principle of operation of the two transistors types NPN and PNP, is exactly the same the only difference being in the biasing (base current) and the polarity of the power supply for each type. In CE configuration, Emitter is common to both the input and output as shown in figure. The direction of the arrow in the symbol shows current flow between the base and emitter terminal, pointing from the positive P-type region to the negative N-type region, exactly the same as for the standard diode symbol. For normal operation, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased.

TABULATION:

INPUT CHARACTERISTICS:

$V_{CE} = 1V$		$V_{CE} = 2V$	
$V_{BE}(V)$	$I_B (mA)$	$V_{BE}(V)$	$I_B (mA)$

OUTPUT CHARACTERISTICS:

$I_B = \quad \mu A$		$I_B = \quad \mu A$	
$V_{CE} (V)$	$I_C (mA)$	$V_{CE} (V)$	$I_C (mA)$

DESCRIPTION:

Input Characteristics: The variation of the base current I_B with the base-emitter voltage V_{BE} keeping the collector-emitter voltage V_{CE} fixed, gives the input characteristic in C_E mode.

Input Dynamic Resistance (r_i): This is defined as the ratio of change in base emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). This is dynamic and it can be seen from the input characteristic, its value varies with the operating current in the transistor:

$$r_i = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE}}$$

The value of r_i can be anything from a few hundreds to a few thousand ohms.

Output Characteristics: The variation of the collector current I_C with the collector-emitter voltage V_{CE} is called the output characteristic. The plot of I_C versus V_{CE} for different fixed values of I_B gives one output characteristic. Since the collector current changes with the base current, there will be different output characteristics corresponding to different values of I_B .

Output Dynamic Resistance (r_o): This is defined as the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at a constant base current I_B .

$$r_o = \left. \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B}$$

The high magnitude of the output resistance (of the order of 100 kW) is due to the reverse biased state of this diode.

Transfer Characteristics: The transfer characteristics are plotted between the input and output currents (I_B versus I_C). Both I_B and I_C increase proportionately.

Current amplification factor (β)

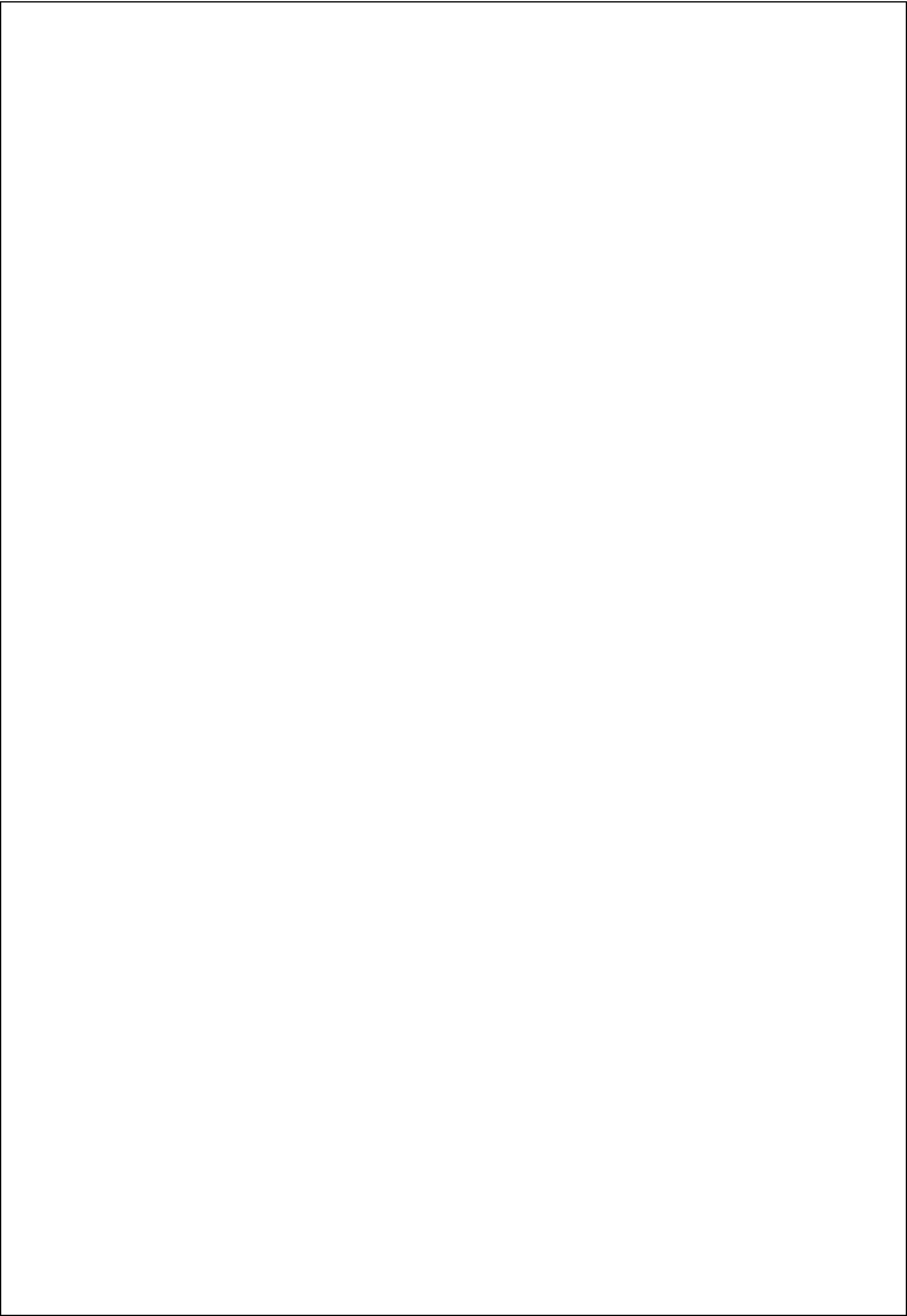
This is defined as the ratio of the change in collector current to the change in base current at a constant collector-emitter voltage (V_{CE}) when the transistor is in active state.

$$\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE}}$$

This is also known as small signal current gain and its value is very large. The ratio of I_C and I_B we get what is called dc of the transistor. Hence,

$$\beta_{dc} = \left. \frac{I_C}{I_B} \right|_{V_{CE}}$$

Since I_C increases with I_B almost linearly, the values of both dc and ac are nearly equal.



PROCEDURE:**TO FIND THE INPUT CHARACTERISTICS:**

1. Connect the circuit as in the circuit diagram.
2. Keep V_{BB} and V_{CC} in zero volts before giving the supply
3. Set $V_{CE} = 1$ volt by varying V_{CC} and vary the V_{BB} smoothly with fine control such that base current I_B varies in steps of $5\mu A$ from zero up to $100\mu A$, and note down the corresponding voltage V_{BE} for each step in the tabular form.
4. Repeat the experiment for $V_{CE} = 1$ volt and 2 volts.
5. Draw a graph between V_{BE} vs. I_B against $V_{CE} = \text{Constant}$.

TO FIND THE OUTPUT CHARACTERISTICS:

1. Start V_{EE} and V_{CC} from zero Volts.
2. Set the $I_B = 20\mu A$ by using V_{BB} such that, V_{CE} changes in steps of 0.2 volts from zero up to 10 volts, note down the corresponding collector current I_C for each step in the tabular form.
3. Repeat the experiment for $I_E = 20\mu A$ and $I_E = 40\mu A$, tabulate the readings.
4. Draw a graph between V_{CE} Vs I_C against $I_B = \text{Constant}$.

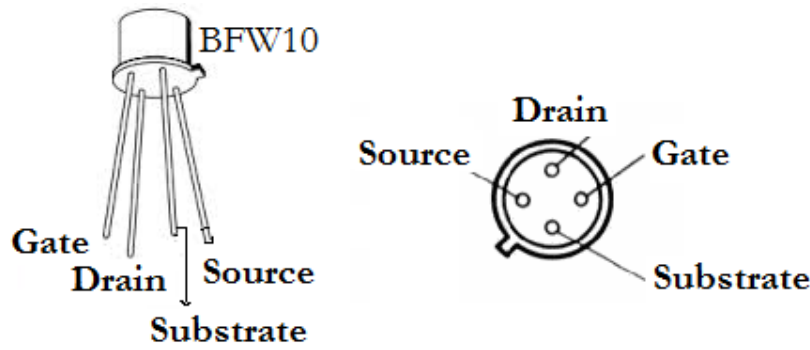
REVIEW QUESTIONS:

1. Why BJT is called current controlled device?
2. Why CE configuration is commonly used for amplifier circuits?
3. Why I_B vs. V_{BE} plots move outwards for higher values of V_{CE} in CE input characteristics?
4. What is indicated by B, C and 107 in BC107?
5. What are the regions of operation of a transistor?
6. Can transistor be replaced by two back to back connected diodes?
7. To operate a transistor as amplifier, emitter junction is forward biased and collector junction is reverse biased. Why?
8. What is the relation between α , β and γ and mention the range of β for BJT?
9. List the current components of BJT in CE configuration.
10. Why the doping of collector is less compared to emitter?
11. What is the difference between CE and emitter follower circuit?
12. What is the phase relation between input and output?
13. Draw diagram of CE configuration for PNP transistor?
14. What is the power gain of CE configuration?
15. What are the applications of CE configuration?

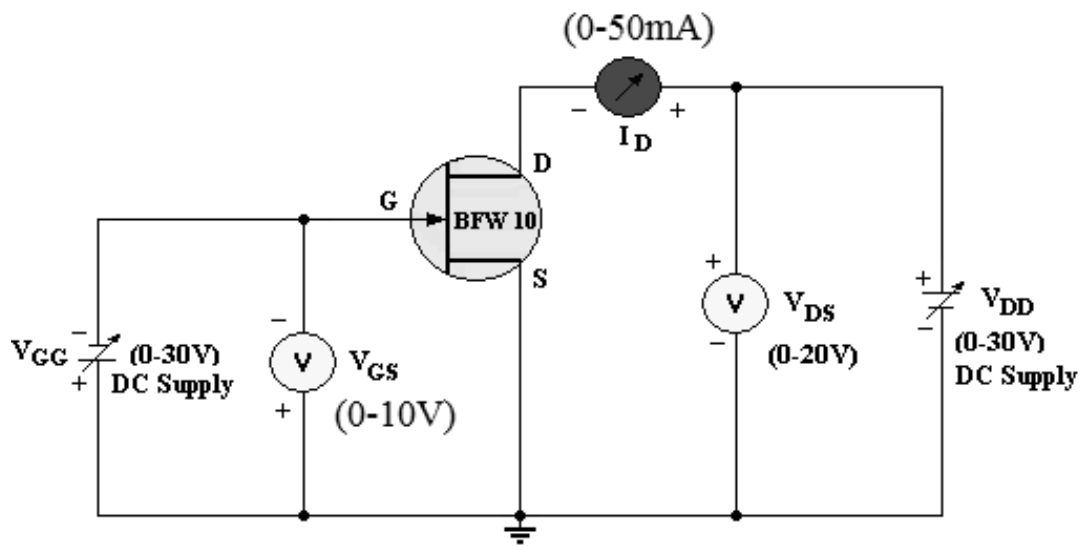
RESULT:

Thus the input and output characteristic of BJT in Common Emitter configuration were plotted and the dynamic resistance and amplification factor were obtained.

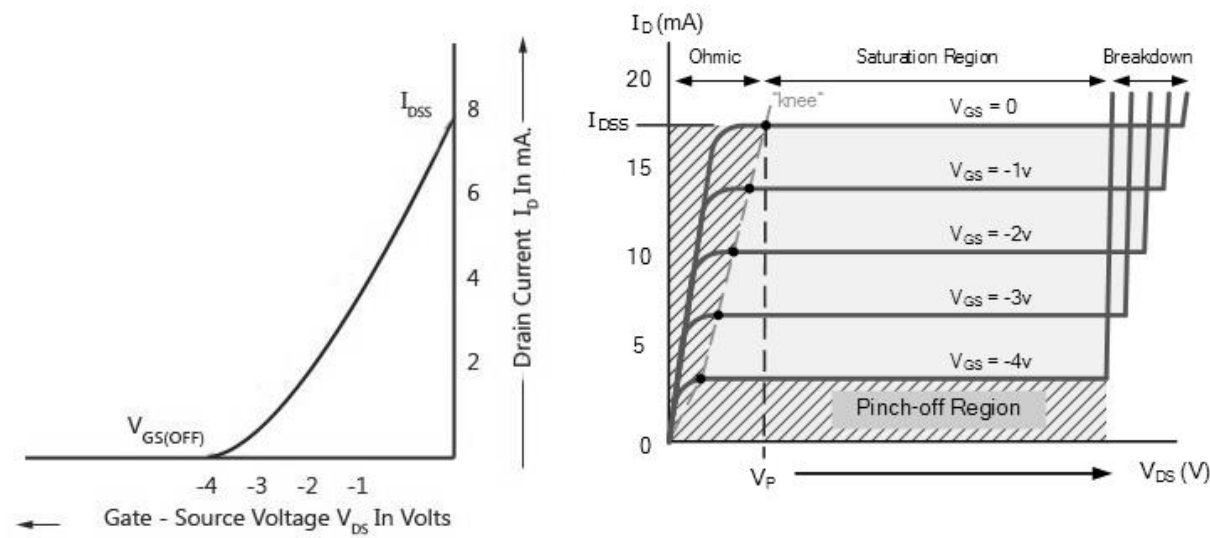
PIN DIAGRAM OF BFW10:



CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 5 FET DRAIN CURRENT AND TRANSFER CHARACTERISTICS

AIM:

To plot the Drain and Transfer characteristics of JFET and to find Drain resistance, Transconductance, Amplification factor, Drain saturation current I_{DSS} and Pinch off voltage.

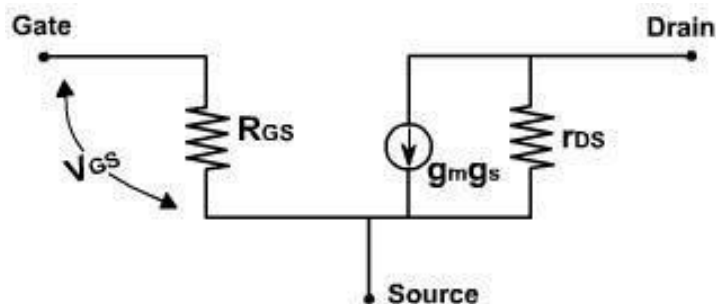
APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	FET	BFW10 or 11 $I_{DSS} > 8 \text{ mA}$, $V_p < 8 \text{ V}$	1
2	Dual Regulated Power Supply	(0-30)V	1
3	Voltmeters	MC (0-10)V, MC (0-20)V	Each One
4	Ammeters	MC (0-50) mA	1
5	Bread Board		1
6	Connecting Wires		Few

THEORY:

The Field Effect Transistor (FET) is a three terminal device. Three terminals are Drain (D), Source (S), Gate (G) and fourth terminal is substrate/body/shield/Bulk but it is not used. In FET, current flow is due to only one type of charge particles, either electrons or holes. So FET is known as unipolar device. The name “field effect” is derived from the fact that the current is controlled by an electric field set up in the device by an externally applied voltage. Thus FET is a voltage controlled device while bipolar transistor is current controlled device.

JFET AC Equivalent Circuit:



TABULATION:

Drain characteristics

$V_{GS} = 0V$		$V_{GS} = -2V$		$V_{GS} = -4V$	
$V_{DS} (V)$	$I_D(mA)$	$V_{DS} (V)$	$I_D(mA)$	$V_{DS} (V)$	$I_D(mA)$

Transfer characteristics

$V_{DS} = 2V$		$V_{DS} = 4V$		$V_{DS} = 6V$	
$V_{GS} (V)$	$I_D(mA)$	$V_{GS} (V)$	$I_D(mA)$	$V_{GS} (V)$	$I_D(mA)$

PROCEDURE:

DRAIN CHARACTERISTICS:

1. Connect the circuit as per the circuit diagram and start with VGG and VDD keeping at zero volts.
2. Keep VGG such that $V_{GS} = 0$ volts, Now vary VDD such that V_{DS} Varies in steps of 1 volt up to 10 volts. And Note down the corresponding Drain current I_D .
3. Repeat the above experiment with $V_{GS} = -2V$ and $-4V$ and tabulate the readings.
4. Draw a graph V_{DS} Vs I_D against V_{GS} as parameter on graph.
5. From the above graph calculate r_d and note down the corresponding diode current against the voltage in the tabular form.
6. Draw the graph between voltages across the Diode vs. Current through the diode in the first quadrant as shown in model graph.

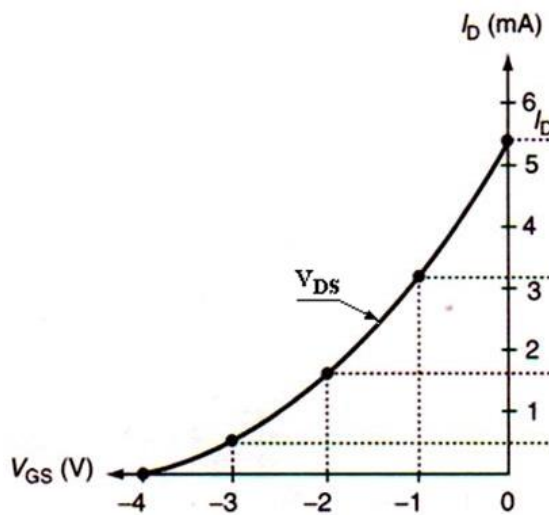
TRANSFER CHARACTERISTICS:

1. Set VGG and VDD at zero volts .keep $V_{DS} = 2V$ olt.
2. Vary VGG such that V_{GS} varies in steps of 0.5 volts. Note down the corresponding
3. Drain current I_D , until $I_D = 0mA$ and Tabulate the readings.
4. Repeat the above experiment for $V_{DS} = 4$ Volts and 6 Volts and tabulate the readings.
5. Draw graph between V_{GS} Vs I_D with V_{DS} as parameter.
6. From the graph find g_m .

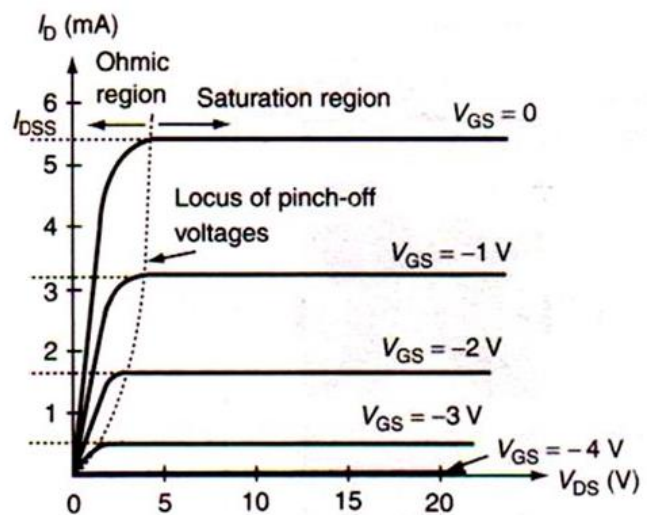
PRECAUTIONS:

1. Check the wires for continuity before use.
2. Keep the power supply at zero volts before starting the experiment.
3. All the contacts must be intact.
4. For a good JFET I_D will be ≥ 11.0 mA at $V_{GS} = 0.0$ volts if not change the JFET.
5. Make sure while selecting the source, drain and gate terminals of the FET.

MODEL GRAPH:



FET Transfer Characteristics



FET Drain Characteristics

CALCULATIONS:

Calculation of r_d :

Construct a Triangle on one of the output characteristic for a particular V_{GS} in the active region and find ΔV_{DS} and ΔI_D .

Drain resistance $r_d = \Delta V_{DS} / \Delta I_D$ ($V_{GS} = \text{constant}$)

Calculation of g_m :

Construct a Triangle on one of the Transfer characteristics for a particular V_{DS} find ΔV_{GS} and ΔI_D .

Transconductance $g_m = \Delta I_D / \Delta V_{GS}$ ($V_{DS} = \text{constant}$).

Calculation of μ :

Amplification factor $\mu = g_m \times r_d$.

REVIEW QUESTIONS:

1. Why it is called by name “Field Effect Transistor”?
2. What are the advantage of FET over BJT?
3. What are the disadvantages of FET?
4. What is the significance of arrowhead in FET symbol?
5. Why FET is called unipolar device?
6. Define VVR.
7. What are the applications of FET?
8. Why FET is called us voltage controlled device?
9. What are the characteristics of JFET?
10. Why input resistance in FET amplifier is more than the BJT amplifier?
11. What is pinch off voltage?
12. What is Enhancement mode and Depletion mode?
13. Draw the Equivalent circuit of JFET for low frequencies.
14. Write the mathematical equation for g_m in terms of g_{mo} .
15. Write equation of FET I_D in terms of V_{GS} and V_p .

RESULT:

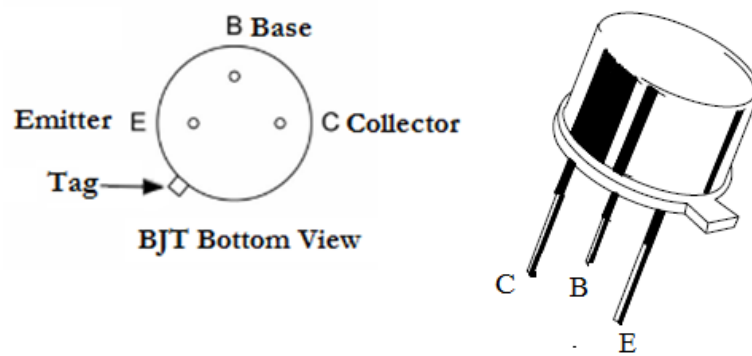
Thus the drain and transfer characteristics of JFET is drawn and following parameters are observed.

Drain resistance (r_d) =

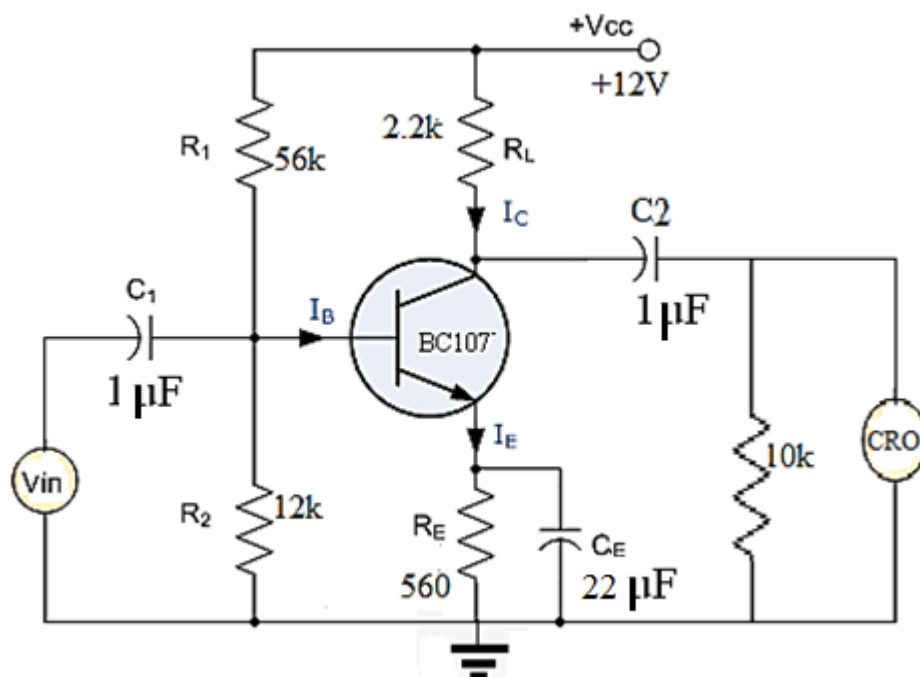
Trans conductance (g_m) =

Amplification factor (μ) =

PIN DIAGRAM:



CIRCUIT DIAGRAM FOR CE AMPLIFIER:



Ex. No.: 6 (a) FREQUENCY RESPONSE OF COMMON EMITTER AMPLIFIER**AIM:**

To design and construct BJT CE Amplifier using voltage divider bias and to obtain its frequency response.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Transistor BC107	Max Rating : 50V 1A, 3W	1
2	Resistors	56k Ω , 12k Ω , 2.2k Ω , 10k Ω , 560 Ω	Each One
3	Capacitor	0.1 μ F, 22 μ F	2,1
4	Dual Regulated Power Supply	(0-30)V	1
5	CRO	(0-30)MHz	1
6	Function Generator	(0 – 1)MHz	1
7	Bread Board		1
8	Connecting Wires		Few
9	BNC CRO Probe		2

THEORY:

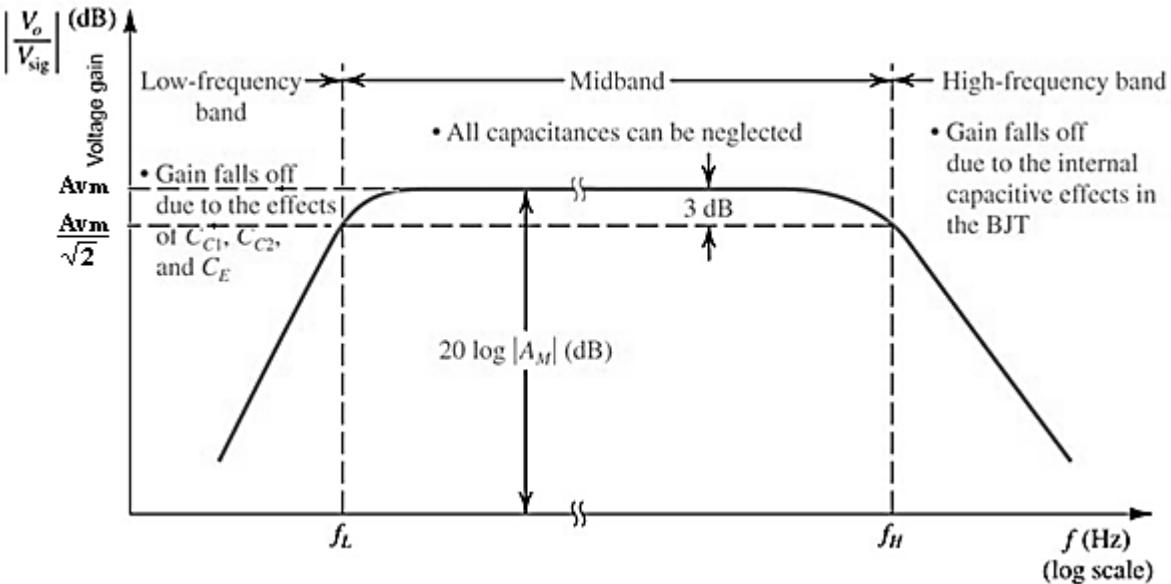
Common Emitter amplifier has the emitter terminal as the common terminal between input and output terminals. The emitter base junction is forward biased and collector base junction is reverse biased, so that transistor remains in active region throughout the operation. When a sinusoidal AC signal is applied at input terminals of circuit during positive half cycle the forward bias of base emitter junction V_{BE} is increased resulting in an increase in I_B , The collector current I_c is increased by β times the increase in I_B , V_{CE} is correspondingly decreased. i.e. output voltage gets decreased. Thus in a CE amplifier a positive going signal is converted into a negative going output signal i.e. 180° phase shift is introduced between output and input signal and it is an amplified version of input signal.

TABULATION:

$$V_i = 1V$$

S.No	Frequency (Hz)	V _o (V)	Gain= 20log(V _o /V _i)dB

MODEL GRAPH:



DESIGN:

$$V_{cc} = 12 \text{ V}, I_c = 2 \text{ mA}, R_B = 10 \text{ k}\Omega, h_{fe} = 100, h_{ie} = 2 \text{ k}\Omega$$

$$V_{ce} = V_{cc} / 2 = 12 / 2 = 6 \text{ V}$$

$$V_E = V_{cc} / 10 = 12 / 10 = 1.2 \text{ V}$$

$$I_E \approx I_c = 2 \text{ mA}$$

$$R_E = V_E / I_E = 1.2 \text{ V} / 2 \text{ mA} = 600 \Omega$$

$$\text{Choose, } R_E = 560 \Omega$$

$$V_{cc} = I_c R_c + V_{ce} + I_E R_E$$

$$R_c = (V_{cc} - V_{ce} - I_E R_E) / I_c$$

$$R_c = (12 - 6 - 1.2) / 2 \text{ mA}$$

$$R_c = 2.4 \text{ k}\Omega$$

$$\text{Choose, } R_c = 2.7 \text{ k}\Omega$$

$$V_{BE} = V_B - V_E$$

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7 + 1.2 = 1.9 \text{ V}$$

$$V_B = V_{cc} (R_2 / (R_1 + R_2)) = 1.9 \text{ V}$$

$$R_2 / (R_1 + R_2) = 1.9 \text{ V} / 12 \text{ V} = 0.158$$

$$R_B = 10 \text{ k} = R_1 R_2 / (R_1 + R_2) = R_1 (0.158)$$

$$R_1 = 63.157 \text{ k}\Omega$$

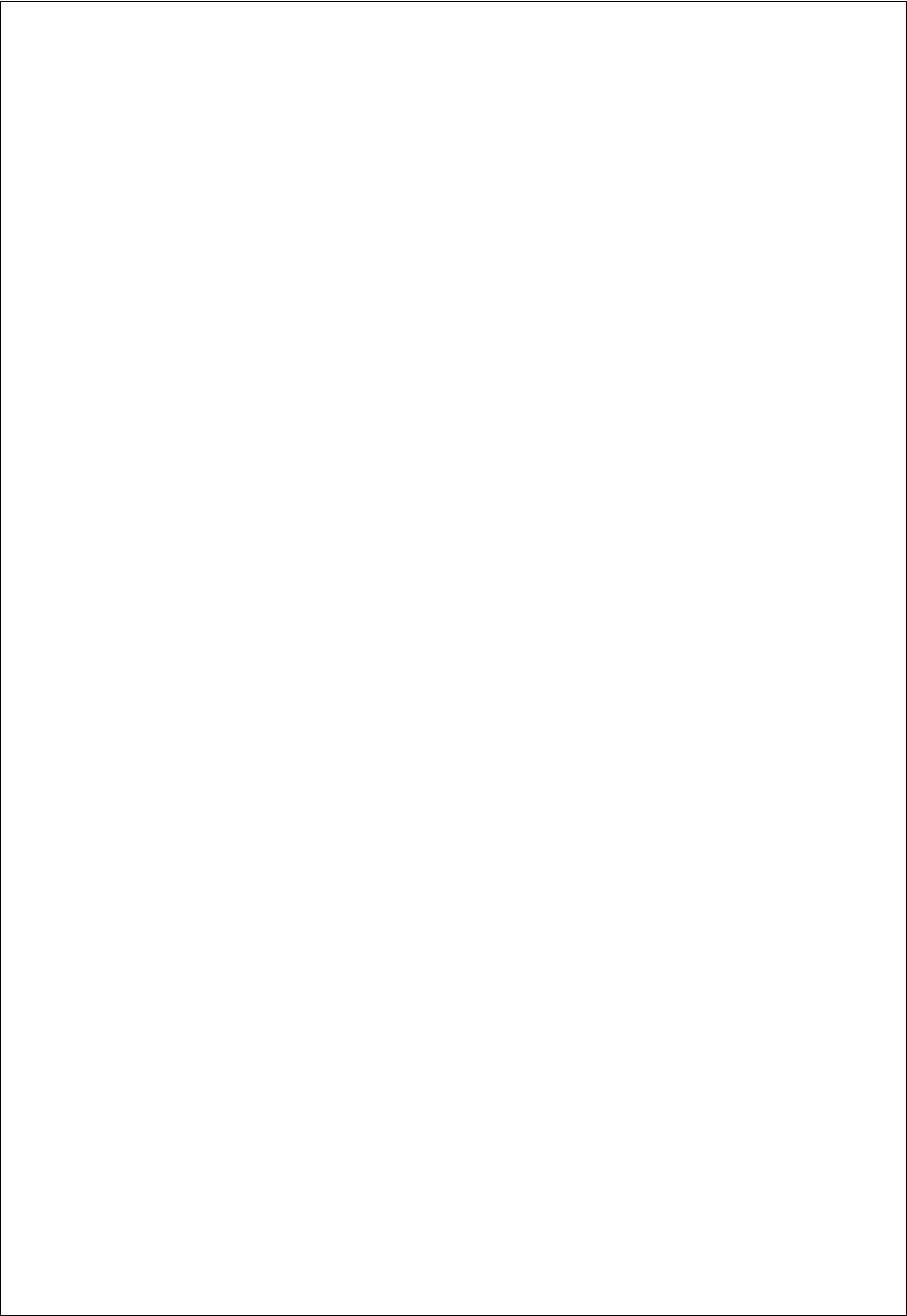
$$R_2 / (R_1 + R_2) = 0.158 \Rightarrow R_2 = 11.58 \text{ k}\Omega$$

$$\text{Choose, } R_1 = 56 \text{ k}\Omega \text{ and } R_2 = 12 \text{ k}\Omega$$

$$X_E = R_E / 10 = 600 / 10 = 60 \Omega$$

$$C_E = 1 / (2\pi f X_E) = 26.5 \mu\text{F} \quad (\text{for } f = 1 \text{ kHz}),$$

$$\text{Choose Coupling capacitors } C_1 = C_2 = 1 \mu\text{F}$$



PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Set $V_{in} = 2V$ in the signal generator. Keeping input voltage constant, vary the frequency from 1Hz to 3MHz in regular steps.
3. Note down the corresponding output voltage.
4. Plot the graph: Gain in dB Vs Frequency in Hz.
5. Calculate the Bandwidth from the Frequency response graph.

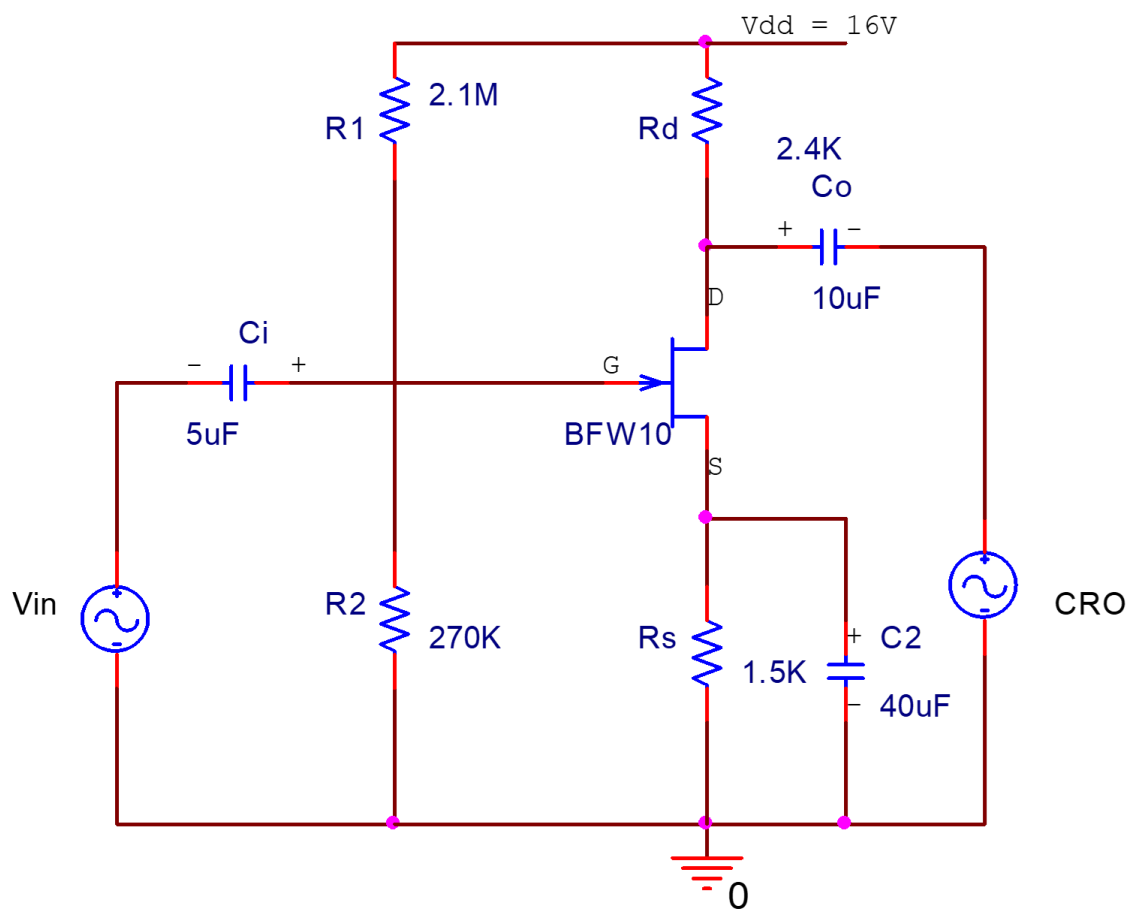
REVIEW QUESTIONS:

1. What are the different operating regions of a BJT based on junction biasing?
2. Why is the Common Emitter (CE) configuration preferred over the Common Base (CB) configuration for amplification?
3. Which applications commonly use the Common Emitter amplifier?
4. What are the typical input and output impedances of a CE amplifier?
5. How does a Common Emitter amplifier provide voltage and current gain?
6. What is meant by the frequency response of a CE amplifier?
7. When is the gain of a CE amplifier considered to be in the mid-frequency region?
8. What is the significance of the lower and upper cutoff frequencies in a CE amplifier?
9. How is the bandwidth of a CE amplifier determined from its frequency response?
10. Why does the gain of a CE amplifier decrease at low and high frequencies?

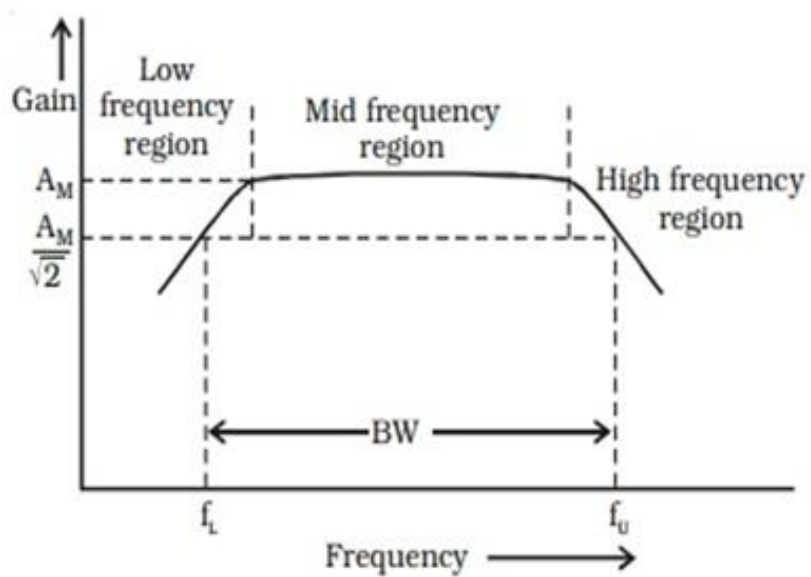
RESULT:

Thus a BJT CE Amplifier with voltage divider bias was designed and plotted the frequency response curve.

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 6 (b) FREQUENCY RESPONSE OF CS AMPLIFIER

AIM:

To construct a Common Source Amplifier and to obtain its frequency response curve and bandwidth.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	FET	BFW10	1
2	Resistors	2.1M Ω , 270k Ω , 2.4k Ω , 1.5	Each One
3	Capacitors	5 μ F, 10 μ F, 40 μ F	Each One
4	Function Generator	(0-3)MHz	1
5	CRO/DSO	(0-20)MHz	1
6	Regulated Power Supply	(0-30)V	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

The common source is the most commonly used MOSFET amplifier. The name “common source” comes from the fact that when the source terminal is grounded, it becomes a common terminal for both drain and gate terminals. The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier.

- As a transconductance amplifier, the input voltage is seen as modulating the current going to the load.
- As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law.

However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics.

DESIGN:

Given:

$$R_1 + R_2 = 2370k\Omega, R_s = 1.5k\Omega, I_{DSS} = 8mA \text{ and } V_p = -4V$$

$$I_D = 2.417mA$$

$$I_D = I_{DSS}(1 - V_{GS}/V_p)^2 \text{ --- (1)}$$

$$\text{By Solving } V_{GS} = -1.8025V$$

$$\text{To Find } V_S: V_S = I_{DSS} R_s = 3.6255V$$

$$V_G = V_{GS} + V_S = -1.8025 + 3.6255 = 1.823V$$

To Find R_1, R_2 :

$$V_G = (R_2/R_1 + R_2)V_{DD},$$

TABULATION:

$V_i =$ Volts

S.No	Frequency (Hz)	Output voltage (V_o) Volts	Gain = V_o / V_i	Gain in dB = $20 \log (V_o/V_i)$

$$1.823 = (R2/2370K\Omega)16$$

$$R2 = 270K\Omega$$

$$R1 + R2 = 2370K\Omega$$

$$R1 = 2370 - 270 = 2.1M\Omega$$

To Find RD:

$$VDS = VDD - IDR D - IDRS$$

$$RD = VDD - (VDS - IDRS)/ID = 16 - (6.5737 - 3.6255)/2.471 * 10^{-3}$$

$$RD = 2.4K\Omega$$

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The regulated power supply is turned on and its voltage level is adjusted to the value of V_{CC} needed.
3. The AFO was switched on and voltage level adjusted to be a suitable value V_s . This level was maintained constant throughout the experiment.
4. The frequency of the oscillator was varied over its working range in suitable steps.
5. For each frequency setting, the corresponding value of output voltage V_o is noted.
6. The voltage gain A_v , given by $20 \log (V_o/V_i)$ is computed for each frequency setting.

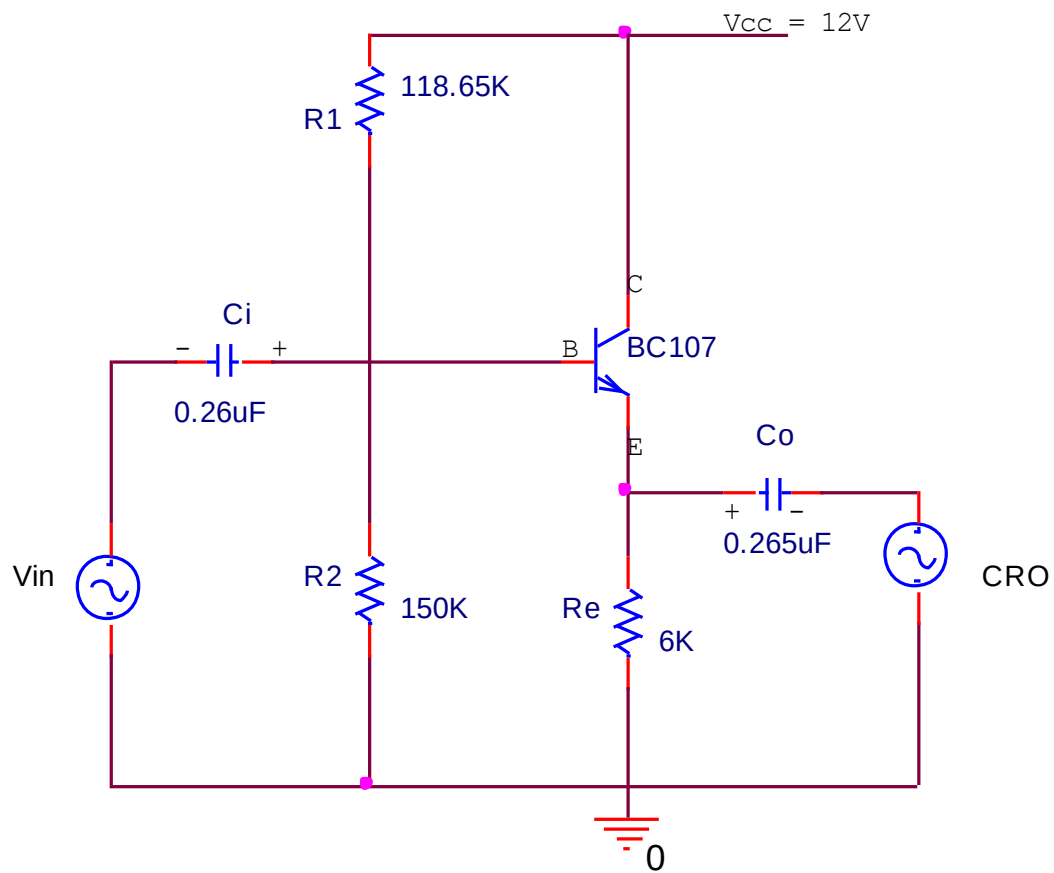
Review Questions:

1. What is the difference between FET and BJT?
2. FET is unipolar or bipolar?
3. Draw the symbol of FET?
4. What are the applications of FET?
5. FET is voltage controlled or current controlled?
6. Draw the equivalent circuit of common source FET amplifier?
7. What is the voltage gain of the FET amplifier?
8. Write the input and output impedance of FET amplifier.
9. What are the FET parameters?
10. What are the applications of FET?

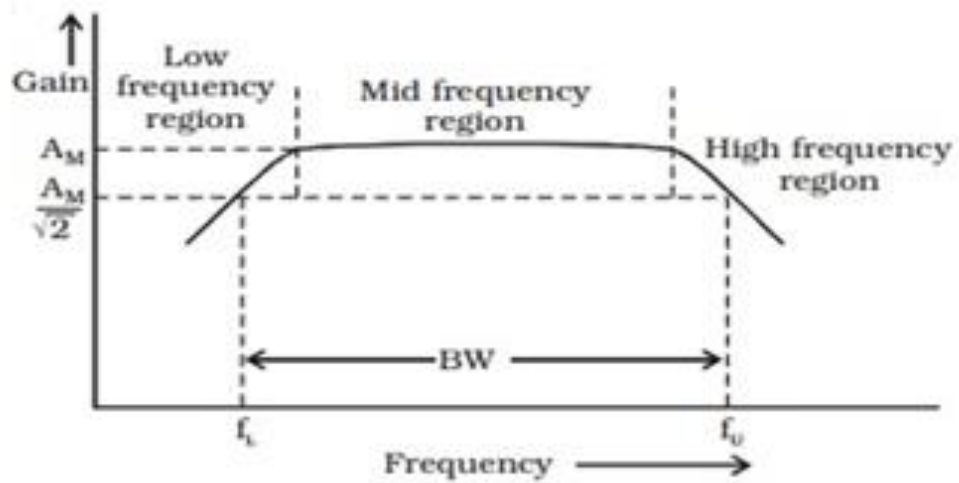
RESULT:

Thus the frequency response for the Common Source amplifier was designed and its frequency response, bandwidth was obtained.

CIRCUIT DIAGRAM:



MODEL GRAPH



Ex. No.: 7 (a) FREQUENCY RESPONSE OF CC AMPLIFIER

AIM:

To design a Common Collector amplifier using voltage divider bias to determine the frequency response.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	BJT	BC107	1
2	Resistors	6K, 118.65K, 150K	Each One
3	Capacitors	0.265μF, 0.26μF	Each One
4	Function Generator	(0-3)MHz	1
5	CRO/DSO	(0-20)MHz	1
6	Regulated Power Supply	(0-30)V	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

A common collector amplifier is also known as an emitter follower or voltage follower. In this circuit the base terminal of the transistor serves as the input, the emitter as the output and the collector is common to both. The common collector amplifier has a voltage gain of unity or larger bandwidth. The circuit has large input impedance and small output impedance. The circuit is useful as a voltage buffer between a source with large output impedance and small load impedance.

DESIGN:

$$V_{CC} = 12V \quad I_C = 1mA \quad \beta = 250$$

$$\text{Let } V_{CE} = \frac{V_{CC}}{2} ; \quad V_{CE} = 6V$$

$$V_E = \frac{V_{CC}}{2} \quad \text{and} \quad I_E = I_C$$

$$R_E = \frac{V_E}{I_E} = 6k\Omega$$

$$R_2 = 0.1 \times h_{fe} \times R_E = 150k\Omega$$

$$V_B = V_{BE} + V_E = 6.7V$$

$$V_B = \frac{V_{CC} R_2}{(R_1 + R_2)} \quad R_1 = \frac{V_{CC} R_2 - V_B R_2}{V_B} = 118.65k\Omega$$

Design of input and output capacitor:

$$h_{ie} = \beta r_e = 6.5k\Omega \quad \text{where } r_e = \frac{26mV}{I_E}$$

$$X_{ci} = (R_B // h_{ie}) / 10 = 592 \Omega \quad \text{where } R_B = R_1 // R_2$$

$$C_i = \frac{1}{2\pi f X_{ci}} = 0.26 \mu F \quad \text{for } f = 1000 \text{ Hz}$$

$$X_{co} = \frac{R_E}{10} = 600 \Omega$$

$$C_o = \frac{1}{2\pi f X_{co}} = 0.265 \mu F \quad \text{for } f = 1000 \text{ Hz}$$

TABULATION:

$V_i =$ Volts

S.No	Frequency (Hz)	Output voltage (Vo) Volts	Gain =Vo / Vi	Gain in dB = 20 log (Vo/Vi)

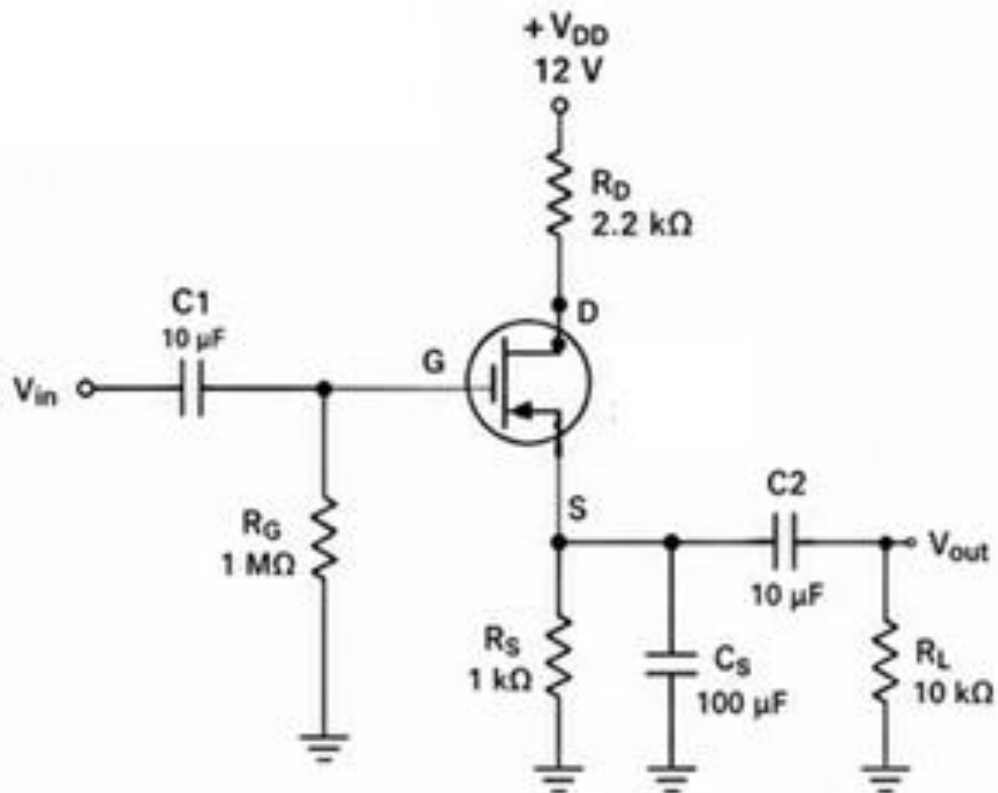
REVIEW QUESTIONS:

1. What are the practical applications of a Common Collector (CC) amplifier?
2. Why the Common Collector amplifier also called an emitter follower?
3. What is the typical voltage gain of a CC amplifier?
4. How do the input and output impedances of a CC amplifier compare with those of a CE amplifier?
5. To which terminal is the collector connected in a Common Collector amplifier circuit?
6. Which type of biasing is commonly used in a CC amplifier circuit?
7. What is the relationship between the current gains α , β , and γ of a transistor?
8. How does the frequency response of a CC amplifier differ from that of a CE amplifier?
9. Why the Common Collector amplifier mainly used for impedance matching rather than voltage amplification?
10. What are the major differences among Common Base (CB), Common Emitter (CE), and Common Collector (CC) amplifier configurations?

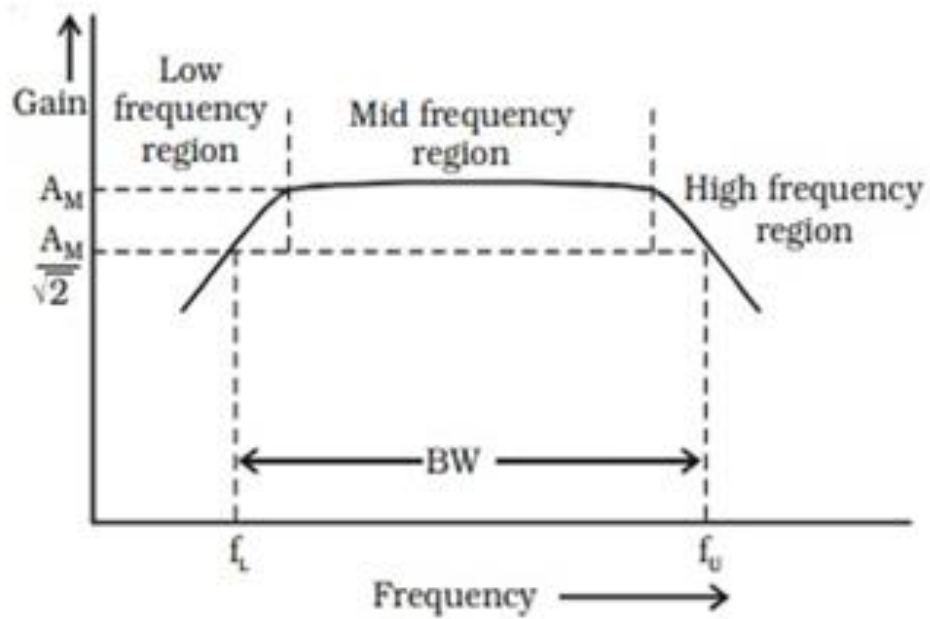
RESULT:

Thus the Common Collector amplifier was designed using voltage divider bias and its frequency response was determined.

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 7 (b) FREQUENCY RESPONSE OF CD AMPLIFIER

AIM:

To design a CD amplifier to determine its frequency response.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	FET	BFW10	1
2	Resistors	1M Ω , 10K Ω , 2.2K Ω , 1K Ω	Each One
3	Capacitors	10 μ F, 100 μ F	2,1
4	Function Generator	(0-3)MHz	1
5	CRO	(0-20)MHz	1
6	Regulated Power Supply	(0-30)V	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

A Common Drain (CD) amplifier, also known as a Source Follower, is a type of FET amplifier in which the drain terminal is common to both the input and output circuits. The input signal is applied to the gate terminal, and the output is taken from the source terminal through a source resistor.

The Common Drain amplifier provides a voltage gain that is approximately equal to unity (slightly less than one). Although it does not provide significant voltage amplification, it offers high input impedance and low output impedance, making it suitable for impedance matching applications.

The frequency response of a Common Drain amplifier describes the variation of voltage gain with respect to the input signal frequency. At low frequencies, the gain decreases due to the effect of coupling and bypass capacitors. In the mid-frequency region, the gain remains nearly constant and the amplifier operates with maximum efficiency. At high frequencies, the gain decreases because of the internal capacitances of the FET and stray circuit capacitances.

The frequencies at which the gain falls to 70.7% of its mid-band value are known as the lower cutoff frequency ((f_L)) and upper cutoff frequency ((f_H)). The range of frequencies between these two cutoff frequencies is called the bandwidth of the amplifier.

DESIGN SPECIFICATION:

Source Voltage

$$V_S = I_D R_S$$

Drain Voltage

$$V_D = V_{DD} - I_D R_D$$

Gate Voltage

$$V_G = 0V$$

(For self-bias configuration)

Gate-to-Source Voltage

$$V_{GS} = V_G - V_S$$

TABULATION:

$V_i =$ Volts

S.No	Frequency (Hz)	Output voltage (V_o) Volts	Gain = V_o / V_i	Gain in dB = $20 \log (V_o/V_i)$

Drain-to-Source Voltage

$$V_{DS} = V_D - V_S$$

Input Coupling Capacitor

$$C_1 = \frac{1}{2\pi R_G f_L}$$

Output Coupling Capacitor

$$C_2 = \frac{1}{2\pi R_L f_L}$$

Source Bypass Capacitor

$$C_S = \frac{1}{2\pi R_S f_L}$$

Voltage Gain

$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

or approximately,

$$A_v \approx 1$$

Input Impedance

$$Z_{in} \approx R_G$$

Output Impedance

$$Z_{out} \approx \frac{1}{g_m}$$

Lower Cut-off Frequency

$$f_L = \frac{1}{2\pi RC}$$

Upper Cut-off Frequency

$$f_H = \frac{1}{2\pi RC}$$

Bandwidth

$$BW = f_H - f_L$$

Mid-band Gain in dB

$$A_v(dB) = 20\log_{10}(A_v)$$



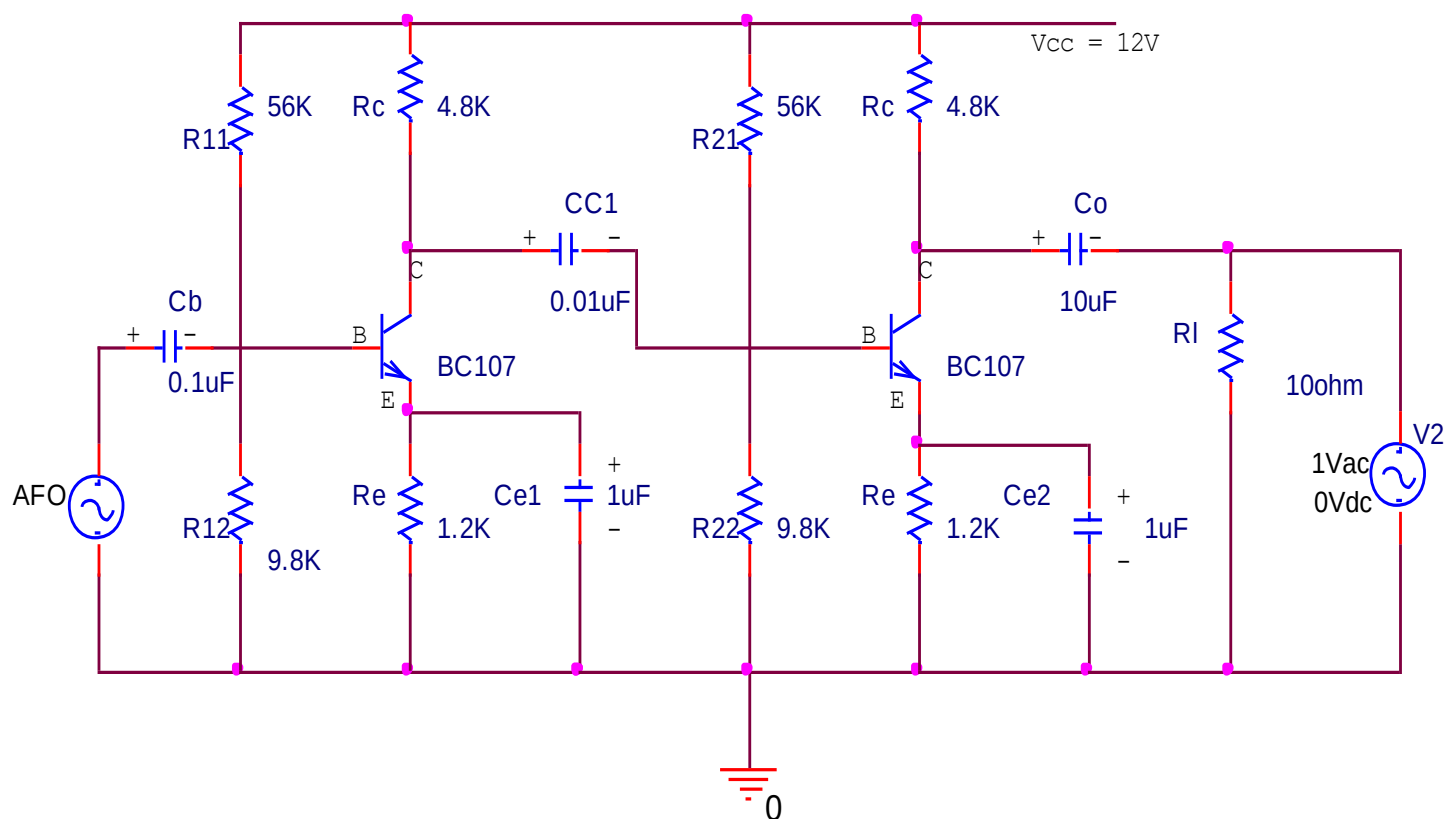
REVIEW QUESTIONS:

1. What is a Common Drain (CD) amplifier?
2. Why the Common Drain amplifier also known as a source follower?
3. How the input signal applied and the output signal obtained in a CD amplifier?
4. Which terminal of the FET is common to both the input and output circuits in a CD amplifier?
5. What is the typical voltage gain of a Common Drain amplifier?
6. How do the input and output impedances of a CD amplifier compare with those of a Common Source amplifier?
7. Where the Common Drain amplifier commonly used in practical applications?
8. When the CD amplifier preferred over a Common Source amplifier?
9. What is meant by the frequency response of a CD amplifier?
10. Why does the gain of a CD amplifier decrease at very low and very high frequencies?

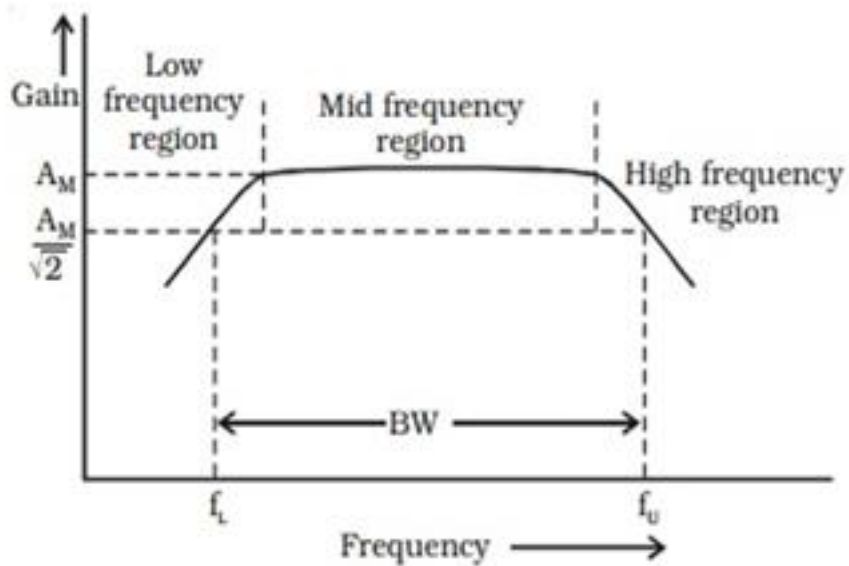
RESULT:

Thus the CD amplifier was designed and its frequency response was determined.

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 8 FREQUENCY RESPONSE OF CASCADE AMPLIFIER

AIM:

To design a Cascade amplifier to determine the frequency response and its bandwidth.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Transistor	BC-107	02
2	Capacitors	0.1 μ F, 0.01 μ F,	Each One
3	Resistors	56 K, 9.8 K, 1.2 K, 4.8 K	Each Two
4	Function Generator	0-1MHZ	1
5	CRO/DSO	20MHZ	1
6	Regulated Power Supply	0-30V	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

When two amplifiers are connected in such a way that the output signal of first serves as the input signal of second, the amplifiers are said to be connected in cascade. Cascading is done to increase the gain of the amplifier. Each stage of the cascade amplifier should be biased at its designed level. It is possible to design a multistage cascade in which each stage is separately biased and coupled to the adjacent stage using blocking or coupling capacitors. In this circuit each of the two capacitors C1&C2 isolate the separate bias network by acting as open circuits to DC and allow only signals of sufficient high frequency to pass through cascade.

DESIGN EQUATIONS:

Given Data: $h_{fe1}=h_{fe2}=200$, $R_L=10\Omega$, $I_{E1}=I_{E2}=1mA$, $s_1=s_2=8$, $f=100HZ$, $V_{CC}=12V$

For fixing the optimum operating point Q, mark the middle of the dc load line and the corresponding $V_{CE}(Q)$ and I_CQ values are determined.

$$V_{CE}(Q) = V_{CC}/2 = 12/2 = 6$$

1.By choosing drop across R_E as $0.1V_{CC}$.

$$V_E = V_{CC}/10 = 12/10 = 1.2V$$

2.In transistor since base current is very small, so I_E is approximately equal to

$$I_C(I_E = I_C), I_{ERE} = 1.2V; I_{CRE} = 1.2V ; R_E = V_E/I_E = 1.2/1mA = 1.2K\Omega$$

3.Applying Kirchoff's voltage law to the collector circuit in the diagram

$$R_C = (V_{CC} - V_{CE} - V_E)/I_C = (12 - 6 - 1.2)/1mA = 4.8K\Omega$$

4.The voltage across R_2 is $V_{BB} = V_{CC} * R_2/(R_1 + R_2)$ -----(1)

$$V_{BB} = V_{BE} + I_{ERE} = 0.6 + (10^{-3})(10^3 * 1.2) = 1.8V$$
 -----(2)

Substitute(2)in(1)

$$1.8 = 12R_2/(R_1 + R_2)$$

$$R_2 = 0.1761R_1$$
 -----(a)

$$S = 1 + R_1R_2/(R_1 + R_2)R_E$$

TABULATION:

$V_i =$ Volts

S.No	Frequency (Hz)	Output voltage (V_o) Volts	Gain = V_o / V_i	Gain in dB = $20 \log (V_o/V_i)$

$$S = 1 + R_1 R_2 / (R_1 + R_2) 1.2 * 10^3 \text{ --- (b)}$$

By solving (a) and (b) we get $R_1 = 56K\Omega$ $R_2 = 9.8K\Omega$

Capacitor calculations:

To provide low reactances almost short circuit at the operating frequency. f

$$= 100\text{HZ}. X_{cE} = 0.1 R_E X_{ci} = 0.1 Z_i, X_{co} = 0.001 Z_0, X_{CE} \ll R_E, X_{CE} = R_E / 10$$

$$= 1.2K / 10 = 120 \Rightarrow C_E = 0.132\mu F$$

$$X_{Ci} = Z_i / 10 \text{ Where } Z_i = h_{ie} // R_E = 8.18K\Omega \Rightarrow C_i = 1.96\mu F$$

$$X_{Co} = Z_0 / 1000$$

$$Z_0 = R_L // R_C = 827\Omega$$

$$\Rightarrow C_O = 19.2\mu F$$

Standard values

$$R_{11} = R_{21} = R_1 = 56K\Omega,$$

$$R_{22} = R_{12} = R_2 = 9.8K\Omega,$$

$$R_{E1} = R_{E2} = R_E = 1.2K\Omega,$$

$$R_{C1} = R_{C2} = R_C = 4.8K\Omega,$$

$$R_L = 10\Omega,$$

$$C_i = 0.1\mu F, C_C = 0.01\mu F, C_E = 1\mu F, C_O = 10\mu F$$

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Apply the supply voltage, $V_{cc} = 12V$.
3. Make sure that transistor is operating in active region by keeping V_{CE} half of V_{cc} .
4. Now feed an ac signal of 20mV at the input of the amplifier with different frequencies ranging from 100Hz to 1MHz and measure the amplifier output voltage, V_o
5. Now calculate the gain in dB at various input signal frequencies.
6. Draw a graph with frequencies on X-axis and gain in dB on Y-axis.

REVIEW QUESTIONS:

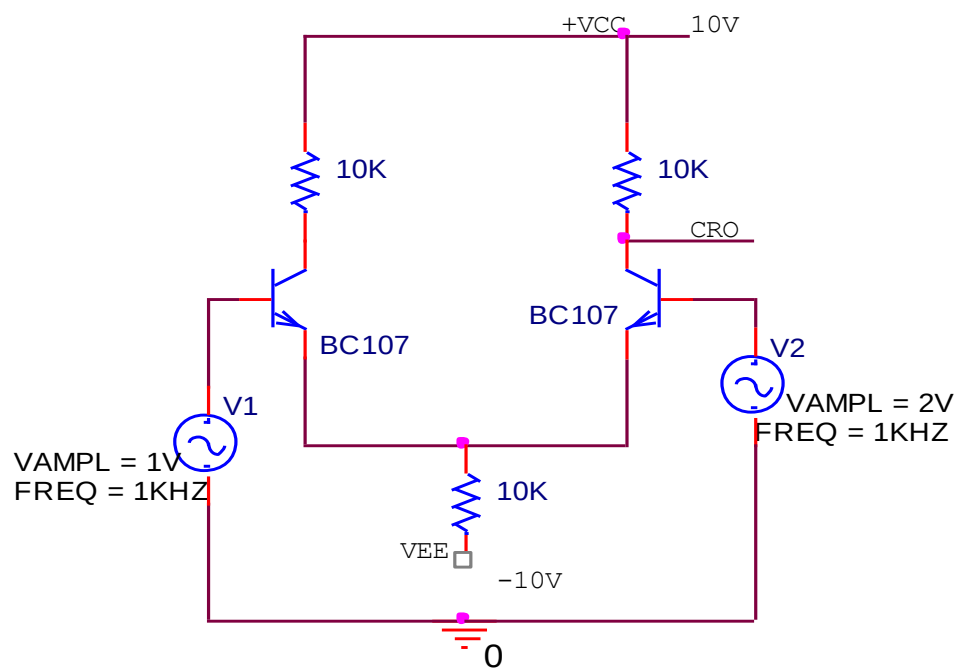
1. What is meant by a cascade amplifier?
2. Why are RC-coupled amplifiers widely used as voltage amplifiers?
3. How is the overall voltage gain of a cascade amplifier calculated?
4. Why does the voltage gain of an RC-coupled cascade amplifier decrease at low frequencies?
5. Why does the voltage gain of an RC-coupled cascade amplifier decrease at high frequencies?
6. Which components are mainly responsible for the reduction in gain at low frequencies?
7. What are the advantages of an RC-coupled cascade amplifier?
8. How does a cascade amplifier differ from a cascode amplifier?
9. Where are cascade amplifiers commonly used in practical electronic systems?
10. When is a cascade amplifier preferred over a single-stage amplifier?

RESULT:

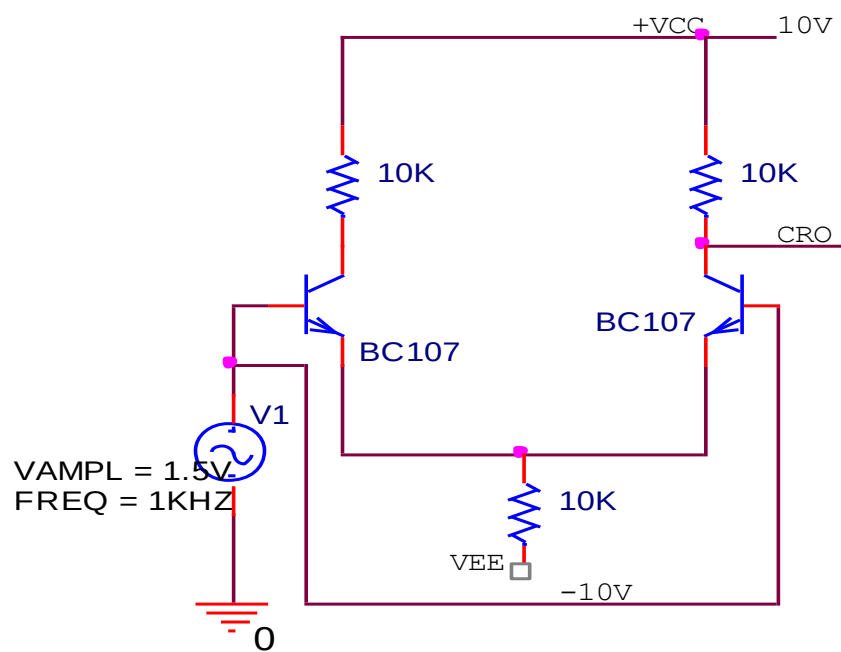
Thus the Cascade amplifier was designed and its frequency response, bandwidth was determined.

CIRCUIT DIAGRAM:

DIFFERENTIAL MODE



COMMON MODE



Ex. No.: 9 CMRR MEASUREMENT OF DIFFERENTIAL AMPLIFIER

AIM:

To construct a differential amplifier using BJT to determine Common Mode Rejection Ratio (CMRR).

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	BJT	BC107	2
2	Resistor	1k Ω , 470 Ω	2,1
3	Function Generator/AFO	(0-3)MHz	2
4	CRO/DSO	(0-20)MHz	1
5	RPS	(0-30)V	2
6	Bread Board		1
7	Connecting Wires		Few

THEORY:

The function of a difference or differential amplifier is to amplify the difference between two signals. The need for differential amplifiers arises in many physical measurements, in medical electronics and in direct coupled amplifier applications. In an ideal differential amplifier, the output V_o is given by

$$V_o = A_d (V_1 - V_2) = A_d V_d \quad \text{Where } V_d = V_1 - V_2$$

A_d is the gain of the amplifier; V_1 and V_2 are the input signals.

The output depends not only on the difference signal V_d but also on the average signal called common mode signal V_c . $V_c = (V_1 + V_2)/2$. Output of the amplifier for the common mode signal is given by $V_o = A_{cm}(V_1 + V_2)/2 = A_{cm}V_c$. A_{CM} is the common mode gain. Common Mode Rejection Ratio of the differential amplifier is given by $CMRR = A_d / A_{CM}$

DESIGN:

Given specifications:

$$V_{CC} = 12V, I_C = 1.2mA, V_{CE} = 5V$$

Assume $Q_1 = Q_2$

where Q_1 = Transistor 1 and Q_2 = Transistor 2.

The collector resistance R_{c1} is given by using KVL at the transistor 1

$$V_{CC} = I_C R_{c1} - V_{CE} - I_{e1} R_{e1}$$

$$R_{c1} = (V_{CC} + V_{CE} + I_{e1} R_{e1}) / I_C,$$

where $V_{CE} = 5V$ and $I_C = 1.2mA$, $I_{e1} = I_C/10$ and assume $R_{c1} = 470\Omega$

Now $R_{c1} = 1k\Omega$.

TABULATION:**Differential Mode Gain:**

I /P Voltage (Volts)		$V_d = V_1 - V_2$ (Volts)	O/P Voltage (V_0) (Volts)	Gain A_d V_0/V_d
V_1	V_2			

Common Mode Gain:

I /P Voltage (Volts)		$V_c = (V_1 + V_2)/2$ (Volts)	O/P Voltage (V_0) (Volts)	Gain A_{cm} V_0/V_c
V_1	V_2			

PROCEDURE:

1. Connect the circuit as shown in Figure.
2. For difference mode circuit, set the input voltage V_1 and V_2 .
3. Measure the output voltage V_o between collector of Q_1 and Q_2 .
4. Calculate the difference mode gain $A_d = V_o / V_d$.
5. Connect the circuit as shown in the Figure: 2.
6. Measure the output voltage V_o .
7. Calculate the common mode gain. $A_{CM} = V_o / V_C$.
8. Determine CMRR value using difference mode gain and common mode gain.

REVIEW QUESTIONS:

1. What is the primary function of a differential amplifier?
2. How does a differential amplifier respond to differential and common mode signals?
3. What is meant by the Common Mode Rejection Ratio (CMRR)?
4. How is the CMRR of a differential amplifier calculated?
5. What is the common mode gain of a differential amplifier?
6. Which type of signal is referred to as a common mode signal?
7. What is the value of CMRR for an ideal differential amplifier?
8. Why does a practical differential amplifier exhibit non-ideal behavior?
9. Where are differential amplifiers commonly used in electronic circuits?
10. When is a high value of CMRR desirable in a differential amplifier?

RESULT:

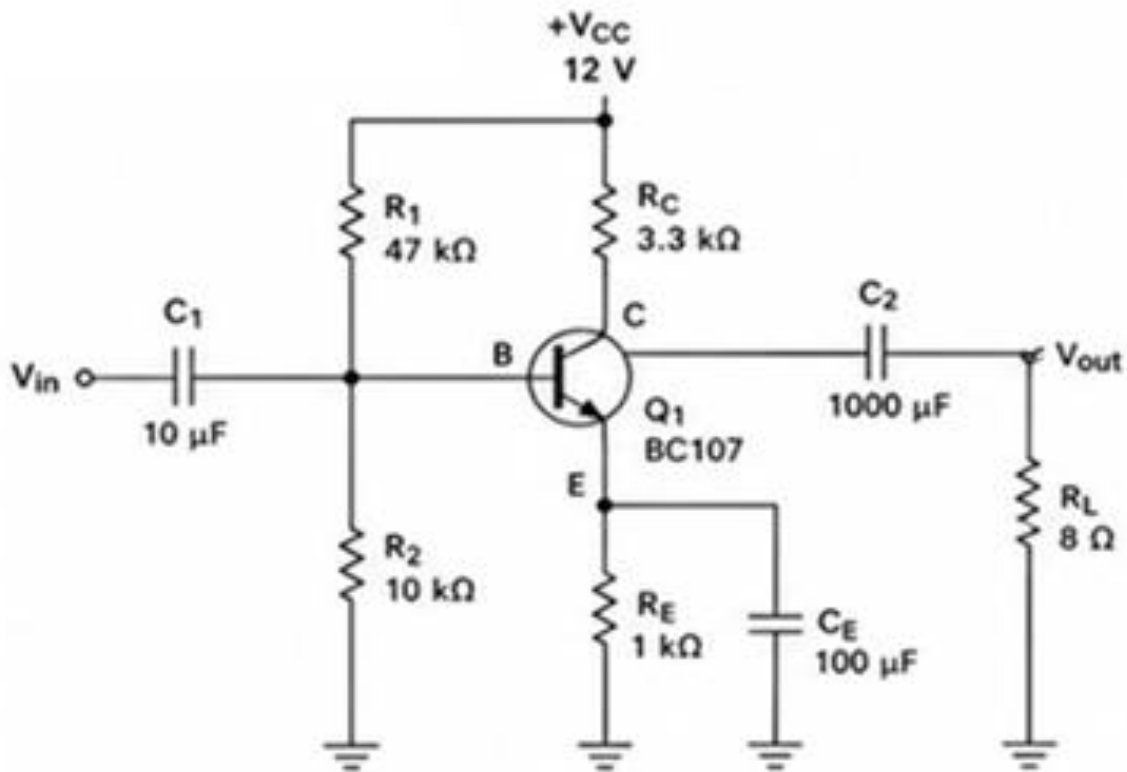
Thus the differential amplifier using BJT was designed and its Common Mode Rejection Ratio (CMRR) was determined.

Differential mode : _____

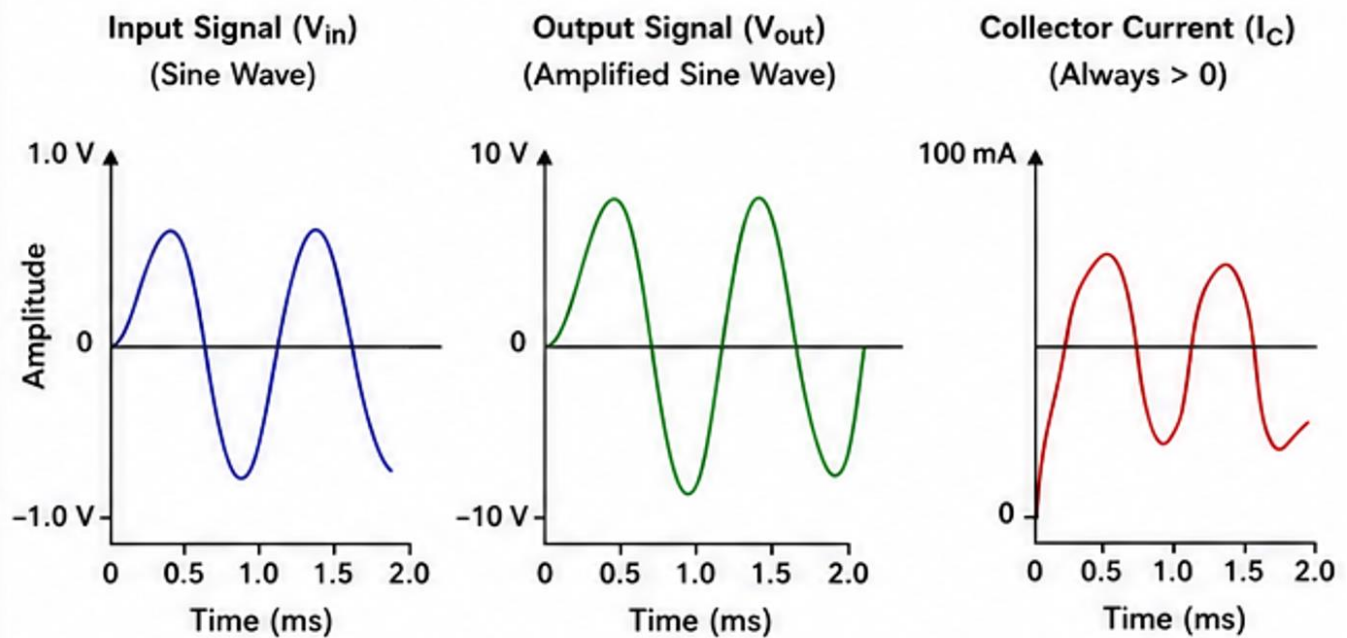
Common mode : _____

CMRR :

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 10 CLASS A POWER AMPLIFIER

AIM:

To determine the operation and performance characteristics of a Class A power amplifier.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1.	Transistor	BC107	1
2.	Resistor	47K Ω , 10K Ω , 3.3K Ω , 1K Ω , 8 Ω	Each One
3.	Capacitors	10 μ f, 100 μ f, 1000 μ f	Each One
4.	CRO	20MHz	1
5.	Regulated Power Supply	(0-30) V	1
6.	Function Generator	20MHz	1
7.	Bread Board		1
8.	Connecting Wires		Few

THEORY:

A Class A power amplifier is a power amplifier in which the active device (transistor) conducts for the entire 360° of the input signal cycle. The transistor is biased in the active region so that it remains ON at all times, even when no input signal is applied.

When an AC input signal is applied to the base of the transistor, the collector current varies according to the variations in the input signal. During the positive half cycle of the input signal, the collector current increases, and during the negative half cycle, the collector current decreases. Since the transistor never turns OFF, the complete input waveform is reproduced at the output with very low distortion.

The operating point of the transistor, known as the quiescent point or Q-point, is generally set near the center of the DC load line to allow maximum undistorted output signal swing. Due to continuous conduction, Class A amplifiers provide excellent linearity and high fidelity amplification. However, the transistor continuously draws current from the power supply, even in the absence of an input signal. As a result, Class A amplifiers have low efficiency and dissipate a considerable amount of power in the form of heat. Therefore, a suitable heat sink is generally required for the power transistor used in practical circuits.

TABULATION:

S.No	Vin	Vout	Ic	Pin	Pout	Efficiency

Characteristics of Class A Power Amplifier:

- Transistor conduction angle is 360° .
- The transistor remains ON throughout the entire input cycle.
- Provides very low distortion and excellent linearity.
- Offers good signal fidelity and waveform reproduction.
- Has low efficiency due to continuous power dissipation.
- Requires proper heat sinking for safe operation.

PROCEDURE:

1. Assemble the circuit as per the circuit diagram.
2. Verify all connections before switching ON the supply.
3. Apply the specified DC supply voltage.
4. Apply the required input signal.
5. Measure input and output values.
6. Record readings in the observation table.
7. Perform necessary calculations.
8. Plot the required graph or waveform.
9. Determine the required parameters.
10. Tabulate the results.

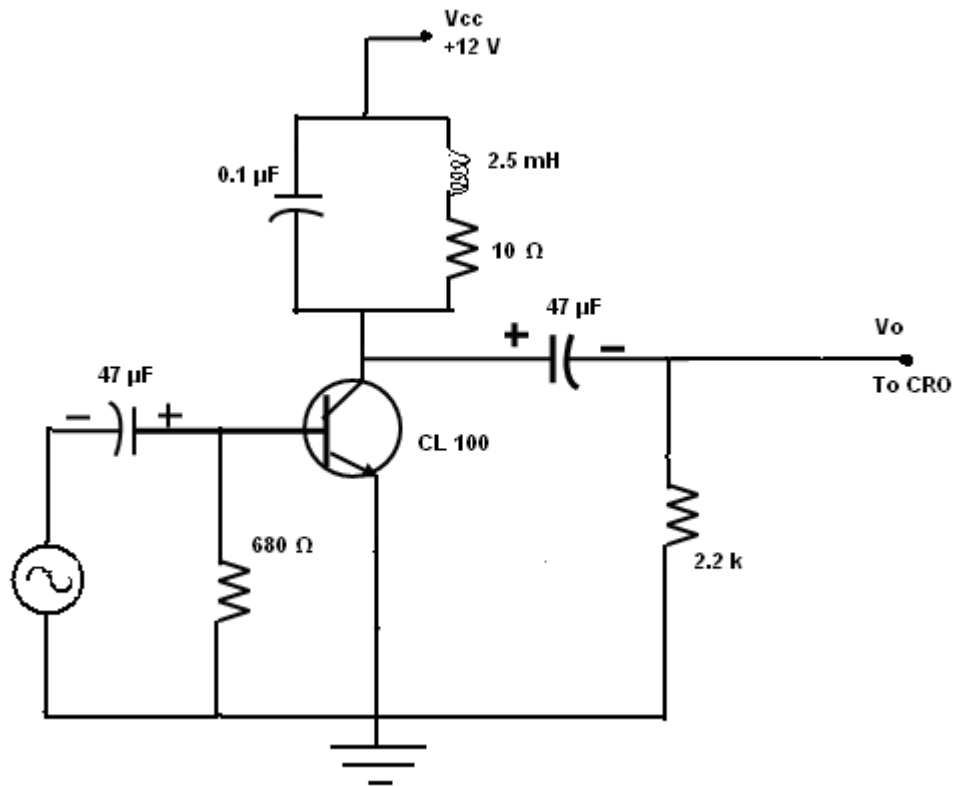
REVIEW QUESTIONS:

1. What is a Class A power amplifier?
2. Why is it called a Class A amplifier?
3. What is the conduction angle of a Class A power amplifier?
4. In which operating region does the transistor work in a Class A amplifier?
5. Why is the transistor biased at the center of the load line in a Class A amplifier?
6. What is the function of the Q-point in a Class A amplifier?
7. Why does a Class A amplifier produce low distortion?
8. Why is the efficiency of a Class A amplifier low?
9. Why is a heat sink required in a Class A power amplifier?
10. What are the practical applications of a Class A power amplifier?

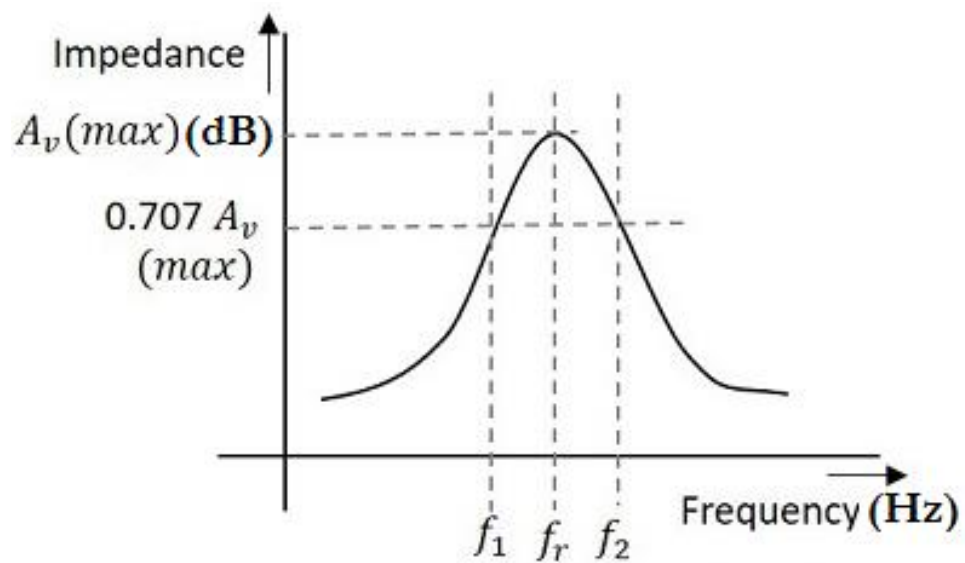
RESULT:

The operation and performance characteristics of a Class A power amplifier was determined and the graph was plotted for the obtained values.

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex. No.: 11 CLASS C POWER AMPLIFIER

AIM:

To observe the operation and frequency response characteristics of a Class C power amplifier.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	Transistor	BC107	1
2	Resistor	4.2K Ω , 500 Ω , 197K Ω , 2.2K Ω ,	Each One
3	Capacitors	0.1 μ f 0.001 μ f, 100 μ f	2 1
4	Decade Inductance Box	-	1
5	Dual Trace CRO	(0- 20MHz)	1
6	Regulated Power Supply	(0-30) V	1
7	Function Generator	20MHz	1
8	Bread Board		1
9	Connecting Wires		Few

THEORY:

In a class-c amplifier, the transistor is in the active region for less than half cycle. It means, conduction takes place for less than one half cycle. This implies that the collector current of a class-c amplifier is highly non-sinusoidal because current flows in pulses. The load is a tuned circuit which converts the non-sinusoidal o/p to nearly sinusoidal form. Because of the flow of collector current less than 180°, the average collector current is much less, if hence losses are less, so efficiency is very high.

$$\text{Resonance frequency } (f_r) = 1/2\pi\sqrt{LC}.$$

At resonant frequency, the inductance of parallel resonant circuit is very high and is purely resistive. When the circuit is tuned to the resonant frequency, the voltage across R_1 is maximum and sinusoidal. The tuned circuit helps in rejecting the harmonics that are developed in the transistor due to class-C operation.

The class-c tuned power amplifier consists of an LC tuned circuit in the collector of Q. R_1 & R_2 provides the necessary biasing for Q. C_1 & C_3 are the i/p and o/p coupling capacitors. The Q point is kept just above the cut-off line on the dc load line. R_L is provided to load the amplifier.

TABULATION:

$V_{in} = \text{____} (v)$

Frequency(Hz)	$V_{out}(v)$	Gain(dB)= $20 \log(V_0/V_{in})$

PROCEDURE:

1. Connect the circuit as for circuit diagram
2. Calculate the theoretical resonant frequency $f_r = \frac{1}{2\pi\sqrt{LC}}$
3. Connect the input signal to the amplifier.
4. Keep input voltage zero initially and adjust frequency to around resonance frequency (f_r)
5. Observe the output waveform increase the input ac voltage until we get the maximum distorted output.
6. Vary the frequency in required steps surrounding resonant frequency and note down the corresponding output voltages & calculate gain.
7. Plot the graph between gain and frequency.

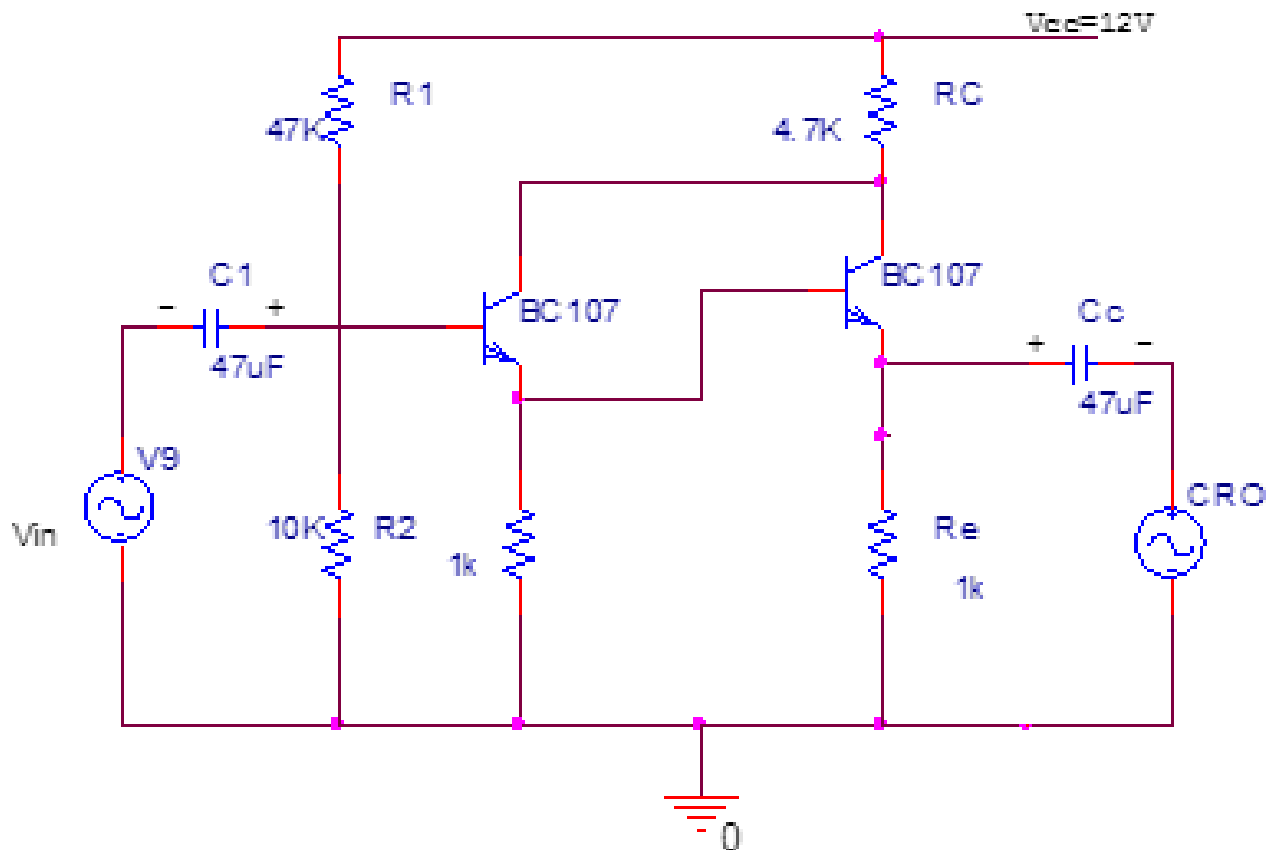
REVIEW QUESTIONS:

1. What is tuned amplifier? What are the various types of tuned amplifiers?
2. Why tuned amplifier cannot be used at low frequency?
3. What is the other name for tuned amplifier?
4. Mention the applications of tuned amplifiers.
5. State advantages and disadvantages of tuned amplifiers.
6. Compare amplifier, feedback amplifier & tuned amplifier.
7. List out the different coil losses.
8. What are the different types of neutralization?
9. What is the need for neutralization circuits?
10. Define loaded and unloaded Q.

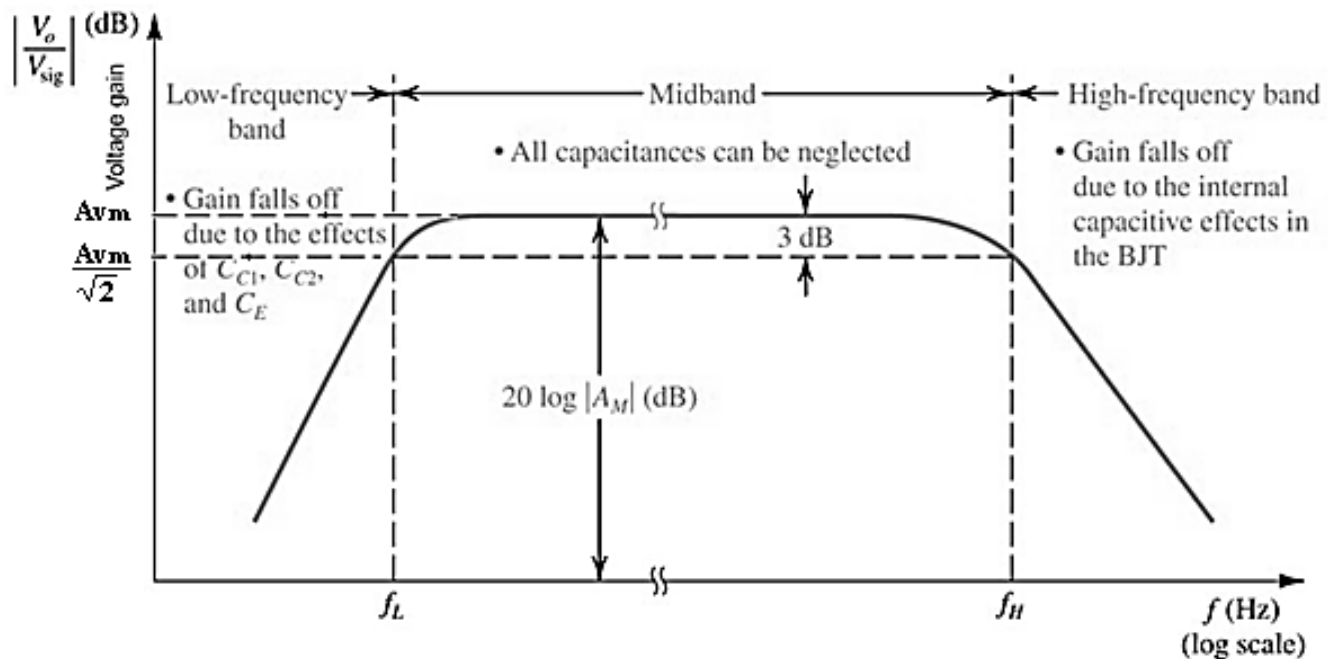
RESULT:

The frequency response characteristics of the Class C power amplifier were observed, and the lower cutoff frequency, upper cutoff frequency, and bandwidth were determined successfully.

CIRCUIT DIAGRAM:



MODEL GRAPH:



Ex .No.: 12 DARLINGTON AMPLIFIER

AIM:

To design a Darlington amplifier using BJT and determine its frequency response characteristics.

APPARATUS REQUIRED:

S.No	Components / Equipments	Specifications	Quantity
1	BJT	BC107	2
2	Resistors	47k Ω , 10k Ω , 4.7k Ω , 1k Ω	1,1,2
3	Capacitors	47 μ f, 100 μ f	2,1
4	Function Generator / AFO	(0-3)MHz	1
5	CRO/DSO	(0-20)MHz	1
6	Regulated Power Supply	(0-30)V	1
7	Bread Board		1
8	Connecting Wires		Few

THEORY:

A Darlington pair may be created using two npn devices, particularly in discrete circuit design, or through the use of an npn and a pnp. The resulting compound device may be considered as a single transistor and it will be used in either the CE or CC configuration. The current amplified by the first transistor is amplified further by the second one. This amplifier gives a much higher current gain. The Darlington amplifier has a voltage gain of unity. The circuit has large input impedance and small output impedance.

DESIGN:

$$V_{CC} = 12V \quad R_2 = 10K\Omega \quad I_C = 1mA$$

$$\text{The drop across } V_{CE} = 6V, V_E = \frac{V_{CC}}{10}, V_{CE} = \frac{V_{CC}}{2}$$

$$\text{The resistance across } R_C = \frac{V_{CC} - V_{CE} - V_E}{I_C} \approx 4.7k\Omega$$

Design of R_1 and R_2 :

$$\text{Drop across } R_E = 1V$$

$$\text{Drop across } V_{BE1} \text{ \& } V_{BE2} \text{ is } 0.6V$$

$$V_{R2} = V_{RE} - V_{BE1} - V_{BE2} = 2.2V$$

R_2 is assumed 10k Ω

$$\frac{V_{CC}R_2}{R_1 + R_2} = 2.2V \text{ by solving,}$$

$$R_1 = 44.5k\Omega \approx 47k\Omega$$

$$\text{Let } C_1 = 47\mu f \text{ and } C_2 = 47\mu f$$

TABULATION:**Vi = Volts**

S.No	Frequency (Hz)	Output voltage (Vo) Volts	Gain =Vo / Vi	Gain in dB = 20 log (Vo/Vi)

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The regulated power supply is turned on and its voltage level is adjusted to the value of V_{CC} needed.
3. The AFO was switched on and voltage level adjusted to be a suitable value V_s . This level was maintained constant throughout the Experiments.
4. The frequency of the oscillator was varied over its working range in suitable steps.
5. For each frequency setting, the corresponding value of output voltage V_o is noted.
6. The voltage gain A_v , given by $20 \log (V_o / V_i)$ is computed for each frequency setting.
7. The frequency response curve is plotted in a semi log graph sheet and BW is calculated.

REVIEW QUESTIONS:

1. What is a Darlington amplifier?
2. Why does a Darlington amplifier provide a very high input impedance?
3. How is the voltage gain of a Darlington amplifier compared with that of a single transistor amplifier?
4. Which applications commonly use a Darlington amplifier?
5. What is the function of the bootstrap circuit in a Darlington amplifier?
6. How do you determine the lower and upper cutoff frequencies of the amplifier?
7. Why is the current gain of a Darlington pair much higher than that of a single transistor?
8. Where is the output signal taken in a Darlington amplifier circuit?
9. When is a Darlington amplifier preferred over a conventional emitter follower circuit?
10. What are the main advantages and limitations of a Darlington amplifier?

RESULT:

Thus, the Darlington amplifier was designed using BJT and its frequency response characteristics were determined successfully.