

SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)
SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK



VII SEMESTER

PEC105 MIXED SIGNAL IC TESTING

Regulation – 2023

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING QUESTION BANK

UNIT I – MIXED SIGNAL TESTING				
Common Types of Analog and Mixed- Signal Circuits – Applications of Mixed-Signal Circuits – Post Silicon Production Flow - Test and Packing – Characterization versus Production Testing - Test and Diagnostic Equipment - Automated Test Equipments – Wafer Probers – Handlers – E-Beam Probers – Focused Ion Beam Equipments – Forced –Temperature.				
PART – A				
Q.No	Questions	CO	BT Level	Competence
1.	Define a mixed signal circuit?	CO1	BTL1	Remember
2.	List four examples of analog circuits	CO1	BTL1	Remember
3.	Mention four examples of mixed signal circuits?	CO1	BTL1	Remember
4.	Write the process of testing a typical mixed signal circuit?	CO1	BTL1	Remember
5.	What is Programmable Gain Amplifier (PGA)?	CO1	BTL1	Remember
6.	What is meant by Phase Locked Loops?	CO1	BTL1	Remember
7.	What is a Test Engineer?	CO1	BTL2	Understand
8.	What do you mean by Handlers?	CO1	BTL2	Understand
9.	When a PGA is combined with a digital logic block to keep a signal at a constant level, what is the combined circuit called?	CO1	BTL2	Understand
10.	Assume a particle of dust lands on a photomask during the photolithographic printing process of a metal layer. List at least one possible defect that might occur in the printed IC.	CO1	BTL2	Understand
11.	Why does the cleanliness of the air in a semiconductor fabrication area affect the number of defects in IC manufacturing?	CO1	BTL2	Understand
12.	Point out at least four production steps after wafers have been fabricated.	CO1	BTL1	Remember
13.	Why would it be improper to draw conclusions about a design based on characterization data from one or two devices?	CO1	BTL1	Remember
14.	List three main components of an ATE tester	CO1	BTL1	Remember
15.	What is the purpose of a DIB board?	CO1	BTL1	Remember
16.	What type of equipment is used to handle wafers as they are tested by an ATE tester?	CO1	BTL1	Remember
17.	List three advantages of concurrent engineering.	CO1	BTL1	Remember
18.	What is the purpose of a test plan?	CO1	BTL2	Understand
19.	State at least four challenges faced by the mixed signal test engineer.	CO1	BTL2	Understand
20.	Mention the use of E Beam Probers.	CO1	BTL1	Remember
21.	Name any two catastrophic defects?	CO1	BTL2	Understand
22.	In a cellular telephone, which type of mixed signal circuit converts the digital samples into speaker's voice?	CO1	BTL2	Understand
23.	Which type of mixed-signal circuit acts as a volume control for the cellular telephone earpiece?	CO1	BTL1	Remember
24.	State the role of handlers in Test and diagnosis of post silicon production	CO1	BTL2	Understand
PART – B				
1.	Explain in detail about the applications of Mixed Signal Circuits	CO1	BTL3	Apply
2.	Discuss in detail about the processes involved in Post Silicon Production Flow.	CO1	BTL3	Apply

3.	Explain the functional blocks of automated test equipment and the industrial developments in ATE	CO1	BTL4	Analyze
4.	Discuss the functionalities of wafer probers and handlers in Automated test equipment.	CO1	BTL4	Analyze
5.	What are the various testing equipment required to test a semiconductor device? Explain them in detail.	CO1	BTL4	Analyze
6.	Explain the role of E-beam tester probes and Focused tester probes in testing?	CO1	BTL3	Apply
7.	What is the role of testing in pre-silicon production, post-silicon production and during volume production? Explain various challenges that are faced in each stage.	CO1	BTL3	Apply
8.	Analyze the mixed signal sub circuits available in a common consumer product.	CO1	BTL4	Analyze
9.	With the help of block diagram, explain the application of the mixed signal circuits concept to cellular phone technology?	CO1	BTL4	Analyze
10.	Describe the working of Automatic Test Equipment?	CO1	BTL3	Apply
11.	Discuss the role of Test Engineer in Testing Process?	CO1	BTL3	Apply
12.	What are the common types of Analog and Mixed Signal circuits that is applied in Testing process?	CO1	BTL3	Apply
13.	Explain any one application of Mixed Signal Circuit?	CO1	BTL3	Apply
14.	Why do we test mixed signal devices? Explain in detail.	CO1	BTL4	Analyze
15.	Analyze the engineering principles, trade-offs, and methodology required to transition a mixed-signal device from characterization to high-volume production testing.	CO1	BTL4	Analyze
16.	Assume that a test program runs on a tester that costs the company 3 cents per second to operate. This test cost includes tester depreciation, handler depreciation, electricity, floor space, personnel, and so on. How much money can be saved per year by reducing a 5-s test program to 3.5 s, assuming that 5 million devices per year are to be shipped. Assume that only 90% of devices tested are good and that the average time to find a bad device drops to 0.5 s.	CO1	BTL4	Analyze
17.	Assume that the profit margin on the device is 20% (i.e., for each \$1 worth of devices shipped to the customer, the company makes a profit of 20 cents). How many dollars worth of product would have to be shipped to make a profit equal to the savings offered by the streamlined test program? If each device sells for \$1.80, how many devices does this represent? What obvious conclusion can we draw about the importance of test time reduction versus the importance of selling and shipping additional devices?	CO1	BTL4	Analyze

UNIT II – MEASUREMENTS

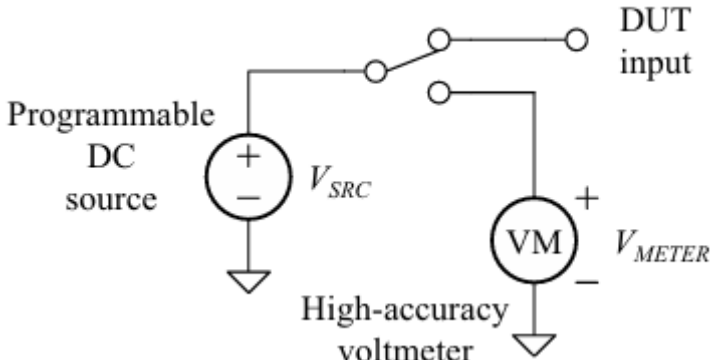
Measurement Terminology - Repeatability, Bias, and Accuracy - Calibrations and Checkers - Tester Specifications - Reducing Measurement Error with Greater Measurement Time – Guard bands - Effects of Measurement Variability on Test Yield - Effects of Reproducibility and Process Variation on Yield - Statistical Process Control.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	State the three major steps of IC manufacturing process?	CO2	BTL1	Remember
2.	Define the term "yield" in semiconductor manufacturing.	CO2	BTL1	Remember
3.	How is yield calculated in each lot of material?	CO2	BTL1	Remember
4.	Differentiate accuracy and precision of measurements.	CO2	BTL1	Remember
5.	In a mixed signal testing procedure, if 15,000 devices are tested with a yield of 63%, how many devices passed the test?	CO2	BTL1	Remember
6.	Calculate the yield percentage if 10,000 parts are tested and only 7000 devices pass all tests?	CO2	BTL1	Remember
7.	Explain the concept of Defect Level (DL) in semiconductor testing?	CO2	BTL2	Understand
8.	Define Bias error	CO2	BTL2	Understand
9.	What are Random errors?	CO2	BTL2	Understand
10.	Explain about quantization error?	CO2	BTL2	Understand
11.	Define the term repeatability in context of measurement	CO2	BTL2	Understand
12.	A 5-mV signal is measured with a meter 10 times, resulting in the following sequence of readings: 5 mV, 6 mV, 9 mV, 8 mV, 4 mV, 7 mV, 5 mV, 7 mV, 8 mV, 11 mV. What is the average measured value? What is the systematic error?	CO2	BTL1	Remember
13.	Describe the ways to improve measurement accuracy?	CO2	BTL1	Remember
14.	If 20,000 devices are tested with a yield of 98%, how many devices failed the test?	CO2	BTL1	Remember
15.	A 55-mV signal is measured with a meter 10 times, resulting in the following sequence of readings: 57 mV, 60 mV, 49 mV, 58 mV, 54 mV, 57 mV, 55 mV, 57 mV, 48 mV, 61 mV. What is the average measured value? What is the systematic error?	CO2	BTL1	Remember
16.	A new product was launched with 100,000 sales over a one-year time span. During this time, seven devices were returned to the manufacturer even though an extensive test screening procedure was in place. What is the defect level associated with this testing procedure in parts per million?	CO2	BTL1	Remember
17.	Define the term reproducibility.	CO2	BTL1	Remember
18.	How do you mathematically express the accuracy of a measurement system?	CO2	BTL2	Understand
19.	Discuss on Focused Calibration?	CO2	BTL2	Understand
20.	Why do standard automated tester specifications often fail to reflect the true variance in consecutive measurements of the same device?	CO2	BTL1	Remember
21.	Write the expression for averaging in measurements?	CO2	BTL2	Understand
22.	Sketch the Probability density plot for measurement result between two test limits.	CO2	BTL2	Understand
23.	What is meant by Statistical Process Control	CO2	BTL1	Remember
24.	State the objective of statistical process control	CO2	BTL2	Understand

PART – B

1.	Explain in detail about the hardware and software calibration methods.	CO2	BTL4	Analyze
2.	Write short notes on the following (i) Guard bands (ii) Tester Specifications	CO2	BTL3	Apply

	(iii) Statistical Process Control			
3.	Explain in detail about the mixed signal IC test and measurement terminologies	CO2	BTL3	Apply
4.	Explain the guard banding technique with detailed examples and illustrations.	CO2	BTL4	Analyze
5.	Illustrate the six sigma based statistical process control techniques with appropriate mathematical analysis.	CO2	BTL4	Analyze
6.	Discuss in detail about the effects of measurement variability on Test yield	CO2	BTL3	Apply
7.	Describe the various measurement terminologies in mixed signal testing.	CO2	BTL3	Apply
8.	A meter is rated at 8-bits and has a full-scale range of ± 5 V. What is the measurement uncertainty of this meter, assuming only quantization errors from an ideal meter ADC?	CO2	BTL3	Apply
9.	A signal is to be measured with a maximum uncertainty of ± 0.5 μ V. How many bits of resolution are required by an ideal meter having a ± 1 V full-scale range?	CO2	BTL3	Apply
10.	Applying mathematical expressions, describe repeatability, bias and accuracy.	CO2	BTL3	Apply
11.	Describe the tester specifications and apply it to a fictitious DC meter	CO2	BTL3	Apply
12.	A measurement of a 1-V reference level is made 100 times, where the minimum reading is 0.95 V and the maximum reading is 1.14 V. What is the absolute accuracy of these measurements? What is the relative accuracy with respect to a full-scale value of 5 V?	CO2	BTL4	Analyze
13.	Explain the process of Reducing Measurement Error with Greater Measurement Time	CO2	BTL3	Apply
14.	A particular test program performs 857 tests, most of which cause little or no yield loss. Five measurements account for most of the yield loss. Using a lot summary and a continue-on-fail test process, the yield loss due to each measurement is found to be: Test #1: 1%, Test #2: 5%, Test #3: 2.3%, Test #4: 7%, Test #5: 1.5% All other tests combined 0.5% What is the overall yield of this lot of material?	CO2	BTL4	Analyze
15.	Describe the process of calibrations and checkers in measurements.	CO2	BTL4	Analyze
16.	Discuss in detail about the effects of Reproducibility and Process Variation on Yield	CO2	BTL4	Analyze
17.	A 2.500-V signal is required from a DC source as shown in Figure. Describe a calibration procedure that can be used to ensure that $2.500 \text{ V} \pm 500 \mu\text{V}$ does indeed appear at the output of the DC source. 	CO2	BTL4	Analyze

UNIT III – DAC TESTING

Basics of Data Converters -Principles of DAC and ADC, Data Formats, Comparison of DAC and ADC, DAC Failure Mechanisms.

Basic DC Tests - Transfer Curve Tests - Dynamic DAC Tests - Tests for Common DAC Applications.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	List the types of DAC architectures.	CO3	BTL1	Remember
2.	List the various data encoding formats of DACs	CO3	BTL1	Remember
3.	How the absolute error curve of DAC is calculated?	CO3	BTL1	Remember
4.	A 4-bit DAC has a full-scale range of 0 to 5V. What is the gain of this DAC?	CO3	BTL1	Remember
5.	Write the equation for data format in binary number?	CO3	BTL1	Remember
6.	Sketch the DAC code-to-voltage transfer curve	CO3	BTL1	Remember
7.	Mention the expression for gain of a DAC?	CO3	BTL2	Understand
8.	A 3-bit ADC has a full-scale voltage range of 0 to 5.0 V. What is the gain of this ADC if its internal operation is based on rounding?	CO3	BTL2	Understand
9.	A 10-bit ADC has a full-scale voltage range of 5.0 to 5.0 V. What is the LSB step size if its internal operation is based on truncation?	CO3	BTL2	Understand
10.	Sketch the Symbol for D -bit Digital to Analog converter	CO3	BTL2	Understand
11.	What is intrinsic parameters of DAC	CO3	BTL2	Understand
12.	Draw the ADC voltage-to-code transfer curve	CO3	BTL1	Remember
13.	What do you mean by transfer curve test in DAC?	CO3	BTL1	Remember
14.	Name the converter specific tests which measures the overall quality of the DACs code to voltage transfer curve.	CO3	BTL1	Remember
15.	Elaborately discuss about the conversion time and Glitch Energy performance parameters of Dynamic DAC testing	CO3	BTL1	Remember
16.	Discuss in detail about the test measurements of DACs used in DC reference and Video Signal generator applications.	CO3	BTL1	Remember
17.	Describe the dynamic DAC Test parameters with appropriate examples	CO3	BTL1	Remember
18.	What is INL and DNL?	CO3	BTL2	Understand
19.	Define Settling time in DAC.	CO3	BTL2	Understand
20.	What is monotonicity?	CO3	BTL1	Remember
21.	What is meant by overshoot?	CO3	BTL2	Understand
22.	Define Rise time?	CO3	BTL2	Understand
23.	State about the full-scale range of DAC	CO3	BTL1	Remember
24.	Write the expression or best fit line of DAC.	CO3	BTL2	Understand

PART – B

1.	Explain the principle of DAC and ADC Conversion	CO3	BTL4	Analyze
2.	Discuss the data formats engaged in DACs?	CO3	BTL3	Apply
3.	A 10-bit DAC has a full-scale voltage range of 5.0 to 5.0 V. What is the LSB step size?	CO3	BTL3	Apply
4.	A 4-bit DAC has a full-scale voltage range of 0 to 1.0 V. The input is formatted using an unsigned binary number representation. List all possible ideal output levels. What output level corresponds to the DAC input code 0?	CO3	BTL4	Analyze
5.	The output levels of a 4-bit DAC produces the following set of voltage levels, starting from code 0 and progressing through to code 15: 0.0465, 0.3255, 0.7166, 1.0422, 1.5298, 1.8236, 2.1693, 2.5637, 2.8727, 3.3443, 3.6416, 4.0480, 4.3929, 4.7059, 5.0968, 5.5050	CO3	BTL4	Analyze

	What is the full-scale range of this DAC?			
6.	A 4-bit DAC has a full-scale voltage range of 0 to 5 V. The input is formatted using an unsigned binary number representation. List all possible ideal output levels. What output level corresponds to the DAC input code 0? What is the VLSB?	CO3	BTL4	Analyze
7.	Compare and contrast the DAC and ADC.	CO3	BTL4	Analyze
8.	Elaborate on DAC failure mechanism.	CO3	BTL3	Apply
9.	Explain the various parameters of the Basic DC test of DAC	CO3	BTL3	Apply
10.	Elaborately discuss about the Dynamic DAC Test and its parameters.	CO3	BTL3	Apply
11.	Describe the different figures of merit of a DAC by applying Transfer Curve Tests.	CO3	BTL3	Apply
12.	Explain in detail about the test mechanisms of DACs used in DC references and Audio reconstruction	CO3	BTL3	Apply
13.	Explain the DAC test mechanisms as applied to Data Modulation and Video Signal Generator?	CO3	BTL3	Apply
14.	A 4-bit unsigned binary DAC produces the following set of voltage levels, starting from code 0 and progressing through to code 15 0.0465, 0.3255, 0.7166, 1.0422, 1.5298, 1.8236, 2.1693, 2.5637, 2.8727, 3.3443, 3.6416, 4.0480, 4.3929, 4.7059, 5.0968, 5.5050 The ideal DAC output at code 0 is 0 V and the ideal gain is equal to 400 mV/bit. Answer the following questions assuming an endpoint-to-endpoint line is used as a reference. (a) Calculate the DAC's gain (volts per bit), gain error, offset and offset error. (b) What is the LSB step size? (c) Calculate the absolute error transfer curve for this DAC. Normalize the result to one LSB. (d) Is the DAC output monotonic?	CO3	BTL3	Apply
15.	Illustrate how the Conversion time and Glitch Energy performance parameters affect the DAC dynamic Test?	CO3	BTL4	Analyze
16.	Analyze the role of monotonicity, INL and DNL in DAC testing and how they affect system performance.	CO3	BTL4	Analyze
17.	Calculate the DNL curve for a 4-bit DAC whose INL curve is described by the following values 0.1994, 0.1180, 0.0177, 0.1310, 0.1253, 0.1036, 0.0272, 0.0089, 0.1039, 0.0096, 0.1537, 0.0565, 0.1077, 0.1196, 0.0490, 0.0429 Does this DAC pass a $\pm 1/2$ LSB specification for DNL?	CO3	BTL4	Analyze

UNIT IV – ADC TESTING

ADC Testing Versus DAC Testing - ADC Code Edge Measurements - Edge Code Testing Versus Center Code Testing, Step Search and Binary Search Methods, Servo Method, Linear Ramp Histogram Method, Histograms to Code Edge Transfer Curves, Rising Ramps Versus Falling Ramps, Sinusoidal Histogram Method - DC Tests and Transfer Curve Tests - Dynamic ADC Tests - Tests for Common ADC Applications.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	What is the primary difference between DAC and ADC testing.	CO4	BTL1	Remember
2.	Mention the limitations of Center Code Testing method of ADC testing.	CO4	BTL1	Remember
3.	State the advantages of servo method-based ADC code Edge Measurements.	CO4	BTL1	Remember
4.	What is code edge measurement in ADC testing?	CO4	BTL1	Remember
5.	How are histograms used in code edge transfer curves?	CO4	BTL1	Remember
6.	What is a transfer curve test?	CO4	BTL1	Remember
7.	What is the significance of histogram analysis in ADC testing?	CO4	BTL2	Understand
8.	Why is a sinusoidal input preferred in histogram – based ADC testing?	CO4	BTL2	Understand
9.	Name two static parameters obtained from ADC transfer curve.	CO4	BTL2	Understand
10.	Compare edge code testing and center code testing in ADC characteristics?	CO4	BTL2	Understand
11.	What do you infer from Aperture Jitter?	CO4	BTL2	Understand
12.	What is the servo method in ADC testing?	CO4	BTL1	Remember
13.	What is INL and DNL in ADC testing?	CO4	BTL1	Remember
14.	What is DC offset in ADC testing?	CO4	BTL1	Remember
15.	Sketch the ADC model with input noise?	CO4	BTL1	Remember
16.	If V is normally distributed with zero mean and a standard deviation of 2 mV, find $P(V < 4 \text{ mV})$?	CO4	BTL2	Understand
17.	If V is normally distributed with zero mean and a standard deviation of 100 mV, what is the value of V_{IN} such that $P(V < V_{IN}) = 0.9641$?	CO4	BTL2	Understand
18.	What is center code testing?	CO4	BTL1	Remember
19.	What is edge code testing?	CO4	BTL1	Remember
20.	Draw the block diagram of ADC servo test setup.	CO4	BTL1	Remember
21.	What are the types of linear histogram inputs?	CO4	BTL2	Understand
22.	Sketch the Up ramp, Down ramp and triangle waveform used as input in linear histogram?	CO4	BTL2	Understand
23.	Point out the advantages of sinusoidal histogram method?	CO4	BTL1	Remember
24.	What is Sparkling in a linear ramp histogram?	CO4	BTL2	Understand

PART – B

1.	Explain in detail about the Linear Ramp Histogram Method of ADC testing?	CO4	BTL4	Analyze
2.	Discuss the performances of DC Tests and Transfer Curve Tests of ADC with appropriate illustrations.	CO4	BTL3	Apply
3.	Perform a detailed performance analysis of Sinusoidal Histogram Method for testing a 4-bit ADC.	CO4	BTL3	Apply
4.	Explain in detail about Sinusoidal Histogram Method of ADC testing with detailed illustrations?	CO4	BTL4	Analyze
5.	Describe in detail about the accuracy limitations of Histogram based ADC testing with appropriate mathematical equations.	CO4	BTL4	Analyze
6.	Explain ADC code edge measurements and their importance in evaluating ADC performance?	CO4	BTL3	Apply

7.	Draw the block diagram of ADC Servo measurement setup and explain in detail	CO4	BTL3	Apply
8.	Describe the tests for common ADC applications like audio and video?	CO4	BTL3	Apply
9.	Compare rising ramps versus falling ramps in ADC testing	CO4	BTL3	Apply
10.	Describe the step search and binary search methods for ADC code edge measurements.	CO4	BTL3	Apply
11.	The distribution of code hits for an two's complement 4-bit ADC excited by a sinusoidal signal beginning with code -8 is as follows 170, 61, 55, 48, 44, 42, 40, 39, 39, 40, 41, 42, 45, 50, 72, 196 A binary search was performed on the first transition between codes -8 and -7 and found the code edge to be at 330 mV. A second binary search was performed and found the code edge between codes 6 and 7 to be 4.561 V. What is the average LSB size for this 4-bit ADC? What is the mid-level of the ADC input? What is the offset and amplitude of the sinusoidal signal seen by the ADC relative to its mid-level? What is expected or ideal sinusoidal distribution of code hits corresponding to this input signal? Determine the width of each code, as well as the code edges (all in volts). Plot the transfer characteristics of this ADC	CO4	BTL3	Apply
12.	Elaborate on sinusoidal histogram method of ADC testing?	CO4	BTL3	Apply
13.	Describe the DC tests and Transfer curve test for an ADC?	CO4	BTL4	Analyze
14.	A linear histogram test was performed on an unsigned 4-bit ADC resulting in the following distribution of code hits beginning with code 0: 4, 5, 5, 7, 8, 4, 2, 4, 4, 3, 6, 3, 4, 6, 5, 9. Determine the best-fit DNL and INL characteristics of this ADC?	CO4	BTL4	Analyze
15.	Discuss the concept of Dynamic ADC tests with necessary diagrams.	CO4	BTL4	Analyze
16.	A sinusoidal histogram test was performed on an unsigned binary 4-bit ADC, resulting in the following distribution of code hits beginning with code 0: 137, 81, 60, 52, 47, 44, 43, 42, 42, 42, 44, 46, 50, 57, 72, 166 A binary search was performed on the first transition between codes 0 and 1 and found the code edge to be at 14 mV. A second binary search was performed and found the code edge between codes 14 and 15 to be 0.95 V. What is the average LSB size for this 4-bit ADC? Determine the width of each code, in volts. Also, determine the location of the code edges. Plot the transfer curve for this ADC.	CO4	BTL4	Analyze
17.	Compare ADC testing with DAC testing, highlighting key differences in methodology and objectives.	CO4	BTL4	Analyze

UNIT V – CLOCK AND SERIAL DATA COMMUNICATIONS CHANNEL MEASUREMENT

Synchronous and Asynchronous Communications - Time-Domain Attributes of a Clock Signal - Frequency-Domain Attributes of a Clock Signal - Communicating Serially Over a Channel - Bit Error Rate Measurement - Methods to Speed Up BER Tests in Production - Deterministic Jitter Decomposition - Jitter Transmission Tests.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	What are the sources of deterministic jitter?	CO5	BTL1	Remember
2.	Give the importance of BER tests for serial data link analysis	CO5	BTL1	Remember
3.	Draw the power spectral density plot of a jittered clock signal	CO5	BTL1	Remember
4.	State functionality of Amplitude based scan test.	CO5	BTL1	Remember
5.	Define BER	CO5	BTL1	Remember
6.	What is Time based scan test	CO5	BTL1	Remember
7.	Compare synchronous and asynchronous mode of transmission	CO5	BTL2	Understand
8.	What is the disadvantage of dual – Dirac jitter composition method?	CO5	BTL2	Understand
9.	Why do we go for Gaussian Mixture Jitter decomposition method?	CO5	BTL2	Understand
10.	Define Period Jitter (PJ) of a serial Communication link?	CO5	BTL2	Understand
11.	A time jitter sequence is described by $J[n] = 0.001 \sin^2(14\pi/1024n) + 0.001$ for $n = 0, 1, \dots, 1023$. Determine the standard deviation.	CO5	BTL2	Understand
12.	Draw a chart illustrating different components of jitter?	CO5	BTL1	Remember
13.	Sketch the general jitter tolerance test setup illustrating the different source conditions	CO5	BTL1	Remember
14.	Give a flowchart of test process for performing an efficient BER test	CO5	BTL1	Remember
15.	What is the use of LFSR?	CO5	BTL1	Remember
16.	Write the generator polynomial for LFSR with degree 8?	CO5	BTL1	Remember
17.	Expand PRBS?	CO5	BTL1	Remember
18.	Write the schematic diagram of 4 stage linear feedback shift register?	CO5	BTL2	Understand
19.	Mention any 2 methods to speed up BER tests in production?	CO5	BTL2	Understand
20.	What is Data – dependent Jitter?	CO5	BTL1	Remember
21.	What did you infer from Bounded and uncorrelated Jitter?	CO5	BTL2	Understand
22.	A time jitter sequence is described by $J[n] = 0.001 \sin^2(14\pi/1024n) + 0.001$ for $n = 0, 1, \dots, 1023$. Calculate the mean	CO5	BTL2	Understand
23.	List the types of jitter?	CO5	BTL1	Remember
24.	Illustrate the asynchronous data communication link involving two D-type registers with a block diagram,	CO5	BTL2	Understand

PART – B

1.	Illustrate the time domain attributes of a clock signal with appropriate mathematical expressions.	CO5	BTL4	Analyze
2.	Explain in detail about the frequency domain attributes of a clock signal with neat diagrams	CO5	BTL3	Apply
3.	Write Short notes on (i) BER Measurement (ii) Jitter Decomposition	CO5	BTL3	Apply
4.	Explain in detail about the analysis of clock signals based on Jitter Transmission Tests?	CO5	BTL3	Apply
5.	Explain in detail about the synchronous and asynchronous data communication with neat diagrams.	CO5	BTL3	Apply
6.	Elaborate the Bit error rate measurement in a communication system?	CO5	BTL4	Analyze
7.	With the help of a flow chart, illustrate the test process for performing an efficient BER test?	CO5	BTL3	Apply

8.	A system transmission test is to be run whereby a BER < 10 ⁻¹⁰ is to be verified at a confidence level of 99% when 2 or less bit errors are deemed acceptable. What are the minimum and maximum bit lengths required for this test? Also what is the minimum and maximum time for this test if the data rate is 2.5 Gbps? Does testing for a fail part prior to the end of the test provide significant test time savings?	CO5	BTL3	Apply										
9.	With the help of block diagram, describe PRBS generation?	CO5	BTL4	Analyze										
10.	Derive the first 15 bits associated with the four-stage LFSR shown in Figure, assuming that the shift register is initialized with seed 1011 (from left to right)	CO5	BTL3	Apply										
11.	Describe the methods to speed up BER tests in production?	CO5	BTL3	Apply										
12.	Discuss on amplitude based scan test for BER analysis	CO5	BTL3	Apply										
13.	Explain the Time based Scan test in the context of BER analysis?	CO5	BTL4	Analyze										
14.	Elaborate the Deterministic Jitter decomposition with the appropriate mathematical expressions.	CO5	BTL4	Analyze										
15.	Explain the Jitter transmission test with necessary diagrams	CO5	BTL4	Analyze										
16.	A system transmission test is to be run whereby a BER < 10 ⁻¹² is to be verified using the amplitude based scan test method. The following BER measurements were made at the following four threshold levels: <table><thead><tr><th>Voltage Threshold Levels</th><th>BER Measurement</th></tr></thead><tbody><tr><td>0.70</td><td>0.5 x 10⁻⁶</td></tr><tr><td>0.90</td><td>0.5 x 10⁻⁹</td></tr><tr><td>1.20</td><td>0.5 x 10⁻⁹</td></tr><tr><td>1.35</td><td>0.5 x 10⁻⁶</td></tr></tbody></table> Does this system have the capability to meet the BER requirements and what is the optimum threshold level? Assume that the noise is asymmetrical.	Voltage Threshold Levels	BER Measurement	0.70	0.5 x 10 ⁻⁶	0.90	0.5 x 10 ⁻⁹	1.20	0.5 x 10 ⁻⁹	1.35	0.5 x 10 ⁻⁶	CO5	BTL4	Analyze
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17.	An LFSR of degree 8 is required. Write a short routine that generates the complete set of unique bits associated with this sequence. Initialize the LSFR using the seed 00000001, where the first bit corresponds to the state of the 7th flip-flop and the last bit is associated with the state of the 0th flip-flop.	CO5	BTL4	Analyze										