

# **SRM VALLIAMMAI ENGINEERING COLLEGE**

**(An Autonomous Institution)**  
SRM Nagar, Kattankulathur – 603 203

**DEPARTMENT OF**  
**ELECTRONICS AND COMMUNICATION ENGINEERING**

**QUESTION BANK**



**IV SEMESTER**

**1906401 – LINEAR INTEGRATED CIRCUITS**

**(Common to Medical Electronics)**

**Regulation – 2019**

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*Prepared by*

**Ms. V.P.Sandhya, Assistant Professor**

**Mr.S.Senthilmurugan, Assistant Professor**

**Ms.S.Abirami, Assistant Professor**

**Dr.S.Ramesh, Associate Professor**

1906401-LIC/IV SEM/21-22 EVEN SEM



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## QUESTION BANK

SUBJECT : 1906401 - LINEAR INTEGRATED CIRCUITS

SEMESTER/YEAR : IV /II

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Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, Op-Amp parameters & Measurement, Input & Out put Off set voltages & currents, slew rate, Open and closed loop configurations – JFET Operational Amplifiers – LF155 and TL082.

### PART – A

Q. No	Questions	BT Level	Competence
1.	Mention the importance of offset voltage of an operational amplifier.	BTL 1	Remembering
2.	Define CMRR.	BTL 1	Remembering
3.	Write down the requirements to be met for a good current source.	BTL 2	Understanding
4.	List the advantages of integrated circuits over discrete component circuit.	BTL 1	Remembering
5.	What is an operational amplifier?	BTL 1	Remembering
6.	How do you make a current mirror with magnification?	BTL 1	Remembering
7.	Define slew rate and what causes the slew rate?	BTL 1	Remembering
8.	State the classes of op-amp IC 741.	BTL 2	Understanding
9.	Why do we use $R_{comp}$ resistor?	BTL 2	Understanding
10.	Draw the op-amp symbol and state its important terminals.	BTL 2	Understanding
11.	Formulate the ideal value of Power supply rejection ratio (PSRR)?	BTL 3	Applying
12.	An op-amp has a gain of twelve million. Express this gain in dB.	BTL 3	Applying
13.	Why $R_E$ cannot be selected very high for practical cases?	BTL 3	Applying
14.	One differential amplifier has CMRR of 100db and other has CMRR of 40db. Which you will prefer and why?	BTL 4	Analyzing
15.	In what way 741S is better than 741?	BTL 4	Analyzing
16.	An op-amp in open loop is not used for most of the applications. Justify	BTL 4	Analyzing
17.	Brief the necessity of active loads preferred than passive loads in the input stage of an operational amplifier.	BTL 5	Evaluating
18.	IC741 op-amp not used for high frequency applications- Justify.	BTL 5	Evaluating
19.	Calculate the maximum distorted amplitude that a sine wave input of 10 kHz, can produce at the output of an op-amp whose slew-rate is 0.5v/ $\mu$ sec.	BTL 6	Creating
20.	A Differential amplifier has a differential voltage gain of 2000 and common mode gain of 0.2. Determine CMRR.	BTL 6	Creating

<b>PART – B</b>				
1.	Define and explain slew rate. Derive its equation. Also explain method adapted to improving slew rate.	(13)	BTL 1	Remembering
2.	(i) Write down the characteristics and their respective values of an ideal Operational amplifier. (ii) Use appropriate block diagram and explain the general stages of an Op-Amp IC.	(6) (7)	BTL 1	Remembering
3.	What is a current mirror? Give the current mirror circuit analysis.	(13)	BTL 4	Analyzing
4.	Draw the circuit of Widlar current source and derive an expression for its output current?	(13)	BTL 2	Understanding
5.	With the help of a neat circuit diagram, discuss the construction and working of Wilson current source?	(13)	BTL 2	Understanding
6.	With neat circuit diagrams, explain the operation of (i) Voltage reference circuit using temperature compensation (ii) Voltage reference circuit using avalanche diode reference	(6) (7)	BTL 2	Understanding
7.	List and explain the DC characteristics of an operational amplifier	(13)	BTL 1	Remembering
8.	Compare the ideal and practical characteristics of IC741	(13)	BTL 4	Analyzing
9.	Determine the output voltage of a differential amplifier for the input voltages of $300\mu\text{V}$ and $240\mu\text{V}$ . The differential gain of the amplifier is 5000 and the value of the CMRR is (i) 100 (ii) $10^5$	(6) (7)	BTL 3	Applying
10.	An Op-amp has a differential gain of 80dB and CMRR of 95dB. If $V_1 = 2\mu\text{V}$ and $V_2 = 1.6\mu\text{V}$ , then calculate the (i) Differential mode output values. (ii) Common mode output values.	(6) (7)	BTL 4	Analyzing
11.	Construct the BJT differential amplifier with active load and explain its operating principle.	(13)	BTL 6	Creating
12.	(i) In response to a square wave input, the output of an op amp changed from -3V to +3V over a time interval of $0.25\mu\text{s}$ . Determine the slew rate of the op amp. (ii) Assuming a slew rate for 741 IC is $0.5\text{V}/\mu\text{s}$ . What is the maximum undistorted sine wave that can be obtained for 12V peak?	(6) (7)	BTL 5	Evaluating
13.	Write note on LF155 JFET input operational amplifier and TL082 wide bandwidth dual JFET input operational amplifier with necessary diagram.	(13)	BTL 1	Remembering
14.	From the equivalent circuit of practical op-amp, obtain the expression for open loop voltage gain	(13)	BTL 3	Applying
<b>PART – C</b>				
1.	Derive the transfer characteristics of dual input differential amplifier	(15)		

	showing the linear and limiting regions. Comment on the same.		BTL 5	Evaluating
2.	(i) A square wave peak-to-peak amplitude of 750mV has to be amplified to a peak-to-peak amplitude of 3.8V, with rise time of 4.5 $\mu$ s or less. Can IC741 be used? (ii) For an operational amplifier having a slew rate of 3V/ $\mu$ Sec. What is the maximum closed loop voltage gain that can be used when the input signal varies by 0.4V in 12 $\mu$ Sec.	(10) (5)	BTL 6	Creating
3.	Construct a Widlar Current Source with a reference current of 1mA and RE as 5K $\Omega$ . Determine the approximate value of IC <sub>2</sub> neglecting the base currents.	(15)	BTL 6	Creating
4.	(i) For a typical op – amp, IC <sub>Q</sub> = 15 $\mu$ A and C = 35pF. The peak value of input is 12V. Determine slew rate and maximum possible frequency of input voltage that can be applied to get undistorted Output. (ii) An Op-amp has 7kHz sine wave input signal. Find the largest amplitude that the output of the amplifier can have without distortion with IC <sub>Q</sub> of 8 $\mu$ A and C <sub>c</sub> of 27pF.	(8) (7)	BTL 5	Evaluating

## UNIT II APPLICATIONS OF OPERATIONAL AMPLIFIERS

**Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, AC amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.**

### PART – A

Q. No	Questions	BT Level	Competence
1.	Mention two linear and two non-linear applications performed by an operational amplifier	BTL 2	Understanding
2.	Write the two realistic simplifying assumptions used for op-amp.	BTL 2	Understanding
3.	Define about sign changer.	BTL 2	Understanding
4.	How to obtain the average circuit from an inverting summer?	BTL 1	Remembering
5.	Compare the inverting and non-inverting operational amplifier configurations.	BTL 4	Analyzing
6.	Give the applications of inverting & non- inverting amplifiers.	BTL 1	Remembering
7.	Identify the operating voltage range of IC 741?	BTL 3	Applying
8.	Outline any four applications of Instrumentation amplifier.	BTL 2	Understanding
9.	Assess the need for converting a first order filter into a second order filter.	BTL 5	Evaluating
10.	What is the function of a Phase shift circuit?	BTL 1	Remembering
11.	Point out the need for converting a first order filter into a second order filter.	BTL 1	Remembering
12.	Sketch the Op-amp integrator & differentiator circuit with necessary equation.	BTL 3	Applying
13.	State the errors in an ideal integrator?	BTL 1	Remembering
14.	List any five characteristics of comparator.	BTL 1	Remembering
15.	Construct an adder circuit using op-amp to get the output expression as $V_o = - (0.1 V_1 + V_2 + 5 V_3)$	BTL 3	Applying

16.	An a.c signal has got a magnitude of 0.1V peak to peak. Suggest a suitable half wave rectifier for this signal.	BTL 4	Analyzing
17.	Why active guard drive is necessary in an instrumentation amplifier?	BTL 4	Analyzing
18.	Find the output voltage of the following circuit. Given $R_1 = R_2 = 10k\Omega$ and $R_f = 100$	BTL 6	Creating
19.	Differentiate precision rectifier from the conventional rectifier.	BTL 5	Evaluating
20.	Draw a inverting AC amplifier circuit.	BTL 6	Creating
<b>PART – B</b>			
1.	With a suitable circuit diagram, explain the operating principle of an instrumentation amplifier and derive its gain.	(13)	BTL 2 Understanding
2.	Construct the circuit diagram of Adder, Subtractor, and Averaging circuit using op-amp with circuit analysis.	(13)	BTL 4 Analyzing
3.	Write the operation of Current to Voltage and Voltage to current converter circuits.	(13)	BTL 1 Remembering
4.	Describe the working of Full wave Precision Rectifier in detail. Draw the waveforms associate with it.	(13)	BTL 1 Remembering
5.	Derive the expression for log computation using op-amp and explain necessary circuit diagram.	(13)	BTL 5 Evaluating
6.	(i)With neat figures describe the working of an integrator using op-amp. (ii) Derive the expression for output voltage of an practical integrator.	(7) (6)	BTL 1 Remembering
7.	Explain the working of clipper and clamper circuits using Op amp?	(13)	BTL 1 Remembering
8.	Design a second order low pass filter using operational amplifier for the upper cut off frequency of 2.5kHz. Assume the value of capacitor to be 0.1 $\mu$ F	(13)	BTL 6 Creating
9.	(i)Discuss the working of an differentiator using op-amp. (ii) List out the errors in ideal differentiator and analyse the practical differentiator for those error.	(6) (7)	BTL3 Applying
10.	For the non-inverting op amp shown in figure, find the output voltage $V_o$	(13)	BTL 3 Applying

11.	Define Schmitt Trigger and explain about the working of inverting and non inverting Schmitt trigger in detail.	(13)	BTL 2	Understanding
12.	How did the analog computations are performed using IC-741. Explain using circuits and necessary equations.	(13)	BTL 5	Evaluating
13.	(i) Analyse the first order Low pass Butterworth filter and derive its voltage gain. (ii) Write the design steps for first order Low pass Butterworth filter	(10) (3)	BTL 4	Analyzing
14.	Elaborate about the working of (i) AC amplifier (ii) Comparator	(7) (6)	BTL 2	Understanding
<b>PART – C</b>				
1.	Design an instrumentation amplifier whose gain can be varied continuously over the range $1 \leq A \leq 1000$ . Assume all other relevant details.	(15)	BTL 6	Creating
2.	Design a differentiator using Op-Amp to differentiate an input signal with $f_{\max} = 150$ Hz	(15)	BTL 5	Evaluating
3.	Design a second order low pass butterworth filter having high cut off frequency of 1kHz. Draw its frequency response.	(15)	BTL 6	Creating
4.	Design a practical integrator circuit with a d.c. gain of 10, to integrate a square wave of 10kHz.	(15)	BTL 5	Evaluating

### UNIT III ANALOG MULTIPLIER AND PLL

**Analog Multiplier using Emitter Coupled Transistor Pair Gilbert Multiplier cell – Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing, Clock synchronization**

#### PART A

Q. No	Questions	BT Level	Competence
1.	Name the two applications of PLL.	BTL 1	Remembering
2.	Define capture range and lock range of PLL.	BTL 1	Remembering
3.	What is Pull-in time?	BTL 1	Remembering

4.	For perfect lock, what should be the phase relation between the incoming signal and VCO output signal?		BTL 4	Analyzing
5.	Mention the classification of phase detector. Write about switch type phase detector.		BTL 2	Understanding
6.	List the problems associated with switch type phase detector.		BTL 1	Remembering
7.	Why VCO is also called as V to F converter?		BTL 1	Remembering
8.	On what parameters does the free running frequency of VCO depend on?		BTL 3	Applying
9.	Outline the need for frequency synthesizer.		BTL 2	Understanding
10.	Interpret the relation between capture ranges and lock range in a PLL.		BTL 2	Understanding
11.	Write the purpose of having a low pass filter in PLL.		BTL 3	Applying
12.	Discuss the effect of having large capture range.		BTL 6	Creating
13.	Assess the features of IC 566 VCO.		BTL 5	Evaluating
14.	Which parameter decides the pull-in time?		BTL 1	Remembering
15.	Identify the merits of companding.		BTL 3	Applying
16.	Give the applications of OTA.		BTL 1	Remembering
17.	Justify the need of pre-distortion circuits in Gilbert analog multiplier.		BTL 5	Evaluating
18.	Analyze the necessity of modulation.		BTL 4	Analyzing
19.	Construct the circuit of AM detector using PLL.		BTL 6	Creating
20.	Distinguish the advantages & disadvantages of monolithic PLLs over discrete PLLs.		BTL 4	Analyzing
<b>PART – B</b>				
1.	How would you describe the block diagram of PLL and derive the expression for Lock range and capture range.	(13)	BTL 1	Remembering
2.	Illustrate the operation of VCO with neat block diagram. Also derive an expression for $f_0$ .	(13)	BTL 2	Understanding
3.	(i) Analyze the Gilbert's four quadrant multiplier cell with a neat circuit diagram. (ii) Identify how a frequency doubler can be realized using this cell.	(8) (5)	BTL 4 BTL 3	Analyzing Applying
4.	Discuss any three applications of PLL in detail.	(13)	BTL 6	Creating
5.	Explain the purpose and functioning of (i) Frequency division circuit using PLL IC565 (ii) Frequency synthesizer.	(7) (6)	BTL 2	Understanding
6.	(i) Estimate the working principle of operational Transconductance Amplifier(OTA). (ii) List the applications of VCO for FM generation.	(8) (5)	BTL 1	Remembering
7.	(i) Define capture range and lock range. (ii) Elaborate the process of capturing the lock and also derive for capture range and lock range.	(3) (10)	BTL 1	Remembering
8.	(i) How would you explain the working of a VCO? (ii) Derive the expression for voltage to frequency conversion factor.	(6) (7)	BTL 1	Remembering
9.	Determine the change in DC control voltage $V_c$ during lock, if input signal frequency $f_s = 20$ KHz, the free running frequency is 21 KHz and the V/F transfer coefficient of VCO is 4 KHz.	(13)	BTL 5	Evaluating

10.	(i) Examine the multiplier cell using emitter-coupled transistor pair. (ii) Illustrate that the output voltage is proportional to the product of the two input voltages and state their limitations.	(8) (5)	BTL 4	Analyzing
11.	A PLL IC565 connected as an FM demodulator has $R_1 = 10K$ , $C_1 = 0.01 \mu F$ and $c = 0.4 \mu F$ . The supply voltage is +12V. Determine the Free running Frequency, Lock range and capture range.	(13)	BTL 3	Applying
12.	Discuss the following applications of Analog Multiplier ICs (i) Voltage squarer and Voltage divider (ii) Square rooter and Phase angle detector	(7) (6)	BTL 2	Understanding
13.	(i) Summarize the basic analog multiplication techniques. (ii) Develop the expression for free running frequency of voltage controlled oscillator.	(7) (6)	BTL 4 BTL 3	Analyzing Applying
14.	Illustrate the closed loop analysis of PLL with necessary diagrams	(13)	BTL 4	Analyzing
<b>PART – C</b>				
1.	(i) For PLL 565, given the free-running frequency as 100KHz, the demodulation capacitor of $2\mu f$ and supply voltage is $\pm 6V$ , determine the lock and capture frequencies and identify the component values.  (ii) A PLL has a free running frequency of 300KHz and the bandwidth of the low pass filter is 50KHz. Check whether the loop acquires lock for an input signal of 320KHz.	(8) (7)	BTL 6	Creating
2.	Explain the operation of a variable trans conductance multiplier circuit. Derive the expression for its output voltage.	(15)	BTL 5	Evaluating
3.	(i) The variable Trans conductance Analog multiplier. (ii) Determine the output frequency $f_0$ , lock range $\Delta f_L$ and capture range $\Delta f_c$ of IC 565. Assume $R_1=15K$ $C_1=0.01\mu F$ , $C=1\mu F$ and the supply voltage is +12V.	(5) (10)	BTL 5	Evaluating
4.	Construct the block diagram and explain principle of working, characteristics and applications of: (i) Frequency synthesizer. (ii) Frequency shift keying (FSK) Demodulator.	(8) (7)	BTL 6	Creating

#### UNIT IV ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

**Analog and Digital Data Conversions, D/A converter – specifications weighted resistor type, R2R Ladder type, Voltage Mode and Current Mode R 2R Ladder types switches for D/A converters, high speed sample and hold circuits, A/D Converters – specifications Flash type Successive Approximation type Single Slope type – Dual Slope type A/D Converter using Voltage to Time Conversion Oversampling A/D Converters, Sigma- Delta converters**

#### PART – A

Q. No	Questions	BT Level	Competence
1.	Classify the A/D converters based on their operational features.	BTL 2	Understanding
2.	List the direct type ADCs.	BTL 4	Analyzing



3.	Recall about the function of integrating type converter.	BTL 1	Remembering
4.	Describe the principle of operation of successive Approximation ADC.	BTL 2	Understanding
5.	Mention the main advantages of integrating type ADCs.	BTL 1	Remembering
6.	Define Sampling.	BTL 1	Remembering
7.	Compare the advantages and drawbacks of a dual-slop ADC.	BTL 2	Understanding
8.	Distinguish between conversion time and settling time.	BTL 4	Analyzing
9.	Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values.	BTL 5	Evaluating
10.	Give the advantages of inverted R-2R (current type) ladder D/A converter over R -2R (voltage type) D/A converter?	BTL 1	Remembering
11.	Brief the need for electronic switches in D/A converter and mention the names of the switches used in MOS transistors.	BTL 1	Remembering
12.	What is meant by delta modulation?	BTL 2	Understanding
13.	How would you justify, which type of ADC is the fastest?	BTL 5	Evaluating
14.	Outline the principle of operation of voltage to time conversion.	BTL 1	Remembering
15.	Calculate the values of LSB and MSB for an 8-bit DAC for 0V to 10V range.	BTL 6	Creating
16.	Point out the features of granular error and slope overload error.	BTL 3	Applying
17.	An 8 bit A/D converter accepts an input voltage signal of range 0 to 12v. What is the digital output for an input voltage of 6V?	BTL 3	Applying
18.	Obtain the number of comparators required for realizing a 4-bit flash ADC.	BTL 6	Creating
19.	Compare and contrast the binary weighted and R-2R ladder DAC.	BTL 4	Analyzing
20.	Write the need of sigma and delta converters.	BTL 3	Applying
<b>PART – B</b>			
1.	(i) How would you categorize A/D converters? (ii) Discuss the working principle of successive approximation type ADC.	(6) (7)	BTL 2 Understanding
2.	(i) Analyze the working of R-2R ladder type DAC. (ii) Compare binary weighted DAC with R-2R ladder network DAC.	(7) (6)	BTL4 Analyzing
3.	(i) With circuit schematic, explain analog switches using FET. (ii) What is meant by resolution, offset error in ADC?	(7) (6)	BTL 1 Remembering
4.	Explain in detail on the operational features of 4-bit weighted resistor type D/A converter	(13)	BTL 4 Analyzing
5.	Describe the operation of any two direct type of ADCs and Explain.	(13)	BTL 1 Remembering
6.	Summarize the following Digital to Analog & Analog to Digital conversion techniques. (i) Flash type ADC. (ii) Weighted resistor DAC.	(7) (6)	BTL 2 Understanding

7.	(i) (ii)	Draw the diagram of sample and hold circuit. State how you will reduce its hold mode droop.	(6) (7)	BTL 1	Remembering
8.		Design a 4-bit binary weighted resistor DAC for the following specifications: Use LM741 op-amp, $R = 10k\Omega$ , $V_{ref} = 2.5V$ and full scale output = 5V.	(13)	BTL 4	Analyzing
9.		A dual slope ADC has a full scale input of 2 Volts .It uses an integrating time of 10ms and integrating capacitor of 0.1 $\mu$ f.the maximum magnitude of the integrator output should not exceed 3V. Calculate the value of the integrating resistor.	(13)	BTL 3	Applying
10.		Describe in detail about the single slope type ADC with neat sketch.	(13)	BTL 3	Applying
11.	(i) (ii)	Sketch the block diagram and explain the working of Charge Balancing VFCS With functional block diagram explain A/D converter using voltage to time converter with input and output waveforms.	(6) (7)	BTL 1	Remembering
12.	(i) (ii)	Elaborate the operation of high speed sample and hold circuits. Develop a system employs a 16-bit word for representing the input signal. If the maximum output voltage is set 2V, calculate the resolution of the system and its dynamic range.	(9) (4)	BTL 6	Creating
13.		An 8-bit A/D converter accepts an input voltage signal of range 0 to 9V, What is the minimum value of the input voltage required for generating a change of 1 least significant bit? Specify the digital output for an input voltage of 4 V. What input voltage will generate all 1s at the A/D converter output?	(13)	BTL 2	Understanding
14.	(i) (ii) (iii)	The basic step of a 9-bit DAC is 10.3mV. If 000000000 represents 0V, what output is produced if the input is 101101111? Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10V range. What output voltage would be produced by a D/A converter whose output range is 0 to 10V and whose input binary number is (i) 10 (for a 2-bit D/A converter) (ii) 0110 (for a 4-bit DAC) (iii)10111100 (for a 8-bit DAC)	(3) (5) (5)	BTL 5	Evaluating
<b>PART – C</b>					
1.	(i) (ii)	For a 4-bit R-2R ladder D/A converter assume that the full scale voltage is 16V.Calculate the step change in output voltage on input varying from 01111 to 1111. Discuss the important specification of Data Converters.	(10) (5)	BTL6	Creating
2.	(i) (ii)	Draw the circuit and explain the working of dual slope A/D converter. Calculate $t_2$ for a particular dual slope ADC, $t_1$ is 83.33ms and the reference voltage is 100mv if 100 mv and 200 mv	(10) (5)	BTL 5	Evaluating

3.	Design the R-2R 4-bit converter and assume that feedback resistance $R_f$ of the op-amp is variable, the resistance $R=10k\Omega$ and $V_R =10V$ . Determine the value of $R_f$ that should be connected to achieve the following output conditions. (i) The value of 1 LSB at the output is 0.5V (ii) An analog output of 6V for a binary input of 1000. (iii)The Full-scale output voltage of 12V (iv)The actual maximum output voltage of 10V	(15)	BTL 6	Creating
4.	(i) Derive the inverted or current mode R-2R Ladder digital to analog converter and explain. (ii) Examine the inverted R-2R ladder DAC with $R=R_f=10k\Omega$ and $V_R=10V$ . Calculate the total current delivered to the op-amp and the output voltage when the binary input is 1110.	(10)  (5)	BTL 5	Evaluating

### UNIT V WAVEFORM GENERATORS AND SPECIAL FUNCTION ICs

**Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator, Low Drop – out(LDO) Regulators -Switched capacitor filter IC MF10, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto-couplers and fiber optic IC.**

#### PART – A

Q. No	Questions	BT Level	Competence
1.	What is the need for voltage regulator ICs?	BTL 2	Understanding
2.	List the characteristics and applications of Opto coupler.	BTL 4	Analyzing
3.	Sketch a fixed voltage regulator circuit and state its operation.	BTL 1	Remembering
4.	Mention the conditions for oscillation.	BTL 2	Understanding
5.	Name the four basic types of switching regulator.	BTL 1	Remembering
6.	Quote the applications of 555 timer in Monostable mode of operation.	BTL 1	Remembering
7.	Classify the three different wave forms generated by ICL8038.	BTL 2	Understanding
8.	Point out the need for current limiting in voltage regulators.	BTL 4	Analyzing
9.	Compare Linear regulator and Switched mode regulator.	BTL 5	Evaluating
10.	Examine the function of a voltage regulator .Give some examples of monolithic IC voltage regulators.	BTL 1	Remembering
11.	Draw the functional block diagram of IC 723 regulator.	BTL 1	Remembering
12.	Propose the principle of linear regulator and a switched mode power supply.	BTL 6	Creating
13.	Write the current transfer ratio of an opto coupler.	BTL 5	Evaluating
14.	Define line and load regulation of a regulator.	BTL 1	Remembering
15.	In a Astable multivibrator of 555 timer, $R_A=606k\Omega$ and $C=0.1\mu F$ . Calculate (a) $t_{HIGH}$ (b) $t_{LOW}$ (c) free running frequency (d) duty cycle (D).	BTL 6	Creating
16.	How does switched capacitor emulate resistor?	BTL 3	Applying
17.	Summarize about low drop out regulators.	BTL 2	Understanding
18.	In a monostable multivibrator using 555 timer, $R=100k\Omega$ and the time delay is 100ms.Solve for the value of C.	BTL 3	Applying
19.	Analyze the purpose of one shot multivibrator.	BTL 4	Analyzing
20.	Give reasons for the purpose of connecting a capacitor at the input and	BTL 3	Applying

	output side of an IC voltage regulator?				
<b>PART – B</b>					
1.		Write a short notes on (i) Opto couplers and (ii) Audio power amplifier	(7) (6)	BTL 2	Understanding
2.		Demonstrate and explain the functional diagram of LM 380 power amplifier.	(13)	BTL 2	Understanding
3.		Explain the working of 555 timer as Monostable Multivibrator and derive an expression for the frequency of oscillation.	(13)	BTL 1	Remembering
4.	(i)	Explain the operation of switching regulator with neat diagram.	(8)	BTL 4	Analyzing
	(ii)	Examine the operation of frequency to voltage converters.	(5)		
5.		Illustrate the working of Astable Multivibrator using op-amp with applications in detail.	(13)	BTL 1	Remembering
6.	(i)	Illustrate a phase shift oscillator to oscillate at 100 Hz.	(6)	BTL 6	Creating
	(ii)	Design a frequency to voltage converter using IC VFC 32 for a full scale output of 8V for a full scale input frequency of 80kHz with a maximum ripple of 8mV.	(7)		
7.		Define voltage regulator and explain the working of Linear Voltage regulator with neat circuit diagram using op-amps.	(13)	BTL 1	Remembering
8.	(i)	Assess the working principle of monolithic switching regulator.	(8)		
	(ii)	Evaluate how the frequency is computed using voltage to frequency converter.	(5)	BTL 5	Evaluating
9.	(i)	With neat diagram, explain the operation of a monostable multivibrators using opamp.	(8)	BTL 3	Applying
	(ii)	Illustrate the functional diagram and connection diagram of a low voltage regulator and explain.	(5)		
10.		Develop the basic principle of function generator? Draw the schematic of ICL 8038 function generator and discuss its features.	(13)	BTL3	Applying
11.		Examine a astable multivibrator circuit to generate output pulses of 25%, 50% duty cycle using a 555 timer IC with the choice of $C=0.01\mu F$ and a frequency of 4 kHz.	(13)	BTL 2	Understanding
12.	(i)	Demonstrate the working of monostable multivibrator.	(10)	BTL 1	Remembering
	(ii)	What are opto-couplers?	(3)		
13.		Analyze the working of a general purpose voltage regulator with necessary diagrams.	(13)	BTL 4	Analyzing
14.		With a neat circuit diagram, explain the working of low drop out regulators.	(13)	BTL 4	Analyzing
<b>PART – C</b>					
<b>Q. No</b>	<b>Questions</b>			<b>BT Level</b>	<b>Competence</b>
1.	(i)	In a astable multivibrator using 555 timer, $R_a=6.8K$ , $R_b = 3.3K$ , $C=0.1\mu F$ . Calculate the free running frequency.	(8)	BTL 5	Evaluating

	(ii)	Design a square wave generator using 555 timer for a frequency of 120Hz and 60% duty cycle. Assume $C=0.2\mu F$ .	(7)		
2.	(i)	Analyze the important features and pin details of switched capacitor filter IC MF10.	(8)	BTL 6	Creating
	(ii)	Design a wave generator using 555 timer for a frequency of 110Hz and 80 % duty cycle. Assume $C =0.12\mu F$	(7)		
3.		Derive the expression and circuit operation for LM 380 Audio power amplifier.	(15)	BTL 5	Evaluating
4.		Design an adjustable voltage regulator circuit using LM 317 for the following specifications: Input dc voltage =13.5 V; Output dc voltage = 5 to 9V; Load current (maximum) = 1A.	(15)	BTL 6	Creating