SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF INFORMATION TECHNOLOGY

QUESTION BANK

V SEMESTER

1908006 – COMPUTER ARCHITECTURE

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Prepared by

Dr. S. JEYALAKSHMI, Assistant Professor (Sel. G)

Mr. R. SANKARANARAYANAN, Assistant Professor (O. G.)

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SUBJECT : 1908006 - COMPUTER ARCHITECTURE

SEM / YEAR : V Sem / III Year

UNIT I - BASIC STRUCTURE OF A COMPUTER SYSTEM			
Functional Units – Basic Operational Concepts – Performance – Instructions: Language of the Computer – Operations, Operands – Instruction representation – Logical operations – decision making – MIPS Addressing– Bus structure – Bus operation			
PART – A			
1	Give the addressing modes in MIPS.	BTL 2	Understanding
2	Identify general characteristics of Relative addressing mode with an example.	BTL 4	Analyzing
3	Define Computer Architecture	BTL 1	Remembering
4	Tabulate the components of computer system	BTL 1	Remembering
5	Give the addressing modes in MIPS.	BTL 2	Understanding
6	Interpret the instruction set Architecture.	BTL 2	Understanding
7	Differentiate DRAM and SRAM.	BTL 4	Analyzing
8	Give the difference between auto increment and auto decrement addressing mode.	BTL 2	Understanding
9	What are the functions of control unit?	BTL 1	Remembering
10	Calculate throughput and response time.	BTL 3	Applying
11	Compose the three categories of the Bus	BTL 6	Creating
12	Measure the Address line.	BTL 5	Evaluating
13	Distinguish pipelining from parallelism	BTL 6	Applying
14	State the need for indirect addressing mode. Give an example.	BTL 1	Remembering
15	Show the control Line in Bus Structure.	BTL 3	Creating
16	Define Bus Arbitration.	BTL 1	Remembering
17	What are the various units in the computer?	BTL 1	Remembering
18	Compare multi-processor and uniprocessor.	BTL 4	Analyzing
19	Classify the instructions based on the operations they perform and give one example to each category.	BTL 3	Applying
20	Examine Bus in computer Architecture?	BTL 5	Evaluating

PART – B			
1	Evaluate the various techniques to represent instructions in a computer system.	BTL 5	Evaluating
2	i)List the various components of computer system and explain with neat diagram (10) ii)List the classes of applications of computers (3)	BTL 1	Remembering
3	i).What is an addressing mode in a computer? (2) ii).Describe the MIPS addressing modes with suitable examples to each category (11)	BTL 1	Remembering
4	i). Identify the various operations in computer system. (7) ii). Examine the operands of computer hardware. (6)	BTL 1	Remembering
5	i).Discuss the logical operations and control operations of computer. (8) ii).Explain the concept of Arithmetic operation with examples (5)	BTL 2	Understanding
6	Consider and explain the centralized and distributed bus system in computer organization.(13)	BTL2	Understanding
7	Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. i) Which processor has the highest performance expressed in instructions per second? (5) ii) If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions? (4) iii) We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction? (4)	BTL 4	Analyzing
8	Describe the branching operations in detail with suitable example. (13)	BTL 2	Understanding
9	i) Formulate the performance of CPU. (7) ii) Compose the factors that affect performance. (6)	BTL 6	Creating
10	i).Illustrate the different types of instruction set architecture in detail. (7) ii).Examine the basic instruction types with examples. (6)	BTL 3	Applying
11	i) Explain in detail about Technologies for Building Processors and Memory (7) ii) Analyze the bus structure in computer system and explain it (6)	BTL 1	Remembering
12	i). Compare uniprocessors and multi- processors. (8) ii). Draw the Simple Bus architecture and explain it. (5)	BTL 4	Analyzing
13	Analyze the various instruction formats and illustrate with an example. (13)	BTL 4	Analyzing
14	i) Distinguish RISC and CISC processor. (6) ii) Describe the Eight Great Ideas in Computer Architecture. (7)	BTL 2	Understanding
PART C			
1	Evaluate a MIPS assembly instruction in to a machine instruction, for the add $to, $s1, $s2 MIPS instruction. (15)	BTL 5	Evaluating

2	Assume a two address format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and the operation done in every instruction. (15)
	MOVE (R5)+, R0
	ADD (R5)+, R0
	MOVE R0, (R5)
	MOVE 16(R5), R3
	ADD #40, R5
		BTL 6	Creating

3	Assume that the variables f anf g are assigned to register $s0 and $s1 respectively. Assume that base address of the array A is in register $s2. Assume f is zero initially. (15) F = g – A[4] A[5] = f + 100 Translate the above C statement into MIPS code .how many MIPS assembly instructions are needed to perform the C statements and how many different registers are needed to carry out the C statements?	BTL 6	Creating

4	Evaluate which code sequence will execute faster according to execution time for the following conditions: (15)
	The computer with three instruction classes and CPI measurements as given below and instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 1GHZ.
	Code from CPI for the instruction class
	  A B C
	CPI 1 2 3
	
	Code from CPI for the instruction class
	  A B C
	Compiler1 2 1 2
	Compiler2 2 1 1
		BTL 5	Analyzing

UNIT II - ARITHMETIC FOR COMPUTERS

ALU – Addition and subtraction – Multiplication – Division – Floating Point Representation and operation - Sub word parallelism.

PART – A

Q.No	Questions	BT Level	Competence
1	Calculate the following: Add 510 to 610 in binary and Subtract -610 from 710 in binary.	BTL 3	Applying
2	Analyze overflow conditions for addition and subtraction.	BTL 4	Analyzing
3	Construct the Multiplication hardware diagram.	BTL 3	Applying
4	x=0000 1011 1110 1111 and y= 1111 0010 1001 1101.Examine x-y	BTL 1	Remembering
5	What is fast multiplication?	BTL 1	Remembering
6	Subtract (11011)2–(10011)2 using 1's complement and 2's complement method.	BTL 2	Understanding
7	Illustrate scientific notation and normalization with example.	BTL 3	Applying
8	Multiply 100011 * 100010	BTL 4	Analyzing
9	Give the representation of double precision floating point number.	BTL 2	Understanding
10	For the following C statement, Develop MIPS assembly code. f = g + (h − 5).	BTL 6	Creating
11	Name the floating point instructions in MIPS.	BTL 1	Remembering
12	Formulate the steps of floating point addition.	BTL 6	Creating
13	Evaluate the sequence of floating point multiplication.	BTL 5	Evaluating

14	Define guard bit. What are the ways to truncate the guard bits?	BTL 1	Remembering
15	Express the IEEE 754 floating point format. Represent (-0.75)10 in single precision	BTL 2	Understanding
16	State sub-word parallelism.	BTL 1	Remembering
17	Interpret single precision floating point number representation with example.	f a	Understanding
18	Divide 1001010 by 1000.	BTL 4	Analyzing
19	Label the steps of division algorithm.	BTL 1	Remembering

20	For the following MIPS assembly instructions above, what is the corresponding C statement?
	add f, g, h
	add f, i, f
		BTL 5	Evaluating

PART – B			
1	i) Discuss the multiplication algorithm in detail with diagram. (7) ii) Express the steps to Multiply 2*3. (6)	BTL 2	Understanding
2	Illustrate the multiplication of signed 2's complement numbers? Give algorithm and example. (13)	BTL 3	Applying
3	Describe about basic concepts of ALU design. (13)	BTL 1	Remembering
4	Develop algorithm to implement A*B. Assume A and B for a pair of signed 2's complement numbers with values: A=010111, B=101100. (13)	BTL 6	Creating
5	i) State the integer division algorithm with diagram. (7) ii) Divide 00000111 by 0010. (6)	BTL 1	Remembering
6	i) Express in detail about Carry look ahead Adder. (13) ii) Divide(12)10 by (3)10	BTL 2	Understanding
7	Point out the division of A and B (13) A=1111 B= 0011	BTL 4	Analyzing
8	i) Examine, how floating point addition is carried out in a computer system?(7) ii) Give an example for a binary floating point addition. (6)	BTL 1	Remembering
9	i) How floating point numbers are represented in IEEE 752. (6) ii) Tabulate the IEEE 752 binary representation of the number - 0.75_{10} to Single precision and Double precision. (7)	BTL 1	Remembering
10	i) Design an arithmetic element to perform the basic floating point operations. (7) ii) Discuss sub word parallelism. (6)	BTL 2	Understanding
11	i) Explain floating point addition algorithm with diagram. (7) ii) Assess the result of the numbers (0.5)10 and (0.4375)10 using binary Floating point Addition algorithm. (6)	BTL 5	Evaluating
12	Calculate using single precision IEEE 754 representation. (7 + 6) i) 32.75 ii)18.125	BTL 4	Analyzing
13	Arrange the given number 0.0625 in i) Single precision and (6) ii) Double precision formats. (7)	BTL 4	Analyzing
14	Solve using Floating point multiplication algorithm i) A= 1.10 10 X 1010 B= 9.200X10-5 (7) ii) 0.5 10 X 0.4375 10 (6)	BTL 3	Applying
PART C			
1	Multiply the following signed numbers using Booth algorithm A=(-34)10 =(1011110)2 and B=(22)10= (0010110) 2where B is multiplicand and A is multiplier. (15)	BTL 6	Creating

2	Evaluate the sum of 2.6125 * 101 and 4.150390625 * 101 by hand, assuming A and B are stored in the 16-bit half precision. Assume 1 guard, 1 round bit and 1 sticky bit and round to the nearest even. Show all the steps. (15)	BTL 5	Evaluating
3	Summarize 4 bit numbers to save space, which implement the multiplication algorithm for 00102, 00112 with hardware design. (15)	BTL 5	Evaluating
4	Design 4 bit version of the algorithm to save pages, for dividing 000001112 by 00102 with hardware design. (15)	BTL 6	Creating

UNIT III – PROCESSOR AND CONTROL UNIT

A Basic MIPS implementation – Building a Data path – Control Implementation Scheme – Pipelining – Pipelined data path and control – Handling Data Hazards & Control Hazards – Exceptions

PART – A

Q.No	Questions	BT Level	Competence
1	Express the control signals required to perform arithmetic operations.	BTL 2	Understanding
2	Define hazard. Give an example for data hazard.	BTL 2	Understanding
3	Recall pipeline bubble.	BTL 1	Remembering
4	List the state elements needed to store and access an instruction.	BTL 1	Remembering
5	Draw the diagram of portion of data path used for fetching instruction.	BTL 2	Understanding
6	Distinguish Sign Extend and Vector interrupts.	BTL 2	Understanding
7	Name the R-type instructions.	BTL 1	Remembering
8	Evaluate branch taken and branch not taken in instruction execution.	BTL 5	Evaluating
9	State the two steps that are common to implement any type of instruction.	BTL 1	Remembering
10	Design the instruction format for the jump instruction.	BTL 6	Creating
11	Classify the different types of hazards with examples.	BTL 4	Analyzing
12	Illustrate data forwarding method to avoid data hazards.	BTL 3	Applying
13	Assess the methods to reduce the pipeline stall.	BTL 5	Evaluating
14	Tabulate the use of branch prediction buffer.	BTL 1	Remembering
15	Show the 5 stages pipeline.	BTL 3	Applying
16	Point out the concept of exceptions and interrupts.	BTL 4	Analyzing
17	What is pipelining?	BTL 1	Remembering
18	Illustrate the various phases in executing an instruction.	BTL 3	Applying
19	Classify the types of instruction classes and their instruction formats.	BTL 4	Analyzing
20	Generalize what is exception. Give one example for MIPS exception.	BTL6	Creating

PART – B			
1	Discuss the basic MIPS implementation of instruction set. (13)	BTL 2	Understanding
2	State and draw a simple MIPS data path with control unit and explain the execution of ALU instruction. (13)	BTL 1	Remembering
3	i) List the types of hazards. (5) ii) Describe the methods for dealing with the control hazards. (8)	BTL 1	Remembering
4	Design and develop an instruction pipeline working under various situations of pipeline stall. (13)	BTL 6	Creating
5	i) What is data hazard? How do you overcome it? (7) ii) What are its side effects? (6)	BTL 1	Remembering
6	i) Summarize control implementation scheme. (7) ii) Distinguish the data and control path methods in pipelining. (6)	BTL 2	Understanding
7	i) Differentiate sequential execution and pipelining. (7) ii) Select the model for building a data path. (6)	BTL 4	Analyzing
8	Recommend the techniques for i) Dynamic branch prediction. (7) ii) Static branch prediction. (6)	BTL 5	Evaluating
9	Examine the approaches would you use to handle exceptions in MIPS. (13)	BTL 3	Applying
10	i) Analyze the hazards caused by unconditional branching statements. (7) ii) Describe operand forwarding in a pipeline processor with a diagram. (6)	BTL 4	Analyzing
11	Express the modified data path to accommodate pipelined executions with a diagram.(13)	BTL 2	Understanding
12	i) Explain single cycle and pipelined performance with examples. (7) ii) Point out the advantages of pipeline over single cycle. (6)	BTL 4	Analyzing
13	i) Tabulate the ALU control with suitable truth table. (7) ii) Differentiate R-type instruction and memory instruction. (6)	BTL 1	Remembering
14	With a suitable set of sequence of instructions show what happens when the branch is taken, assuming the pipeline is optimized for branches that are not taken and that we moved the branch execution to the ID stage. (13)	BTL 3	Applying
PART C			

1	Assume the following sequence of instructions are executed on a 5 stage pipelined data path: (15)
	add r5, r2, r1
	lw r3, 4(r5)
	lw r2, 0(r2)
	or r3, r5, r3
	sw r3, 0(r5)
	If there is no forwarding or hazard detection, insert NOPS to ensure correct execution.
	i) If the processor has forwarding, but we forgot to implement the hazard detection unit, what if happens when this code executes? (5)
	ii) If there is forwarding, for the first five cycles, compose which signals are asserted in each cycle. (5)
	iii) If there is no forwarding, what if new inputs and output signals do we need for the hazard detection unit. (5)
		BTL6	Creating

2	Explain in detail about the laundry process through which the pipelining techniques can be established. (15)	BTL 5	Evaluating
3	Consider the following loop: (15) Loop: lw r1,0(r1) and r1,r1,r2 lw r1,0(r1) lw r1,0(r1)	BTL 5	Evaluating

	beq r1, r0, loop Assume that perfect branch prediction is used (no stalls) that there are no delay slots, and that the pipeline has full forwarding support. Also assume that many iterations of this loop are executed before the loop exits. i) Assess a pipeline execution diagram for the third iteration of this loop. (8) ii) Show all instructions that are in the pipeline during these cycles (for all iterations). (7)		
4	Plan the pipelining in MIPS architecture and generate the exceptions handled in MIPS. (15)	BTL 6	Creating

UNIT IV - PARALLELISIM

Parallel processing challenges – Flynn's classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors.

PART – A

Q.No	Questions	BT Level	Competence
1	State the main idea of ILP.	BTL 2	Understanding
2	Illustrate the overall speedup if a webserver is to be enhanced with a new CPU which is 10 times faster on computation than an old CPU. The original CPU spent 40% of its time processing and 60% of its time waiting for I/O.	BTL 3	Applying
3	List the three important properties of vector instructions.	BTL 1	Remembering
4	Analyze the main characteristics of SMT processor.	BTL 4	Analyzing
5	Quote the importance of loop unrolling technique.	BTL1	Remembering
6	Define VLIW processor.	BTL1	Remembering
7	Express anti-dependence. How is it removed?	BTL 2	Understanding
8	State the efficiency of superscalar processor.	BTL 1	Remembering
9	Differentiate between strong scaling and weak scaling.	BTL 2	Understanding
10	Show the performance of cluster organization.	BTL 3	Applying
11	Compare SMT and hardware multithreading.	BTL 5	Evaluating
12	Define the Flynn classification.	BTL 1	Remembering
13	Integrate the ideas of in-order execution and out-of-order execution.	BTL 6	Creating
14	Discriminate UMA and NUMA.	BTL 5	Evaluating
15	Quote fine grained multithreading.	BTL 1	Remembering
16	Express the need for instruction level parallelism.	BTL 2	Understanding
17	Formulate the various approaches to hardware multithreading.	BTL 6	Creating
18	Categorize the various multithreading options.	BTL 4	Analyzing

19	Differentiate fine grained multithreading and coarse grained multithreading.	BTL 4	Analyzing
20	Classify shared memory multiprocessor based on the memory access latency	BTL 3	Applying
	PART – B		
1	i) Define parallelism and its types. (7) ii) List the main characteristics of Instruction level parallelism. (6)	BTL 1	Remembering
2	i) Give the concept of parallel processing. (7) ii) Summarize the challenges faced by parallel processing. (6)	BTL 2	Understanding
3	Express in detail about hardware multithreading. (13)	BTL 2	Understanding
4	Solve: suppose you want to achieve a speed up to 90 times faster with 100 processors. What percentage of the original computation can be sequential?	BTL 3	Applying
5	List the software and hardware techniques to achieve Instruction Level Parallelism. (13)	BTL 1	Remembering
6	i) Point out how will you use shared memory concept in multi-processor? (7) ii) Compare and contrast Fine grained and Coarse grained multithreading. (6)	BTL 4	Analyzing
7	i) Evaluate the features of Multicore processors. (7) ii) How message passing is implemented in Multiprocessors (6)	BTL 5	Evaluating
8	i).Classify the types of multithreading. (7) ii).Analyze the advantages in multithreading. (6)	BTL 4	Analyzing
9	Formulate the ideas of Flynn's classification. (13)	BTL 6	Creating
10	Elaborate in detail about the following (7 + 6) i) SISD ii) MIMD	BTL 1	Remembering
11	Explain simultaneous Multithreading with example. (13)	BTL 4	Analyzing
12	i)Describe about Graphics Processing unit (7) ii) Discuss about cluster and warehouse architecture (6)	BTL 1	Remembering
13	Illustrate the following in detail i) Data Dependence (5) ii) Name Dependence (4) iii) Control dependence (4)	BTL 3	Applying
14	Discuss the following in detail i) Vector processor. (7) ii) Superscalar processor. (6)	BTL 2	Understanding
	PART C		

1	Explain how would this loop be scheduled on a static two issue pipeline for MIPS? (15)
	Loop: lw $t0,0($s1) #$t0=array element
	Addu $t0,$t0,$s2 #add scalar in $s2
	Sw $t0, 0($s1) # store result
	Addi; %s1,$s1, -4 #decrement pointer
	Bne $s1,$zero,loop # branch $s1!=0
	Decide and reorder the instruction to avoid as many pipeline stalls as possible. Assume branches are predicted, so that control hazards are handled by the hardware.
		BTL 6	Creating

2	A pipelined processor uses delayed branch technique. Recommend any one of the following possibility for the design of the processor. In the first possibility, the processor has a 4-satge pipeline and one delay slot. In the second possibility, it has a 6-stage pipeline and two delay slots. Compare the performance of these two alternatives, taking only the branch penalty into account. Assume that 20% of the instructions are branch instructions and that an optimizing compiler has an 80% success rate in filling in the single delay slot. For the second alternative, the compiler is able to fill the second slot 25% of the time. (15)	BTL 5	Evaluating

3	Consider the following portions of two different programs running at the same time on four processors in a symmetric multicore processor (SMP). Assume that before this code is run, both x and y are 0? Core 1: x=2; Core 2: y=2; Core 3: w= x + y +1; Core 4: z= x + y; i. What if all the possible resulting values of w, x, y, z ? For each possible outcome, explain how we might arrive at those values. (8) ii. Develop the execution more deterministic so that only one set of values is possible? (7)	BTL 6	Creating
4	Suppose we want to perform 2 sums: one is a sum of 10 scalar variables and one is a matrix sum of a pair of two dimensional arrays, with dimensions 10 by 10. For now let's assume only the matrix sum is parallelizable. What if the speed up do you get with 10 versus 40 processors and next calculate the speed ups assuming the matrices grow to 20 by 20. (15)	BTL6	Creating

UNIT V - MEMORY & I/O SYSTEMS

Memory Hierarchy - memory technologies – cache memory – measuring and improving cache performance – virtual memory, TLB's – Accessing I/O Devices – Interrupts – Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits - USB.

PART – A

Q.No	Questions	BT Level	Competence
1	Distinguish the types of locality of references.	BTL 2	Understanding
2	Draw the structure of memory hierarchy	BTL 1	Remembering
3	Give the definition of memory –mapped I/O.	BTL 2	Understanding
4	Compare and contrast SRAM and DRAM.	BTL 4	Analyzing
5	What is the need to implement memory as a hierarchy?	BTL 1	Remembering
6	Define Rotational Latency.	BTL 1	Remembering
7	State direct-mapped cache.	BTL 1	Remembering
8	Evaluate the following instance wherein the cache size is 64 blocks and block size is 16 bytes. What block number does byte address 1200 map?	BTL 5	Evaluating
9	Formulate, how many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bit address?	BTL 6	Creating
10	Analyze the writing strategies in cache memory.	BTL 4	Analyzing
11	Integrate the functional steps required in an instruction cache miss.	BTL 6	Creating
12	State hit rate and miss rate.	BTL 1	Remembering
13	Summarize the various block placement schemes in cache memory.	BTL 2	Understanding
14	Quote the purpose of Dirty/Modified bit in Cache memory.	BTL 1	Remembering
15	Point out how DMA can improve I/O speed.	BTL 4	Analyzing
16	Show the role of TLB in virtual memory.	BTL 3	Applying

17	Illustrate the advantages of virtual memory.	BTL 3	Applying
18	Assess the relationship between physical address and logical address.	BTL 5	Evaluating
19	Differentiate Programmed I/O and Interrupt I/O.	BTL 2	Understanding
20	Demonstrate the sequence of events involved in handling an interrupt request from a single device.	BTL 3	Applying
	PART-B		
1	i) List the various memory technologies and examine its relevance in architecture design. (7) ii) Identify the characteristics of memory system. (6)	BTL 1	Remembering
2	Elaborate in detail the memory hierarchy with neat diagram. (13)	BTL 1	Remembering
3	i) Give the advantages of cache. (7) ii) Identify the basic operations of cache in detail with diagram. (6)	BTL 2	Understanding
4	Express the following various mapping schemes used in cache design. i) Direct. (4) ii) Associative. (4) iii) Set associative. (5)	BTL 2	Understanding
5	i) Analyze the given problem: (7) A byte addressable computer has a small data cache capable of holding eight 32-bit words. Each cache block contains 132-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses – 200, 204, 208, 20C, 2F4, 2F0, 200,204,218, 21C, 24C, 2F4. The pattern is repeated four times. Assuming that the cache is initially empty, show the contents of the cache at the end of each pass, and compute the hit rate for a direct mapped cache. ii) What are the methods used to measure and improve the performance of the cache. (6)	BTL 4	Analyzing
6	i) Define virtual memory and its importance. (7) ii) Examine TLB with necessary diagram. (6)	BTL 1	Remembering
7	i) Demonstrate the DMA controller. (7) ii) Illustrate how DMA controller is used for direct data transfer between memory and peripherals? (6)	BTL 3	Applying
8	i) Evaluate the advantages of interrupts. (7) ii) Summarize the concept of interrupts with neat diagrams. (6)	BTL 5	Evaluating
9	Design standard input and output interfaces required to connect the I/O device to the bus. (13)	BTL 6	Creating
10	Classify the bus arbitration techniques of DMA in detail. (13)	BTL 4	Analyzing
11	Point out the following in detail i) Programmed I/O. (7) ii) Instructions executed by IOP. (6)	BTL 4	Analyzing
12	Describe in detail about the methods used to reduce cache misses. (13)	BTL 1	Remembering
13	Discuss virtual memory address translation in detail with necessary diagram. (13)	BTL 2	Understanding
14	Calculate the performance the processor : Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, estimate how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%. (13)	BTL 3	Applying

PART C			
1	Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR) and Mean Time To Failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about devices with the following metrics: MTTF : 3 years MTTR: 1 day i) Develop and calculate the MTBF for each of the devices. (4) ii) Develop and calculate the availability for each of the devices. (4) iii) What if happens to availability as the MTTR approaches 0? (4) iv) What if happens to availability as the MTTR gets very high? (3)	BTL6	Creating
2	Design and explain parallel priority interrupt hardware for a system with eight interrupt sources. (15)	BTL6	Creating
3	For a direct mapped cache design with a 32 bit address, the following bits of the address are used to access the cache. Tag : 31-10 Index: 9-5 Offset: 4-0 i) Judge what is the cache block size? (5) ii) Decide how many entries does the cache have? (5) iii) Assess what is the ratio between total bits required for such a cache implementation over the data storage bits? (5)	BTL5	Evaluating
4	Summarize by considering web application. Assuming both client and servers are involved in the process of web browsing application, where can caches be placed to speed up the process. Design a memory hierarchy for the system. Show the typical size and latency at various levels of the hierarchy. What is the relationship between the cache size and its access latency? What are the units of data transfers between hierarchies? What is the relationship between data location, data size and transfer latency? (15)	BTL5	Evaluating