SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Question Bank

M.E Communication Systems – I Semester

1911108 – REAL TIME EMBEDDED SYSTEMS

Regulation 2019

ACADEMIC YEAR 2019 – 20 ODD

Prepared by

Mr. S.SENTHILMURUGAN,

Assistant Professor (Sel. G)/ECE

UNIT I INTRODUCTION TO ARM PROCEESORS

Fundamentals of ARM, ARM Instruction set, Thumb Instruction set, ARM assembly language programming, Digital Signal Processing in ARM, Exceptions & Interrupt Handling. Introduction to ARM-v7-M (Cortex-M3) and ARM-v7-R (CortexR4) Processors.

PART A

Q.No	Questions	BT Level	Competence
1.	State Embedded system and list the types of ARM processor modes.	BTL1	Remember
2.	In what ways CISC and RISC processors differ?	BTL1	Remember
3.	Distinguish single register Load/Store & Multiple register Load/Store instructions.	BTL2	Understand
4.	Compare and contrast Exception & Traps.	BTL2	Understand
5.	Could you summarize the major goals of embedded system design?	BTL5	Evaluate
6.	Demonstrate with suitable example: Thumb code offers high code density.	BTL3	Apply
7.	Define the terms UML and Co-processor.	BTL1	Remember
8.	What is the difference between a big-endian and little –endian data representation?	BTL1	Remember
9.	Draw the format of CPSR & SPSR.	BTL1	Remember
10.	How do you return from an ARM procedure?	BTL1	Remember
11.	Explain the syntax of data processing class of instruction.	BTL5	Evaluate
12.	Illustrate the features of conditional execution of ARM instruction with suitable example.	BTL3	Apply
13.	Write ARM7 ALP fragment that implements 'block move' functions assuming the elements of the block are words, the starting address of source block is in 'r9' register, the destination address is in 'r10' register and the size of the block is 8 words.	BTL6	Create
14.	Compare the basic task of SWI and SWP instructions.	BTL4	Analyze
15.	Investigate the result of execution of 'MOV r0, 055555555' instruction? Why?	BTL6	Create
16.	Point out the advantages and disadvantages of load-store multiple instructions.	BTL2	Understand
17.	Describe the addressing modes of load - store instruction.	BTL2	Understand
18.	Illustrate the importance of instruction scheduling and conditional execution of ARM instructions.	BTL3	Apply
19.	Differentiate ARM and THUMB instruction set.	BTL4	Analyze
20.	Implement the multiplication of a register by 35 using 'ADD' and 'RSB' instructions.	BTL4	Analyze

PART –B

1.	(i)Define the architectural inheritance of ARM processor and explain. (7) (ii)Name the principle features of ARM architecture. (6)	BTL1	Remember
2.	(i) Discuss the instruction set of ARM processor with examples? (10) (ii) Formulate necessary code using ARM assembly language program for creating a delay? (3)	BTL6	Create
3.	Outline the organization of ARM processor and Co-processor? (13)	BTL1	Remember
4.	How to construct loop structures (i) Using fixed number of iterations. (6) (ii) Using variable number of iterations. (7)	BTL3	Apply

5.	(i)Discuss the interrupt handling schemes of ARM processor. (7) (ii)Summarize its Advantages and Disadvantages. (6)	BTL2	Understand
6.	State in detail about the (i) 3 stage pipelined ARM Organization. (6) (ii) 5 stage pipelined ARM Organization. (7)	BTL1	Remember
7.	(i) Draw the data core flow model of a ARM processor and explain the function of each block. Also explain the operating modes supported by the ARM process. (8) (ii) With relevant ARM instructions, explain the various forms of base-plus offset addressing. (5)	BTL4	Analyze
8.	Explain with neat diagram of exception handling and modes of operations. (13)	BTL2	Understand
9.	Illustrate the thumb instruction set of ARM processor with examples in detail. (13)	BTL2	Understand
10.	(i) Conclude on Optimizing the assembly code in ARM processor. (10) (ii) Point out the factors that influence the efficiency of loops structure. (3)	BTL5	Evaluate
11.	(i) Examine the implementation of branch, call and return instructions in ARM instruction set. (10) (ii) Write a program to find the product of two numbers? (3)	BTL4	Analyze
12.	Write ARM assembly language code that handles a breakpoint. It should save the necessary registers, call a subroutine to communicate with the host, and upon return from the host, cause the break pointed instruction to be properly executed (13)	BTL1	Remember
13.	(i)Describe about the interrupts and its associated usage in ARM processor. (7) (ii)How would you enable and disable FIQ and IRQ exceptions. (6)	BTL3	Apply
14.	(i) Analyze the structure arrangement in programming ARM processor. (7) (ii)Propose the accomplishment of Push and Pop instructions in ARM. (6)	BTL4	Analyze
PART C			
1.	Elaborate the following (i) ARM instruction set and (8) (ii) THUMP instruction set. (7)	BTL6	Create
2.	(i)Select the guidelines to write code for FIR filters on ARM? (7) (ii)Implement a block filter in ARM processor using DSP concepts? (8)	BTL5	Evaluate
3.	Develop a code to implement radix – 4 FFT using ARM processor. (15)	BTL6	Create
4.	Describe with neat diagram of Exception and Interrupt Handling schemes. (15)	BTL5	Evaluate

UNIT II COMPUTING PLATFORM AND DESIGN ANALYSIS

CPU buses – Memory devices – I/O devices – Memory Protection Units – Memory Management Units – Component interfacing – Design with microprocessors – Development and Debugging – Program design – Model of programs – Assembly and Linking – Basic compilation techniques – Analysis and optimization of execution time, power, energy, program size – Program validation and testing.

PART A

Q.No	Questions	BT Level	Competence
1.	Define the term page table and list their types.	BTL 1	Remember
2.	How would you define cross compiler?	BTL 1	Remember
3.	What is meant by four cycle handshake?	BTL2	Understand
4.	Identify the debugging challenges.	BTL3	Apply

5.	Point out software configuration and control components in MMU.	BTL2	Understand
6.	Classify the types of assembler and describe its functions?	BTL4	Analyze
7.	Discuss about the data flow graph?	BTL3	Apply
8.	Provide any two features of software development for embedded system.	BTL6	Create
9.	Quote the use of bus bridge?	BTL 1	Remember

10.	For the basic given block, rewrite in single assignment form and draw the data flow graph.
	w = a-b+c
	x = w-d;
	y = x-2;
	w = a+b-c;
	z = y+d;
	y = b*c;
		BTL5	Evaluate

11.	List any 2 technique used to optimize execution time of a program?	BTL 1	Remember
12.	If you have a choice among several DRAMs of the same capacity but with different data widths, when would you want to use a narrower memory? When would you want to use a taller memory?	BTL6	Create
13.	Classify the IO devices used in design of embedded system?	BTL3	Apply
14.	Point out the components of typical bus.	BTL 1	Remember
15.	Show the content of the assembler's symbol table at the end of code generation for each line of the following program. ORG 100 p1 CMP r0,r1 BEQ x1 p2 CMP r0,r2 BEQ x2 p2 CMP r0,r3 BEQ x3	BTL4	Analyze
16.	Differentiate burst mode and page mode operations.	BTL4	Analyze
17.	Draw the timing diagram of Bus read and write operation.	BTL5	Evaluate
18.	Discuss about Busy Wait I/O Concept in polling.	BTL2	Understand
19.	Mention the need of a watchdog timer.	BTL 1	Remember
20.	Outline the memory protection rules.	BTL2	Understand
PART –B			
1.	How would you explain the various bus structures used in Embedded Systems? (13)	BTL 1	Remember

2.	(i) Draw a UML sequence diagram for copying characters from an input to an output device using busy wait I/Q. The diagram should include the two devices and two busy-wait I/O handle (6)
	(ii) Use the branch condition testing strategy to determine a set of tests for the following statement:
	if (a < 5 && b > 7) proc1( );
	else if (a < 5) proc2( );
	else if & > 7) proc3( );
	else proc4( ); (7)
		BTL 1	Remember

3.	Name the IO devices used in embedded systems and describe about each device in detail with necessary diagrams? (13)	BTL2	Understand

4.	(i) Draw the UML state diagram for a bus mastership transaction in which one side shows the CPIJ as the default bus master and the other shows the device that can request bus mastership. (6)
	(ii) The following loop is executed on a machine that has a lK word data cache with four words per cache line.
	for (i = 0; i < 50; i++)
	for (j = 0;j < 4; j++)
	x[i][j] = a[i][j] * c[i];
	How 'x' and 'a' must be placed relative to each other in memory in order to produce a conflict miss every time the inner loop's body is executed and how 'x' and 'a' must be placed relative to each other in memory if no conflict misses are to be produced ? (7)
		BTL3	Apply

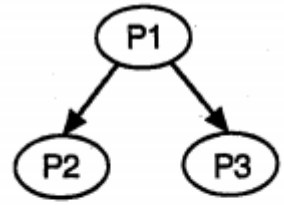
5.	Explain how debugging is carried out using debuggers & compliers with examples? (13)	BTL4	Analyze
6.	With an example explain how Logic analyzer, In circuit Emulator and Co simulator are used as debugging tools. (13)	BTL6	Create
7.	Write short notes on (i)Assembly. (8) (ii)Linking. (5)	BTL2	Understand
8.	Discuss about the Basic compilation techniques? (13)	BTL 1	Remember
9.	Show in detail about the Program level energy, power analysis and optimization. (13)	BTL4	Analyze
10.	(i)Summarize the need for ICE, JTAG for embedded system development? (8) (ii) State the advantages of vectored addressing of stack? (5)	BTL3	Apply
11.	Compose model of programs and Program design with suitable examples? (13)	BTL4	Analyze
12.	What are program Validation and testing? Discuss with necessary illustrations? (13)	BTL2	Understand
13.	(i)Write about clear box testing? (5) (ii)Outline the debugging process with necessary examples? (8)	BTL 1	Remember
14.	(i)Narrate about Interpreters and JIT compilers? (6) (ii)Point out any one device which acts as input and output device used in embedded systems and describe in detail? (7)	BTL5	Evaluate
	PART C		
1.	Write an ARM code for compiling the arithmetic expression a*b + 5*(c – d)? (15)	BTL6	Create

2.	Illustrate operator scheduling for register allocation for the given C code fragment:
	w = a + b;
	x = c + d;
	y = x + e;
	z = a – b; (15)
		BTL5	Evaluate

3.	(i) Evaluate with necessary diagrams about the design pattern, loop transformation and scheduling. (10) (ii) Frame the key features of clear box testing. (5)	BTL5	Evaluate
4.	Describe in detail about priority based scheduling with an example. (15)	BTL6	Create

UNIT III PROCESS AND OPERATING SYSTEMS			
Multiple tasks and multi processes – Processes – Context Switching – Scheduling policies - Multiprocessor – Inter Process Communication mechanisms – Evaluating operating system performance – Power optimization strategies for processes – Firmware and Operating Systems for ARM processor.			
PART A			
Q.No	**Questions**	**BT Level**	**Competence**
1.	What is the use of interrupt service routine?	BTL2	Understand
2.	What are the 3 conditions that must be examined by the re-entrant function?	BTL3	Apply
3.	Provide an examples of (i) Blocking inter process communication. (ii) Non-blocking inter process communication.	BTL2	Understand
4.	What is meant by context switching mechanism?	BTL2	Understand
5.	Compare between a process and thread.	BTL4	Analyze
6.	List out the functionalities supported by an operating system.	BTL 1	Remember
7.	Identify the major goals of an embedded system design?	BTL3	Apply
8.	Bring out the difference between a process and a task.	BTL3	Apply
9.	Summarize the major inter process communication mechanisms?	BTL5	Evaluate
10.	Elaborate the functions of preemptive real time operating system.	BTL6	Create
11.	Determine the important characteristics of Multitasking.	BTL5	Evaluate
12.	Draw the sequence diagram for preemptive execution.	BTL 1	Remember
13.	Elaborate the ways of assigning priorities in scheduling?	BTL6	Create
14.	Write the metrics CPU utilization.	BTL 1	Remember
15.	Outline the various scheduling states of a process.	BTL2	Understand
16.	How would you define threads?	BTL 1	Remember
17.	Give examples of blocking and Non-blocking inter process communication	BTL 1	Remember
18.	How is a Real time operating system uniquely different than a general purpose OS?	BTL 1	Remember
19.	Investigate the organization of scheduling policy.	BTL4	Analyze
20.	Point out the different ways of communication in process.	BTL4	Analyze
PART –B			
1.	What are the services of operating system in handling multi process scheduling and communication? (13)	BTL 1	Remember
2.	Demonstrate any two scheduling policies used in multi process environment? (13)	BTL2	Understand
3.	(i) Explain why an automobile engine requires multi rate control? (5) (ii) With suitable example explain the Earliest – Deadline – First scheduling? (8)	BTL 1	Remember
4.	Analyze the power management and optimization for processes and its strategies for processes? (13)	BTL4	Analyze

<table>
<tr><td>5.</td><td>How to evaluate operating system performance? Explain? (13)</td><td>BTL5</td><td>Evaluate</td></tr>
<tr><td>6.</td><td>(i)Summarize about multi task and multi process with respect to embedded systems? (8)
(ii)Compare EDF and RMS algorithm? (5)</td><td>BTL2</td><td>Understand</td></tr>
<tr><td>7.</td><td>(i) Describe in detail about the Inter Process Communication mechanisms? (10)
(ii) Write short notes on Co – operative scheduling? (3)</td><td>BTL4</td><td>Analyze</td></tr>
<tr><td>8.</td><td>(i)Outline the concepts of priority based context switching mechanism? (3)
(ii)Discuss about the various priorities based scheduling algorithms? (10)</td><td>BTL2</td><td>Understand</td></tr>
<tr><td>9.</td><td>(i) With neat sketches, explain in detail about shared memory communication and message passing mechanisms (7)
(ii) In each of the circumstance given below, would shared memory or message passing communication be better? Explain.
A) A digital video decoder and a process that overlays user menus on the display
B) A software modem process and a printing process in a fax machine. (6)</td><td>BTL 1</td><td>Remember</td></tr>
<tr><td>10.</td><td>Point out the process of evaluation and optimization of OS performance? (13)</td><td>BTL4</td><td>Analyze</td></tr>
<tr><td>11.</td><td>(i)With necessary diagrams describe Advanced Configuration and Power Interface? (8)
(ii)Annotate the CPU metric used in embedded Systems? (5)</td><td>BTL 1</td><td>Remember</td></tr>
<tr><td>12.</td><td>(i)Briefly explain about co-operative multitasking and pre-emptive multitasking. Bring out the difference between these two context switching techniques. (8)
(ii)Briefly explain about Advanced Configuration and Power Interface (ACPI). (5)</td><td>BTL3</td><td>Apply</td></tr>
<tr><td>13.</td><td>(i)Using C language, write the code for EDF algorithm? (8)
(ii)How to use SWP instruction to implement atomic test and set in ARM? (5)</td><td>BTL3</td><td>Apply</td></tr>
<tr><td>14.</td><td>(i)Define scheduling overhead? (3)
(ii)Determine the utilization of the given three processes. (10)
<table><tr><th>Process</th><th>Period</th><th>Execution Time</th></tr><tr><td>P1</td><td>1.0×10^{-3}</td><td>1.0×10^{-3}</td></tr><tr><td>P2</td><td>1.0×10^{-3}</td><td>2.0×10^{-3}</td></tr><tr><td>P3</td><td>5.0×10^{-3}</td><td>3.0×10^{-3}</td></tr></table></td><td>BTL6</td><td>Create</td></tr>
<tr><td colspan="4">PART C</td></tr>
</table>

1.	Interpret and Analyze the scheduling process by applying Rate Monotonic Algorithm for the given set of process. (15) Process / Execution Time / Period P1 / 1 / 4 P2 / 2 / 6 P3 / 3 / 12	BTL5	Evaluate
2.	For the given set of periodic processes shown in below Fig. all of which share the same deadline of 12:  Process / CPU time P1 / 2 P2 / 1 P3 / 2 (i) Schedule the processes for the given arrival times using standard rate monotonic scheduling (no data dependencies). (7) (ii) Schedule the processes taking advantage of the data dependencies. By how much is the CPU utilization reduced? (8)	BTL6	Create
3.	(i) Discuss about pre-emptive real time operating systems in detail. (8) (ii) Evaluate the special characteristics of Processes and Internet with the help of a suitable diagrams. (7)	BTL5	Evaluate
4.	Create the scheduling process by employing Earliest Deadline first for the given set of process. (15) Process / Execution Time / Period P1 / 1 / 3 P2 / 1 / 4 P3 / 2 / 5	BTL6	Create

UNIT IV HARDWARE ACCELERATES & NETWORKS			
Accelerators – Accelerated system design – Distributed Embedded Architecture –Networks for Embedded Systems – Network based design – Internet enabled systems.			
PART A			
Q. No	**Questions**	**BT Level**	**Competence**
1.	Mention the services provided by TCP.	BTL 1	Remember
2.	State the need for accelerator?	BTL 1	Remember
3.	Give the advantages of multiprocessors used in embedded system design.	BTL2	Understand
4.	Draw the CAN data frame packet format.	BTL 1	Remember

5.	Compare fixed priority arbitration and round – robin arbitration.	BTL3	Apply
6.	Write down the networks for distributed embedded systems.	BTL2	Understand
7.	Why did you support distributed system in embedded system?	BTL5	Evaluate
8.	What are the difference between multistage network and direct network?	BTL4	Analyze
9.	Summarize the role played by the accelerator in the design of embedded system.	BTL5	Evaluate
10.	Narrate the important requirements to develop Network based embedded systems.	BTL 1	Remember
11.	How would you highlight the use of exponential back off technique?	BTL6	Create
12.	Why did you suggest networks instead of microprocessor bus while designing an embedded system?	BTL6	Create
13.	Point out the advantages of network based design?	BTL2	Understand
14.	State some of the networks dedicated for embedded systems.	BTL2	Understand
15.	List some internet enabled embedded systems.	BTL 1	Remember
16.	Classify the different types of embedded system architectures.	BTL3	Apply
17.	What is the concept behind "Atomic test and Set" protocol?	BTL 1	Remember
18.	Analyze the component involved to calculate the execution time for an accelerator?	BTL4	Analyze
19.	Differentiate single hop network from multi hop network?	BTL4	Analyze
20.	List the merits of embedded distributed architecture?	BTL3	Apply
	PART –B		
1.	With suitable examples explain the Accelerator system design process? (13)	BTL 1	Remember
2.	Discuss in detail about the distributed embedded architecture with suitable example. (13)	BTL 1	Remember
3.	(i) With a neat block diagram, explain briefly how the CPU cache causes problems for accelerators and also suggest a technique by which the problem could be overcome? (8) (ii) With an example, explain how does single threaded or multithreaded control of an accelerator will affect the speedup factor? (5)	BTL 1	Remember
4.	Explain about network based embedded system design with suitable diagrams. (13)	BTL4	Analyze
5.	Point out how the internet can be used by embedded computing system. (13)	BTL4	Analyze
6.	Illustrate I^2C bus for an embedded system with meaningful diagrams. (13)	BTL4	Analyze
7.	(i)Outline the concepts of Accelerated system Design in embedded systems. (8) (ii) State the advantages of accelerated system Design. (5)	BTL2	Understand
8.	Write short notes on (i)CAN bus protocol. (7) (ii)Ethernet. (6)	BTL 1	Remember
9.	Narrate the detailed description of (i) Cross bar network. (6) (ii) Multistage network. (7)	BTL2	Understand
10.	Annotate the principle of distributed system design with a suitable example. (13)	BTL6	Create
11.	(i)With a suitable example explain the operation of Internet enabled system. (7)	BTL2	Understand

	(ii)Describe the network abstractions with the help of OSI model layers. (6)		
12.	Demonstrate Network based system Design with necessary diagrams. (13)	BTL3	Apply
13.	Mention the different types of network buses used in creating the distributed embedded computing platform. With neat sketches, state transition graph and control word formats; briefly explain how the data transaction is taking place using the I^2C bus? (13)	BTL5	Evaluate
14.	(i)Describe the different arbitration schemes with diagrams. (10) (ii)Summarize about Message passing programming. (3)	BTL3	Apply
	PART C		
1.	Use principle of Distributed system to design an elevator controller. (15)	BTL6	Create
2.	Illustrate the usage of automotive networks while designing an embedded system. (15)	BTL5	Evaluate
3.	Evaluate how an IP packet may be sent from a client on one Ethernet to a client on a second Ethernet. The two Ethernets are connected by a router. (15)	BTL5	Evaluate
4.	Describe briefly the system architecture framework of CPU accelerators. (15)	BTL6	Create

UNIT V CASE STUDY			
Hardware and software co-design - Data Compressor - Software Modem – Personal Digital Assistants – Set–Top–Box. – System-on-Silicon – FOSS Tools for embedded system development. Medical monitoring systems, Process control system (temp, pressure) Soft real time: Automated vending machines, Communication: Wireless (sensor) networks.			
PART A			
Q.No	**Questions**	**BT Level**	**Competence**
1.	What is hardware and software co design?	BTL 1	Remember
2.	Point out the steps to destroy a message queue.	BTL4	Analyze
3.	Give any two advantages of Data Compressor.	BTL2	Understand
4.	State the applications of Software Modem.	BTL 1	Remember
5.	Describe about PDA.	BTL2	Understand
6.	Mention the FOSS tools for embedded systems.	BTL 1	Remember
7.	What do you understand by feature creep?	BTL 1	Remember
8.	Name the hardware requirements of STB.	BTL 1	Remember
9.	List the major components in the PDA systems.	BTL5	Evaluate
10.	Assess the use of exponential back off technique?	BTL5	Evaluate
11.	Point out the need for hardware and software Co –design.	BTL2	Understand
12.	Compare Hardware and software Co – Design.	BTL4	Analyze
13.	Why most designers use FOSS tools in embedded system development?	BTL4	Analyze
14.	Enumerate the advantages of Set Top Box.	BTL 1	Remember
15.	Mention the skills required to design a set top box.	BTL6	Create
16.	How do you define a software modem?	BTL3	Apply
17.	Summarize the advantages and limitations of SOS.	BTL2	Understand
18.	What are the methods for testing a software modem?	BTL3	Apply
19.	Enumerate the function of lossy data compression.	BTL6	Create
20.	What are the different categories of program design for data compressor?	BTL3	Apply
PART –B			
1.	Discuss how the System Integration and testing is done while designing a	BTL4	Analyze

	software modem. (13)		
2.	With necessary diagrams, explain the embedded Hardware and software co – design. (13)	BTL 1	Remember
3.	(i)Explain how Personal Digital Assistant device is designed. (10) (ii)Point out the features of PDA device. (3)	BTL 1	Remember
4.	(i)Provide the general design challenges of SOS. (10) (ii)List out the advantages and disadvantages of SOS. (3)	BTL1	Remember
5.	(i)What are the problems that arise in Co design? (4) (ii)Write Short notes on Open source software tools used in embedded system. (9)	BTL2	Understand
6.	Annotate in detail about the specification, component design and test of an embedded system that use FSK technique? (13)	BTL5	Evaluate
7.	(i)Demonstrate the role of a Set Top Box along with its Hardware and software design. (5) (ii)Write Short notes on PDAs. (8)	BTL4	Analyze
8.	Outline the embedded concepts in the design of data compressor. (13)	BTL2	Understand
9.	(i)What is the need for Hardware and Software Co design? (5) (ii)Summarize the concepts of design of Set Top Box. (8)	BTL3	Apply
10.	(i)Justify through two features on how system on chip design is useful. (3) (ii)Enumerate some of the FOSS tools for embedded system development and explain. (10)	BTL1	Remember
11.	Starting from the requirement analysis, design an alarm clock covering all the phases of EDLC. (13)	BTL 6	Create
12.	Narrate in detail about the embedded concepts to design a Telephone answering machine. (13)	BTL3	Apply
13.	Design a Video accelerator as an example of accelerated embedded system. (13)	BTL4	Analyze
14.	With neat sketches and UML diagrams, explain the specifications, design and functionalities of a data compressor. (13)	BTL2	Understand
PART C			
1.	Describe in detail about the principle of operation of software modem? (15)	BTL 6	Create
2.	Illustrate the design of Data Compressor with neat diagram. (15)	BTL5	Evaluate
3.	Create the design flow of the hardware /software co-design approach. (15)	BTL 6	Create
4.	With neat diagram, explain the hardware and software architecture of a Personal Digital Assistants (PDA). (15)	BTL5	Evaluate