SRM VALLIAMMAI ENGINEERING COLLEGE

(AN AUTONOMOUS INSTITUTION, AFFILIATED TO ANNA UNIVERSITY)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

I SEMESTER

1912102 – ADVANCED COMPUTER ARCHITECTURE

Regulation – 2019

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SUBJECT : 1912102 – ADVANCED COMPUTER ARCHITECTURE

SEM / YEAR : I / I

UNIT I - FUNDAMENTALS OF COMPILER DESIGN AND ILP			
Fundamentals of Mother Board architecture – CPU socket–Fan and Heat Sink mounting point-Power connector–DRAM- PCI slot–CMOS–Connectors and Integrator–Computer Design –Measuring and Reporting Performance –Instruction Level Parallelism and its Exploitation –Concepts and Challenges –Exposing ILP -Advanced Branch Prediction – Dynamic Scheduling -Exploiting ILP -Instruction Delivery and Speculation -Limitations of ILP.			
PART-A (2 - MARKS)			
Q. No	**QUESTIONS**	**BT Level**	**Competence**
1.	**Write** the features of Mother Board Architecture.	Remember	BTL-1
2.	**Demonstrate** your understanding about CPU socket Fan.	Apply	BTL-3
3.	**Examine** the reason behind heatsink and fan mounted on CPU.	Apply	BTL-3
4.	**Differentiate** between Port and Connector.	Understand	BTL-2
5.	**List** the advantages of using DRAM for main memory.	Remember	BTL-1
6.	**Explain** the role of Conventional PCI.	Evaluate	BTL-5
7.	**Identify** the CMOS Applications.	Remember	BTL-1
8.	**Analyse** the graphic model of Computer Design.	Analyze	BTL-4
9.	**Summarize** the pros and cons of iterative software development model?	Evaluate	BTL-5
10.	**Define** the factors that affect the performance of a computer.	Remember	BTL-1
11.	**List** the two approaches to Instruction Level Parallelism.	Remember	BTL-1
12.	**Compare** Instruction level parallelism and machine parallelism.	Analyze	BTL-4

13.	**Predict** about ILP challenges.	Understand	BTL-2
14.	**Discuss** about static and Dynamic Technique.	Understand	BTL-2
15.	**Generalize** about basic pipelining scheduling.	Create	BTL-6
16.	**Show what** is meant by Dynamic scheduling ?	Apply	BTL-3
17.	**Differentiate** Forwarding and Bypassing technique**.**	Analyze	BTL-4
18.	**Create** a scenario for giving an example of data dependencies**.**	Create	BTL-6
19.	**Summarize** the various types of dependencies.	Understand	BTL-2
20.	Why system engineers must understand the environment of a system? **Give** two reasons.	Remember	BTL-1
	PART-B (13- MARKS)		
1.	Define and list all the details of Mother board Architecture.(13)	Remember	BTL-1
2.	(i) **Explain** alteast one scenario where : a) Fan mounted on a CPU stops Working. (3) b) Heat coming from the CPU is controlled by the Fan. (3) (ii) **What** are the physical requirements for the I/O Device. (7)	Analyze	BTL-4
3.	(i) **What** do you mean by DRAM Technology and memory performance inside it? (6) (ii) **Explain** in detail about PCI slot with an example. (7)	Remember	BTL-1
4.	(i) **Write** short notes on: a) CMOS (3) b) Integrators (3) (ii) **Explain** in detail about the Computer Design. (7)	Evaluate	BTL-5
5.	(i) **What** is the procedure for measuring and reporting the performance of the computer ? (6) (ii) **Describe** how the connectors are used with a specific diagram. (7)	Understand	BTL-1
6.	(i) **Compare** SRAM and DRAM. (6) (ii) **Discuss** about the following problem: The microprocessors today are designed to have adjustable voltage, so that a 15% reduction in voltage may result in a 15% reduction in frequency. What would be the impact on dynamic power? (7)	Analyze	BTL-4

7.	**Explain** in Detail with the help of an example about Dynamic Scheduling with Renaming.	Analyze	BTL-4
8.	**Discuss** in detail about Loop Unrolling with the help of an example.	Understand	BTL-2
9.	**Discuss** about how the pipelining scheduling is done with the help of an example.	Understand	BTL-2
10.	**Illustrate** in detail about the pipelining obstacles.	Apply	BTL-3
11.	**Describe** the mechanism to handle dependencies.	Understand	BTL-2
12.	**Generalize** the dependencies in pipelined processor.	Create	BTL-6
13.	**Describe** the compiler techniques for exposing ILP.	Remember	BTL-1
14.	**Explain** in detail about the shortcomings in ILP.	Apply	BTL-3
PART-C (15- MARK)			
1.	**Summarize** in details about the various dependences causes in ILP and the limitations of ILP.	Evaluate	BTL-5
2.	**Hypothesize** how the Hardware based Speculation is used to overcome control Dependence**.**	Create	BTL-6
3.	Suppose that we are Considering an enhancement to the processor of a server system used for Web Serving. The new CPU is 10 times faster on computation in the Web serving application than the original processor Assuming that the original CPU is busy with computation 40% of the time and is waiting for I/O 60% of the time, **Infer** the overall speedup gained by incorporating the enhancement.	Analyze	BTL-4
4.	**Rewrite** a common transformation required in graphics engines in square root. Implementation of floating-point square root vary significantly in performance, especially among processors designed for graphics .Suppose FP square root is responsible for 20% of the execution time of a critical graphics benchmark one proposal is to enhance FPSQR hardware. And speedup this operation by a factor of 10. The other alternative is just to try to make all FP instructions in the graphics processor run faster by a factor of 1.6.FP instructions are responsible for total of 50% of the execution time for the applications. The design team believes that	Create	BTL-6

	they can make all FP instructions run 1.6 times faster with the same effort as required for the fast square root. Compare these two design alternatives.		

UNIT II- MEMORY HIERARCHY DESIGN

Introduction –Optimizations of Cache Performance –Memory Technology and Optimizations –Protection: Virtual Memory and Virtual Machines –Design of Memory Hierarchies.

PART-A (2 - MARKS)

Q.No	QUESTIONS	BT Level	Competence
1.	**Give** the defination of the memory hierarchy.	Understand	BTL-2
2.	**Define** volatile memory.	Remember	BTL-1
3.	**Classify** memory hierarchy.	Apply	BTL-3
4.	Draw and **explain** the components in memory hierarchy.	Analyze	BTL-4
5.	**List** the characteristics of Memory hierarchy Design.	Remember	BTL-1
6.	**Define** Memory Access Time.	Remember	BTL-1
7.	How can address translation be avoided during the indexing of the cache's?	Apply	BTL-3
8.	**Develop** memory hierarchy using a diagram.	Create	BTL-6
9.	**Differentiate** magnetic disk and magnetic tape.	Understand	BTL-2
10.	**Point out** the advantages of memory hierarchy	Analyze	BTL-4
11.	**Distinguish** hardware based prefetching and compiler based prefetching.	Understand	BTL-2
12.	**List** the techniques that can be used to reduce miss penalty and miss rate.	Remember	BTL-1
13.	**Classify** the classical components of computer.	Analyze	BTL-4
14.	**Express** CPI.	Understand	BTL-2
15.	**Explain** Principle of Locality.	Evaluate	BTL-5
16.	**What** is hit time and miss penalty?	Remember	BTL-1
17.	**Classify** two ways in which virtual machine is handled.	Apply	BTL-3
18.	**Define** Virtual Memory Machine.	Remember	BTL-1
19.	**Explain** Page based virtual memory**.**	Evaluate	BTL-5
20.	**Generalize** Protection in Virtual Machines.	Create	BTL-6

PART-B (13- MARK)			
1.	(i) **Differentiate** between Private and Shared Memory. (7) (ii) **Give** the techniques to reduce the hit time. (6)	Understand	BTL-2
2.	**Express** in detail about the optimizations of cache performance (13)	Understand	BTL-2
3.	(i) **List** and **explain** Memory Hierarchy . (7) (ii) **List** the memory technologies used in Computer Architecture(6)	Remember	BTL-1
4.	(i) **Demonstrate** the Protection in virtual memory. (7) (ii) **Show** the Protection in Virtual Machine. (6)	Apply	BTL-3
5.	(i) **Explain** in detail about Xen Architecture. (7) (ii) **Describe** SRAM and DRAM technologies used in memory. (6)	Remember	BTL-1
6.	**Analyze** about the Technology Trends. (13)	Analyze	BTL-4
7.	(i) **Pointout** the way Prediction to reduce Hit Time. (2) (ii) State DIMM. (4) (iii) **List** the benefits of using VMs. (4) (iv) **Elaborate** the concept of Virtualization. (3)	Remember	BTL-1
8.	**Assess** how Pipelined Cache Access used to Increase Cache Bandwidth. (13)	Evaluate	BTL-5
9.	(i) **What** is Flash Memory? (4) (ii) **How** will you classify the soft errors? (5) (iii) **List** the techniques used to reduce miss Penalty. (4)	Create	BTL-6
10.	**List** the levels in a typical memory hierarchy. (13)	Remember	BTL-1
11.	(i) **Classify** Cache Optimizations. (7) (ii) **Demonstrate on** Role of Blocking Factor. (6)	Apply	BTL-3
12.	(i) **Discuss** about Sequential Interleaving. (7) (ii) **Describe** about the Graphic Data RAM's. (6)	Understand	BTL-2
13.	(i) **Analyze** the ways for improving Memory Performance Inside a DRAM Chip. (6) (ii) **Explain** about 3 C's of Cache Miss. (7)	Analyze	BTL-4
14.	(i) What is the purpose of Enhancing Dependability in Memory Systems. (7)	Analyze	BTL-4

	(ii) **Explain** the concept of Merging Write Buffer used to Reduce Miss Penalty. (6)		
PART-C (15 -MARKS)			
1.	(i) **Summarize** the segmented virtual memory protections with suitable example. (7) (ii) **Evaluate** the 3 C's of Cache Miss. (8)	Evaluate	BTL-5
2.	(i) **Compile** the various hit time reduction techniques for improving the cache performance. (8) (ii) **Formulate** the various Compiler Optimizations to Reduce Miss Rate. (7)	Create	BTL-6
3.	Assume that L2 has a block size four times that of L1.**Analyze** how a miss for an address that causes a replacement in L1 and L2 can lead to violation of the inclusion property.	Analyze	BTL-4
4.	(i) **Write** note on Intel core i7 architecture. (8) (ii) **Generalize** the techniques for reducing cache miss penalty. (7)	Create	BTL-6
UNIT III- MULTIPROCESSOR ISSUES			
Introduction- Centralized, Symmetric and Distributed Shared Memory Architectures – Cache Coherence Issues –Performance Issues –Synchronization –Models of Memory Consistency - Interconnection Networks –Buses, Crossbar and Multi-stage Interconnection Networks			
PART-A (2 - MARKS)			
1.	**Express** cache coherence.	Understand	BTL-2
2.	**Discuss** serialization	Understand	BTL-2
3.	**Define** Distributed shared memory	Remember	BTL-1
4.	**List** cache coherence protocol	Remember	BTL-1
5.	**Describe** interconnection network	Understand	BTL-2
6.	**Differentiate** Buses from crossbar networks.	Understand	BTL-2
7.	**What** is a Multistage interconnection network?	Remember	BTL-1
8.	**Summarize** snooping coherence protocols	Evaluate	BTL-5
9.	**Examine** about invalidate protocol.	Remember	BTL-1
10.	**Write** short note on false sharing.	Create	BTL-6
11.	**Point** out load linked instruction.	Analyze	BTL-4
12.	**Illustrate** spin locks.	Apply	BTL-3
13.	**Evaluate** the concept of partial store order.	Evaluate	BTL-5
14.	**What** is the need of multiprocessor?	Remember	BTL-1

15.	**Discover** the two important hurdles which make parallel processing challenging.	Apply	BTL-3
16.	**Explain** Coherent view of memory	Analyze	BTL-4
17.	**Name** the types of messages	Remember	BTL-1
18.	**Illustrate** the Factors affecting the two components of miss rate in cache performance.	Apply	BTL-3
19.	**Analyze** data-race-free.	Analyze	BTL-4
20.	**Formulate** the relaxed models.	Create	BTL-6
PART-B (13- MARKS)			
1.	(i) **Discuss** about the Distributed Shared Memory. (7) (ii) **List** the challenges of Parallel Processing in detail. (6)	Remember	BTL-1
2.	**Explain** Centralized Shared Memory Architectures. (13)	Evaluate	BTL-5
3.	**Analyze** the role of cache coherence in Multiprocessor . (13)	Analyze	BTL-4
4.	(i) **Demonstrate** the Cache Coherence Performance issues. (7) (ii) **Illustrate** in detail Snooping Coherence Protocols. (6)	Apply	BTL-3
5.	(i) **Give** the the Crossbar interconnection Networks. (6) (ii) **Discuss** the Multi-Stage Interconnection Networks. (7)	Understand	BTL-2
6.	(i) **List** Coherence and explain that the behavior of reads and writes to the same memory location, the memory system is coherent. (6) (ii)**Describe** Basic Schemes for Enforcing Coherence. (7)	Remember	BTL-1
7.	(i) **Discuss** the Cache Coherence Issues. (7) (ii) **Discuss** the Performance measurements of the Commercial workload. (6)	Remember	BTL-2
8.	**Describe** Performance measurements of the Multiprogramming and OS workload. (13)	Understand	BTL-2
9.	**Examine** Implementing Locks Using Coherence. (13)	Apply	BTL-3
10.	(i) **Analyze** Design Dimensions of Interconnection Networks. (6) (ii) **Explain** the Multistage Interconnection Networks. (7)	Analyze	BTL-4

11.	(i) **Describe** Multistage Interconnection Networks. (7) (ii) Explain the Bus Network. (6)	Remember	BTL-1
12.	(i) **Generalize** the key design dimensions for interconnection networks. (7) (ii) **Develop** a strategy that design the cache block in a directory based system and structure as the transition diagram for an individual cache. (6)	Create	BTL-6
13.	(i) **Analyze** Synchronization. (6) (ii) **Classify** Multicomputer from Multiprocessors. (7)	Analyze	BTL-4
14.	(i) **What** the Basic Hardware Primitives. (7) (ii) **Discuss** the Coherence Protocols. (6)	Remember	BTL-1
	PART-C(15 -MARKS)		
1.	(i) **Evaluate** the distributed memory architecture with different message passing mechanisms. (8) (ii) **Assess** the basic schemes for Enforcing Coherence. (7)	Evaluate	BTL-5
2.	(i) **Design** the directory-based cache coherence protocol (8) (ii) **Hypothesize** on how to implement synchronization Of processes in a multiprocessor using hardware primitive(7)	Create	BTL-6
3.	(i)Suppose we have an application running on a 32-processor multiprocessor, which has a 200 ns time to handle reference to remote memory. For this application, assume that all the reference except those involving communication hit in the loca memory hierarchy, which is slightly optimistic. Processors are stalled on a remote request, and the processor clock rate is 3. 3GHz. If the base CPI(assuming that all reference hit in the cache) is 0.5, **Point out** how much faster is the multiprocessor if there is no communication versus if 0.2% of the instructions involve a remote communication reference. (8) (ii) **Explain** in detail about limitation in Symmetric shared memory multiprocessors and snooping protocols. (7)	Analyze	BTL-4
4.	(i) A 40 MHz processor was used to execute a benchmark program with the following instructions mix and clock cycle counts. Instruction types Instruction Count Clock cycle count **Instruction types** **Instruction Count** **Clock Cycle Count** Integer arithmetic 45000 1	Create	BTL-6

	Data Transfer 32000 2 Floating Point 15000 2 Control Transfer 8000 2 Produce the effective CPI, MIPS rate and Execution time for this program. **Give** justification for each. (8) (ii) Assume that L2 has a block size four times that of L1.Show how a miss for an address that causes a replacement in L1 and L2 can lead to violation of the inclusion property. **Design** such Cache. (7)		

UNIT IV- MULTICORE ARCHITECTURES

Homogeneous and Heterogeneous Multi-core Architectures –Intel Multicore Architectures – SUN CMP architecture –IBM Cell Architecture. Introduction to Warehouse –scale computers- Architectures-Physical Infrastructure and Costs – Cloud Computing

PART-A (2 -MARKS)

1.	**Describe** the homogeneous multicore architecture.	Remember	BTL-1
2.	**Analyze** the SUN CMP architecture.	Analyze	BTL-4
3.	**Differentiate** between SMT and CMP.	Understand	BTL-2
4.	**Identify** scale computer.	Remember	BTL-1
5.	**Show** the categorization of Cloud Computing.	Remember	BTL-1
6.	**Measure** Chip Multithreading.	Evaluate	BTL-5
7.	**What** the Limitations of SUN Niagara Processor?	Remember	BTL-1
8.	**Poinout** the diagram of IBM Cell Architecture.	Analyze	BTL-4
9.	**What** do you mean by airside economization?	Remember	BTL-1
10.	**Summarize** the Power Utilization effectiveness.	Understand	BTL-2
11.	**Examine** short note on MapReduce.	Remember	BTL-1
12.	**Classify** the elements of Interconnect Bus.	Apply	BTL-3
13.	**Identify** important design factors for WSC.	Apply	BTL-4
14.	**Give** short note on Google File System.	Understand	BTL-2
15.	**Generalize** the Cooling and Power issues in the Google WSC.	Create	BTL-6
16.	**Examine** warehouse.	Apply	BTL-3
17.	**Show** the features of Multi-Core.	Apply	BTL-3
18.	**Generalize** between Homogeneous and heterogeneous multi-core architecture.	Create	BTL-6

19.	**Give** the the potential Drawbacks of Cloud Computing.	Understand	BTL-2
20.	**Assess** the role of Cloud Computing.	Evaluate	BTL-5
	PART-B (13- MARKS)		
1.	**Describe** the following topics: (i) Homogenous Multi-core architecture . (6) (ii) Hetrogeneous Multi-core architecture. (7)	Remember	BTL-1
2.	(i) **Explain** the SUN CMP architecture in detail. (7) (ii) **Analyze** Intel Multicore Architecture. (6)	Analyze	BTL-4
3.	(i) **Write** Cell Architecture (7) (ii) **Explain** the relation between Bus design and communication among the Cell. (6)	Remember	BTL-1
4.	**(i)** What do you mean by Warehouse-scale computers? **Tell** something about it. (7) (ii) **Give** a description a Batch processing framework. (6)	Understand	BTL-2
5.	(i) **Describe** the Computer Architecture of Warehouse-Scale Computers. (7) (ii) **Explain`** the Physical Infrastructure and Costs of Warehouse-Scale Computers (6)	Remember	BTL-1
6.	(i) **Summarize** the Efficiency of a WSC. (7) (ii) **Describe** the Capital expenditures (CAPEX). (6)	Understand	BTL-2
7.	(i) How would you **apply** Amazon Web Services to different applications ? (7) (ii) **Explain** the factors involved in Reducing Customer Risks and Economies of Scale. (6)	Apply	BTL-3
8.	**(i) Analyze** the Case Study- Google Warehouse-Scale Computer (7) **(ii) Explain** the customized and standardize 1AAA container for Google. (6)	Analyze	BTL-4
9.	(i) How will you **Support** the Servers in a Google WSC over others? (7) (ii) **Summarize** the Cooling and Power factors of the Google WSC (6)	Evaluate	BTL-5
10.	Write a **generalized** role of Networking in a Google WSC. (13)	Create	BTL-6

11.	(i) **Describe** the Monitoring and Repair elements of a Google WSC (7) (ii) **Explain** the Physical Infrastructure and Costs of Warehouse-Scale Computers (6)	Remember	BTL-1
12.	**Apprise and analyze** the cloud computing which is a model for enabling convenient, on-demand network access to a shared pool of configurable computing resources. (13)	Analyze	BTL-4
13.	(i) What is the Physical Infrastructure and Costs of Warehouse-Scale Computers? (7) (ii) **Summarize** the Measuring Efficiency of a WSC. (6)	Understand	BTL-2
14.	(i) **Explain** in detail the Computer Architectural details of Warehouse Scale Computers. (7) (iii) **Explain** a Heterogeneous Multi-core architecture (6)	Apply	BTL-3
	PART-C (15-MARKS)		
1.	(i) **Evaluate** the primary components of the instruction set architecture of VMIPS and explain the basic vector architecture with neat block diagram. (8) (ii) **Order** any five double-precision floating –point VMIPS vector instructions and explain its functions. (7)	Evaluate	BTL-5
2.	**Argue** the similarities and differences between the following (i) Vector architectures and GPUs. (8) (ii) Multimedia SIMD computers and GPUs. (7)	Evaluate	BTL-5
3.	(i) Suppose we have 8 memory banks with a bank busy time of 6 clocks and a total memory latency of 12 cycles. How long will it take to complete a 64-element vector load with a stride of 1? And with a stride of 32? **Create** the same. (8) (ii) **Explain** the Layer 3 network used to link arrays together and to the Internet (7)	Create	BTL-6
4.	**(i) Compile** the Batch processing framework. (8) **(ii) Explain** the important design factors for WSC. (7)	Create	BTL-6

UNIT V VECTOR, SIMD AND GPU ARCHITECTURES			
Introduction-Vector Architecture –SIMD Extensions for Multimedia –Graphics Processing Units –GPGPU Computing –Detecting and Enhancing Loop Level Parallelism- Case Studies- porting scientific applications.			
PART-A (2 -MARKS)			
1.	**Differentiate** between scalar and vector processors	Remember	BTL-1
2.	**Analyze** the Vector functional units.	Analyze	BTL-1
3.	**Assess** Thread block.	Evaluate	BTL-5
4.	**Contrast** scalar registers and Vector registers	Analyze	BTL-4
5.	**List** the definition of Graphics Processing unit?	Remember	BTL-1
6.	**Discuss** SIMD.	Understand	BTL-2
7.	**Give** Loop Level Parallelism.	Understand	BTL-2
8.	**Compare** on heterogeneous architecture and homogeneous architecture.	Evaluate	BTL-5
9.	**Predict** the issues in VMIPS.	Understand	BTL-2
10.	**Examine** short note on Vector Architecture.	Remember	BTL-1
11.	**Describe** the Vector execution time.	Remember	BTL-1
12.	**Give** GPGPU Computing.	Understand	BTL-2
13.	**Relate** on loop carried dependences.	Apply	BTL-3
14.	**Generalize** the improvements obtained with graphics processing units.	Create	BTL-6
15.	**List** the Structural hazards in vectored architecture.	Remember	BTL-1
16.	**Classify** the factors influencing the Vector Execution Time.	Analyze	BTL-4
17.	**Infer** the reasons for the usage of memory banks in vector processors.	Analyze	BTL-4
18.	**Explain** the vector-length register and maximum vector length.	Apply	BTL-3
19.	**Show** the important features of CPU and GPU.	Apply	BTL-3
20.	**Generalize** the output dependency.	Create	BTL-6
PART-B(13 MARKS)			
1.	(i) **Describe** Vector Architecture in detail. (7) (ii) **Identify** the need for SIMD Extension for multimedia. (6)	Remember	BTL-1
2.	(i) **Analyze** the basic Graphics processing Units. (7)	Analyze	BTL-4

	(ii) **Explain** the details of GPGPU computing. (6)		
3.	(i) **Write** about Detecting and Enhancing Loop Level Parallelism. (7) (ii) **Prepare** about Vector Length Registers and Vector Mask. Registers (6)	Create	BTL-5
4.	**Develop** in detail about Roofline Visual Performance model. (13)	Evaluate	BTL-6
5.	(i) **Summariz**e the elements of Graphics processing Units (6) (ii) **Discuss** in detail about NVIDIA GPU computational structures. (7)	Understand	BTL-2
6.	**Demonstrate** the factors in Eliminating dependent computations (13)	Apply	BTL-3
7.	**Describe** the primary components of the instruction set architecture of VMIPS.	Remember	BTL-1
8.	**Explain** the basic structure of a vector architecture VMIPS. (13)	Analyze	BTL-4
9.	**Discuss** the VMIPS functional units that consumes one element per clock cycle. (13)	Understand	BTL-2
10.	**Discuss** the concept of Multiple Lanes: Beyond One Element per Clock Cycle. (13)	Remember	BTL-1
11.	(i) **Explain** the details of handling Multidimensional Arrays in Vector Architectures. (7) (ii) **Analyse**. how to Handle Sparse Matrices in Vector Architectures. (6)	Analyze	BTL-4
12.	**Apply** the Programming features used for the Multimedia SIMD Architectures. (13)	Apply	BTL-3
13.	(i) **Predict** the Conditional Branching in GPUs. (7) (ii) **Give** the NVIDIA GPU Memory Structures	Understand	BTL-2
14.	(i) **Describe** the Innovations in the Fermi GPU Architecture. .(7) (ii) How to eliminate Dependent Computations? (6)	Remember	BTL-1

PART-C(15 MARKS)			
1.	**Prepare** the primary components of the instruction set architecture of VMIPS and explain the basic vector architecture with neat block diagram.	Create	BTL-6
2.	**Prepare** the similarities and differences between the following (i) Vector architectures and GPUs. (8) (ii) Multimedia SIMD computers and GPUs. (7)	Create	BTL-6
3.	(i) A design choice is to be made in enhancing a processor. One option is to invest in additional hardware that works at twice the speed which will be benefit 60% of the program. The other is to keep the hardware simple, but invest in compiler optimization, which provides varying benefits for different programs. 40% of the programs can be speeded up by a factor 2, while 30% of the programs can be speeded up by a factor 3. Which option would be better? **Evaluate** a solution to this. (8) (ii) **Develop** any four multicore architectures which you have studied , analyze the advantages and disadvantages and present a summary of it. (7)	Evaluate	BTL-5
4.	**Orde**r the issues in Eliminating Dependent Computations and Finding Dependences.	Evaluate	BTL-5