SRM VALLIAMMAI ENGINEERING COLLEGE

(AN AUTONOMOUS INSTITUTION, AFFILIATED TO ANNA UNIVERSITY)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

III SEMESTER

1912307 – EMBEDDED SOFTWARE DEVELOPMENT

Regulation – 2019

Academic Year 2021 - 22(ODD)

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QUESTION BANK

SUBJECT : Embedded Software Development
SEM / YEAR: III Semester / M.E – CSE II Year

UNIT I - EMBEDDED PROCESSORS			
Embedded Computers - Characteristics of Embedded Computing Applications - Challenges in Embedded Computing System Design - Embedded System Design Process- Formalism for System Design - Structural Description - Behavioural Description - ARM Processor - Intel ATOM Processor.			
PART - A			
Q.No	Questions	BT	Competence
1.	**Define** embedded computers.	BTL-1	Remember
2.	**Differentiate** CPU and platform in embedded computer.	BTL-2	Understand
3.	**Access** What is an embedded computer system?	BTL-5	Evaluate
4.	**Identify** the layers embedded computer system.	BTL-1	Remember
5.	**Show** the characteristics of embedded computing.	BTL-3	Apply
6.	**What** is the nature of embedded computing machines makes their design more difficult?	BTL-5	Evaluate
7.	**Summarize** about the costs of various sorts are also very important.	BTL-3	Apply
8.	**Why** use microprocessors?	BTL -1	Remember
9.	**Infer** the embedded computing systems have to provide sophisticated functionality.	BTL-4	Analyze
10.	**Generalize** to make things more difficult, embedded computing operations must often be performed to meet deadlines.	BTL-6	Create
11.	**State** and express the multirate.	BTL-2	Understand
12.	**Analyse** How much hardware do we need?	BTL-4	Analyze
13.	**Generalize** and define performance in embedded computing.	BTL-6	Create
14.	**What** are the typical non functional requirements?	BTL-1	Remember
15.	**Summarizes** the major steps in the embedded system design process.	BTL-1	Remember

16.	**Express** the requirements form that can be filled out at the start of the project.	BTL-2	Remember
17.	**What** are requirements might we have for our GPS moving map?	BTL-4	Analyze
18.	**Give** the object-oriented design emphasizes two concepts of importance	BTL-2	Understand
19.	**How** do we design for upgradability?	BTL-2	Understand
20.	**Show** what are the Object-oriented specification can be seen in two complementary ways?	BTL-3	Apply
PART – B			
1.	i) **How** did you describe Embedding Computers?(7) ii) **How** did you describe some of the microprocessors used in the BMW 850i? (6)	BTL-1	Remember
2.	**Summarize** in detail about BMW 850i brake and stability control system. (13)	BTL-2	Understand
3.	**Describe** in detail about i) **Challenges** in Embedded Computing System Design.(6) ii) **Characteristics** of Embedded Computing Applications.(7)	BTL-1	Remember
4.	**Can** you apply the facts to describe the embedded system design process. (13)	BTL-3	Apply
5.	**Compare** between typical non-functional requirements and sample requirements form. (13)	BTL-5	Evaluate
6.	**Explain** the Requirements analysis of a GPS moving map. (13)	BTL-4	Analyze
7.	**Discuss** about specification and architecture design the embedded system design process. (13)	BTL-2	Understand
8.	**Analyse** the characteristic of embedded computing applications. (13)	BTL-4	Analyze
9.	**Compose** and explain in detail about designing hardware and software components. (13)	BTL-6	Create
10.	**Examine** the formalisms for system design. (13)	BTL-1	Remember
11.	**Explain** the structural description and behavioral description. (13)	BTL-4	Analyze
12.	**Discuss** about the ARM processor with the help of an illustration. (13)	BTL-2	Understand
13.	**Describe** the Intel ATOM processor. (13)	BTL-1	Remember
14.	**Show** the signal, call, and time-out events in UML and a state machine specification in UML. (13)	BTL-3	Apply

PART-C

1.	**How** would you measure the execution speed of a program running on a microprocessor? You may not always have a system clock available to measure time. To experiment, write a piece of code that performs some function that takes a small but measurable amount of time, such as a matrix algebra function. Compile and load the code onto a microprocessor, and then try to observe the behaviour of the code on the microprocessor's pins. (15)	BTL-4	Analyze
2.	**Develop** a requirements description for an interesting device. The device maybe a household appliance, a computer peripheral, or whatever you wish. (15)	BTL-5	Evaluate
3.	**Write** a specification for an interesting device in UML. Try to use a variety of UML diagrams, including class diagrams, object diagrams, sequence diagrams, and so on (15)	BTL-6	Create
4.	**Draw** a state diagram for a behavior that sends the command bits on the track. The machine should generate the address, generate the correct message type, include the parameters, and generate the ECC. (15)	BTL-6	Create

UNIT II - EMBEDDED COMPUTING PLATFORM

CPU Bus Configuration - Memory Devices and Interfacing – Input / Output Devices and Interfacing - System Design - Development and Debugging – Emulator – Simulator - JTAG Design Example – Alarm Clock - Analysis and Optimization of Performance - Power and Program Size.

PART - A

Q.No	Questions	BT	Competence
1.	Define data registers.	BTL-1	Remember
2.	What are the Devices typically have several registers?	BTL-1	Remember
3.	Define compute the average memory access time.	BTL-1	Remember
4.	Discover the major steps in the process.	BTL-3	Apply
5.	Define page fault.	BTL-1	Remember
6.	Rank and list the ARM7 performs the following steps when responding to an interrupt.	BTL-5	Evaluate
7.	Draw the four-cycle handshake.	BTL-1	Remember
8.	Show the DMA requires the CPU to provide two additional bus signals.	BTL-3	Apply
9.	Generalize the a typical DMA controller includes the following three registers.	BTL-6	Create
10.	Differentiate SRAM and DRAM .	BTL-2	Understand
11.	Examine the DDR.	BTL-3	Apply

12.	Summarize the SIMMs and DIMMs.	BTL-2	Understand
13.	Summarize the gives a total transfer time in clock cycles.	BTL-2	Understand
14.	Access the Draw a timing diagram for a write operation with no wait states.	BTL-5	Evaluate
15.	Point out front panel of the alarm clock.	BTL-4	Analyze
16.	Give the times and data volumes in a burst bus transfer.	BTL-2	Understand
17.	Compose the steps to get the data from memory to the CPU.	BTL-6	Create
18.	Analyse the definition of state and timing modes.	BTL-4	Analyze
19.	Tell the classification of the system control module contains the following peripheral devices.	BTL-1	Remember
20.	Point out and define test-bench program and test bench.	BTL-4	Analyze
	PART - B		
1.	**Discuss** about i) Bus Protocols. (6) ii) System Bus Configurations. (7)	BTL-2	Understand
2.	**Summarize** the following uninformed i) Memory Device Organization. (6) ii) Random-Access Memories. (7)	BTL-5	Evaluate
3.	**i) Explain** in detail about CPU bus configuration. (6) ii) **Explain** assertions and queries in memory devices. (7)	BTL-4	Analyze
4.	**Relate** memory interfacing and device interfacing discuss in detail about the same. (13)	BTL-3	Apply
5.	(i) **Compose** what is touch screen? Explain input /output devices with example.(6) (ii) **Compose** the memory device and interface.(7)	BTL-6	Create
6.	(i) **Explain** the LED connected to a digital output with an example. (7) (ii) Write a Cross section of a resistive touch screen. (6)	BTL-1	Remember
7.	(i) Write a short note with neat sketch in Touch screens with example.(7) (ii) Explain an n-digit display in detail. (6)	BTL-4	Analyze
8.	What is the cross-compiler? Explain in detail with example on development environments.(13)	BTL-1	Remember
9.	Describe the approach of debugging techniques with example. (13)	BTL-2	Understand
10.	(i) Explain the components of debugging challenges with example.(7) (ii) Briefly explain the development environments .(6)	BTL-1	Remember
11.	Explain Briefly design example with alarm clock. (13)	BTL-4	Analyze

12.	Draw a timing diagram that shows a complete DMA operation, including handing off the bus to the DMA controller, performing the DMA transfer, and returning bus control back to the CPU. (13)	BTL-2	Understand
13.	Explain power and program size with examples. (13)	BTL-1	Remember
14.	Show and explain Optimization of performance. (13)	BTL-3	Apply

PART-C			
1.	**Compose** draw a UML sequence diagram for a bus mastership request, grant, and return.(15)	BTL-6	Create
2.	(i) **Develop** the Class diagram for the alarm clock.(8) (ii**) State** with neat sketch Pre-processing button inputs.(7)	BTL-6	Create
3.	Explain the memory interfacing. Draw UML state diagrams for a bus master ship transaction in which one sideshows the CPU as the default bus master and the other shows the device that can request bus master ship.	BTL-4	Analyze
4.	Summarize about the following with examples (i) Design example with alarm clock (8) (ii) Development environments (7)	BTL-5	Evaluate

UNIT-III EMBEDDED NETWORK ENIVIRONMENT

Distributed Embedded Architecture - Hardware And Software Architectures - Networks for Embedded Systems - I2C - CAN Bus - SHARC Link Supports – Ethernet – Myrinet – Internet - Network-based Design - Communication Analysis - System Performance Analysis - Hardware Platform Design - Allocation and Scheduling - Design Example - Elevator Controller.

PART - A

Q.No	Questions	BT Level	Competence
1.	Define PEs.	BTL-1	Remember
2.	What is meaning of embedded system?	BTL-1	Remember
3.	Show what is hardware platform?	BTL-3	Apply
4.	Why is an embedded system important?	BTL-5	Evaluate
5.	Represent the advantage of this fact when analyzing network performance?	BTL-3	Apply
6.	Define network abstractions.	BTL-1	Remember
7.	Which software is used for embedded system?	BTL-4	Analyze
8.	Which language is used in embedded system?	BTL-2	Understand
9.	How do you diagnose a CAN bus system?	BTL-1	Remember
10.	Is CAN bus digital or analog?	BTL-5	Evaluate
11.	Define the feature of SHARC.	BTL-3	Understand

12.	What is the fieldbus?	BTL-4	Analyze
13.	What are the Internet provides a standard way for an embedded system?	BTL-6	Create
14.	State the single-hop network.	BTL-2	Understand
15.	What is critical analysis in communication?	BTL-2	Understand
16.	How do you evaluate the performance of embedded computing?	BTL-6	Apply
17.	State Is real-time scheduler in embedded system?	BTL-4	Analyze
18.	Write the elevator system.	BTL-2	Create
19.	List the scheduling in embedded systems?	BTL-1	Remember
20.	Show the purpose of hardware platform.	BTL-1	Remember
PART - B			
1.	Explain the detail with neat sketch distributed embedded system .(13)	BTL-1	Remember
2.	What are the steps for network abstractions? Explain each step. (13)	BTL-3	Apply
3.	Explain the hardware and software architectures with an example. (13)	BTL-4	Analyze
4.	**Explain** the signal processing system built from print-to-point links in detail with example. What is the need format of a typical message on a bus? (13)	BTL-2	Understand
5.	**Discuss** in detail with sketch crossbar network and multistage network.(13)	BTL-4	Analyze
6.	**Describe** the steps involved in the Message Passing Programming with example in Data-push network architectures. (13)	BTL-5	Evaluate
7.	**Summarize** the networks for embedded systems (13)	BTL-2	Understand
8.	**Explain** format of an I^2C address transmission. (13)	BTL-1	Remember
9.	**Write** a short note on the I^2C Bus and Electrical interface to the I^2C bus. (13)	BTL-6	Create
10.	**Explain** briefly I^2C interface in a microcontroller and Transmitting a byte on the I^2C bus. (13)	BTL-1	Remember
11.	i) Let's **assume** that our I^2C bus runs at the rate of 100KB/s and that we need to send one 8-bitbyte. Based on the message format, we can compute the number of bits in the complete packet ii) **Generalize** about multihop communication (13)	BTL-4	Analyze
12.	i). **Discuss** the general-purpose of Ethernet is very widely used as a local area network.(6) ii).Explain the typical bus transactions on the I^2C bus.(7)	BTL-2	Understand
13.	i) **How** did you describe theory of operation and requirements in elevator controller (6)? ii) **How** would you identify an example for Physical interface classes for the elevator system? (7)	BTL-1	Remember
14.	i) **Illustrate** the basic class diagram for the elevator system with detail notes.(8) ii) **Write** short note on the networks in the elevator. (5)	BTL-3	Apply

PART-C			
1.	**What** is the longest time that a processing element may have to wait between two successive data transmissions on a round-robin arbitrated bus? Assume that each data transmission requires one time unit.(15)	BTL-4	Analyze
2.	**How** can an automotive network ensure that safety-critical components are not starved of bus access—that they are guaranteed to be able to transmit within a certain amount of time? (15)	BTL-5	Evaluate
3.	**Give** an example of a simple protocol that would allow sensor nodes in a sensor network to determine the other nodes with which they can communicate.(15)	BTL-6	Create
4.	**Summarize** about the design example elevator controller with neat sketch.(15)	BTL-6	Create

UNIT IV - REAL-TIME CHARACTERISTICS			
Clock Driven Approach - Weighted Round Robin Approach - Priority Driven Approach - Dynamic versus Static Systems - Effective Release Times and Deadlines - Optimality of the Earliest Deadline First (EDF) Algorithm - Challenges in Validating Timing Constraints in Priority Driven Systems - Off-Line versus On-Line Scheduling.			
PART - A			
Q.No	**Questions**	**BT Level**	**Competence**
1.	Define clock-driven approach .	BTL-1	Remember
2.	Articulate the difference between clock-driven scheduler and cyclic scheduler explain in detail.	BTL-3	Apply
3.	Illustrate the Time driven scheduling in real time.	BTL-1	Analyze
4.	Write the priority driven scheduling.	BTL-6	Create
5.	Summarize the round robin in embedded system.	BTL-2	Understand
6.	Pivot the round robin scheduling explain with example.	BTL-6	Create
7.	Identify the use of weighted round-robin approach.	BTL-1	Remember
8.	Describe the weighted round-robin approach.	BTL-1	Remember
9.	Define priority-driven approach	BTL-1	Remember
10.	Conclude the algorithm for priority based scheduling.	BTL-4	Remember
11.	Solve the dynamic versus static systems.	BTL-3	Apply
12.	Summarize the embedded system has a deadline for each task.	BTL-2	Understand
13.	Classify the type of embedded system can miss deadlines to complete the task.	BTL-2	Understand
14.	Defend the process misses a deadline in embedded systems	BTL-5	Evaluate
15.	Define effective release time	BTL-1	Remember
16.	How effective release times and deadlines are useful in real-time scheduling?	BTL-5	Evaluate
17.	Interpret the period and release time in RTS.	BTL-2	Understand
18.	Illustrate the effective release time and effective deadline.	BTL-4	Analyze
19.	Judge the EDF as a dynamic priority scheduling algorithm for real-time tasks.	BTL-4	Analyze
20.	Solve the EDF scheduling adopts dynamic scheduling policy.	BTL-3	Apply
PART - B			
1.	**What** are characteristics of real-time systems? Difference between FCFS and SJF CPU scheduling algorithms.(13)	BTL-1	Remember
2.	**Write** briefly on clock driven approach and weighted round robin approach.(13)	BTL-2	Understand

3.	**Write** a short note on priority driven approach and clock driven approach with examples. (13)	BTL-4	Analyze
4.	**Define** real time embedded system. Write a short note on dynamic versus static system.(13)	BTL-1	Remember
5.	**Explain** weighted round robin approach in detail. Difference between dynamic versus static system (13)	BTL-1	Remember
6.	**Explain** effective release times and deadlines in detail with real time example. (13)	BTL-5	Evaluate
7.	**Narrate** optimality of the earliest deadline first algorithm in detail. Heavy traffic analysis for EDF ueues with reneging (13)	BTL-2	Understand
8.	**Briefly explain** on EDF (i). Deadline interchange (4) (ii). Heavy traffic analysis for EDF queues with reneging (3) (iii). Comparison with Fixed-priority schedulers(3) (iv). Kernels implementing EDF scheduling (3)	BTL-6	Create
9.	What is online scheduling and offline scheduling? With diagrammatic representation, explain in off line versus online scheduling detail.(13)	BTL-3	Apply
10.	**Compare** and contrast about the dynamic versus static system and effective release times and deadlines.(13)	BTL-4	Analyze
11.	Examine the challenges in validating timing constraints in priority driven systems.(13)	BTL-4	Analyze
12.	Describe the optimality of the EDF algorithm and clock driven approach.(13)	BTL-2	Understand
13.	Explain about online scheduling in real time system. List the type of scheduling is used in real life operating systems Why?(13)	BTL-1	Remember
14.	How do you execute the planning in solving problems in challenges in validating timing constraints in priority driven systems and anomalous behavior of priority –driven systems with neat sketch ? (13)	BTL-3	Apply

PART-C			
1	Create and design the architecture of challenges in validating timing constraints in priority driven systems and anomalous behavior of priority –driven systems with neat sketch. (15)	BTL-6	Create

2.	Explain about the off line versus online scheduling . (15)	BTL-5	Evaluate
3.	Develop the optimality of the earliest deadline first algorithm . (15)	BTL-6	Create
4.	Analyse about the weighted round robin approach, priority driven approach and explain it. (15)	BTL-4	Analyze

UNIT V - SYSTEM DESIGN TECHNIQUES

Design Methodologies - Requirement Analysis – Specification - System Analysis and ArchitectureDesign - Quality Assurance - Design Examples - Telephone PBX - Ink jet printer - Personal Digital Assistants - Set-Top Boxes

PART - A

Q.No	Questions	BT Level	Competence
1.	**List** the design process has several important goals.	BTL-1	Remember
2.	**Define** design flow.	BTL-1	Remember
3.	**Illustrate** the design methodologies.	BTL-4	Analyze
4.	**Summarize** the waterfall model.	BTL-2	Understand
5.	**Draw** the successive refinement development model.	BTL-2	Understand
6.	**Solve** the simple hardware/software design methodology.	BTL-3	Apply
7.	**Judge** the use of Concurrent engineering	BTL-5	Evaluate
8.	**Articulate** the elements of Concurrent product realization in Concurrent engineering	BTL-3	Apply
9.	**Discover** a good set of requirements should meet one tests verifiability in requirements analysis?	BTL-3	Understand
10.	**Illustrate** in requirements analysis for test in Traceability.	BTL-4	Analyze
11.	**Design** an OR state in state charts in control-oriented specification languages.	BTL-6	Apply
12.	**Defend** the AND/OR table are labelled with the basic variables in the expression.	BTL-5	Evaluate
13.	**Describe** the three major items that the methodology tries to identify	BTL-1	Remember
14.	**Classify** the steps when using it to analyze a system.	BTL-2	Create
15.	**Summarize** the quality assurance	BTL-2	Understand
16.	**Conclude** the five levels of maturity.	BTL-4	Analyze
17.	**Design** the cost of fixing bugs grows over the course of the design process.	BTL-6	Create
18.	**Illustrate** the design of cyber-physical systems	BTL-1	Remember
19.	**Describe** the design review is a critical component of any QA process.	BTL-1	Remember

20.	**Identify** the problems listed in design reviews.	BTL-1	Remember
	PART - B		
1.	**Explain** the design methodologies in three of these goals are summarized detail with example.(13)	BTL-1	Remember
2.	i) **Describe** The waterfall model of software development in the Design Flows (6) ii) **Explain** the spiral model of software design in Design Flows(7)	BTL-1	Remember
3.	i) **Illustrate** the successive refinement development model in design flows (7) ii) **Conclude** the concept of simple hardware/software design methodology in design flows.(6)	BTL-4	Analyze
4.	**Explain** in detail notes with neat sketch the a hierarchical design flow for an embedded system (13)	BTL-1	Remember
5.	**Solve** the Concurrent engineering applied to telephone systems (13)	BTL-3	Apply
6.	i) **Categories** the types of requirements (3) ii) **Conclude** the A good set of requirements should meet several tests in requirement analysis.(10)	BTL-4	Analyze
7.	**Write** notes on control-oriented specification languages.(13)	BTL-5	Evaluate
8.	**Summarize** the steps when using it to analyze a system in system analysis and architecture design.(13)	BTL-2	Understand
9.	Explain the concept of Layout of a CRC card in detail.(13)	BTL-2	Understand
10.	i) **Write** the CRC card analysis of the elevator system of basic set of classes. (8) ii) **Pivot** the several usage scenarios define the basic operation of the elevator system.(5)	BTL-6	Create
11.	**Conclude** about quality management based on ISO 9000 in quality assurance technique in details. (13)	BTL-4	Analyze
12.	i) **Classify** the five levels of maturity the CMM provides a model for judging an organization. (7) ii) **Summary** the verifying the specification in quality assurance.(6)	BTL-2	Understand
13.	Write detailed notes on the following i) Ink jet printer. (5) ii) Personal digital assistants. (4) iii) Set top boxes.(4)	BTL-1	Remember
14.	Solve the design reviews with neat sketch in quality assurance.(13)	BTL-3	Apply
	PART - C		
1.	i) Briefly **describe** the differences between the waterfall and spiral development models. (8)	BTL-6	Create

	ii) What skills might be useful in a cross-functional team that is responsible for designing a set-top box? (7)		
2.	i) **Estimate** the cost of finding and fixing a single software bug. (5) ii) **Defend** in details the Concurrent engineering applied to telephone systems.(10)	BTL-5	Evaluate
3.	i) **What** are the main phases of a design review? (5) ii) **Write** the details with neat sketch in the Therac-25 medical imaging system.(10)	BTL-6	Create
4.	**Analyse** about the quality assurance in design reviews and quality assurance techniques.(15)	BTL-4	Analyze