SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF INFORMATION TECHNOLOGY

(Common to Artificial Intelligence and Data Science)

QUESTION BANK

Academic Year 2022 – 2023

III SEMESTER

1908302-DIGITAL PRINCIPLES AND SYSTEM DESIGN

Regulation – 2019

CHOICE BASED CREDIT SYSTEM

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DEPARTMENT OF INFORMATION TECHNOLOGY

QUESTION BANK

SUBJECT : DIGITAL PRINCIPLES AND SYSTEM DESIGN

SEM / YEAR : III SEMESTER/ SECOND YEAR

UNIT I - BOOLEAN ALGEBRA AND LOGIC GATES

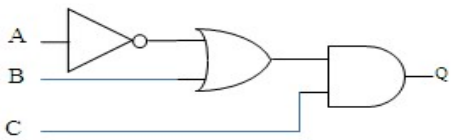
Number Systems - Arithmetic Operations - Binary Codes- Boolean Algebra and Logic Gates - Theorems and Properties of Boolean Algebra - Boolean Functions - Canonical and Standard Forms - Simplification of Boolean Functions using Karnaugh Map and Tabulation method - NAND and NOR Implementations.

PART-A

Q.no	Question	BTL	Competence
1	Find the octal equivalent of hexadecimal numbers of AB.CD (or) DC.BA	BTL5	Evaluating
2	Convert $(0.6875)_{10}$ to binary (or) Convert $(126)_{10}$ to Octal	BTL3	Applying
3	Convert $(1001010.1101001)_2$ to base 16 &$(231.07)_8$ to base 10	BTL3	Applying
4	Analyse the octal and hexadecimal equivalent of $(377)_{10}$.	BTL4	Analyzing
5	If $(123)_5 = (A3)_7$, then what is the value of A?	BTL5	Evaluating
6	Convert the binary $(1011111011)_2$ into gray code.	BTL3	Applying
7	Convert 143_{10} into its binary and binary coded decimal equivalent.	BTL2	Understanding
8	What is Excess-3 Code?	BTL1	Remembering
9	Show that Excess-3 code is self-complementing.	BTL2	Understanding
10	Write short notes on weighted binary codes.	BTL2	Understanding
11	State and prove the Consensus theorem.	BTL2	Understanding
12	State the principle of Duality.	BTL2	Understanding
13	Prove the following using DE Morgan's Theorem. [(X + Y)'+(X + Y) '] '=X + Y.	BTL5	Evaluating
14	Simplify Z = (AB +C) (B'D + C'E')+(AB+C)'	BTL4	Analyzing
15	Find the complement of the function F= X'YZ' + X'Y'Z.	BTL1	Remembering
16	Implement AND gate using only NOR gates. (or) Realize XOR gate using only NAND gates.	BTL6	Creating
17	Realize G = AB'C +DE+F'	BTL4	Analyzing
18	What are Universal Gates? Why are they named so?	BTL1	Remembering

19	Illustrate NOR Operation with a truth table	BTL2	Understanding
20	How many NOR gates are required if NAND gate is implemented using NOR.	BTL2	Understanding
21	What are the limitations of K-map?	BTL1	Remembering
22	Express the following Boolean expression in to minimum number of literals. XYZ+X'Y+XYZ'.	BTL5	Evaluating
23	Analyse the following Boolean functions using three variable maps. F(X, Y, Z) = ∑m(0,2,3,6,7).	BTL4	Analyzing
24	Express the Boolean Function F= A+B'C as sum of minterm (SOP).	BTL1	Remembering

PART-B

Q.no	Question	Mark	BTL	Competence
1(a)	Add, subtract and multiply the following numbers $(110010)_2$ and $(11101)_2$.	03	BTL1	Remembering
1(b)	State and prove De Morgan's theorems for 2-variables	04	BTL1	Remembering
1(c)	Find complement of the following Boolean expression xyz'+ x'yz + z(xy+w)	06	BTL1	Remembering
2	Evaluate: $(ABCD.1234)_{16}$ $= (?)_8$ $= (?)_{10}$ $= (?)_2 = (?)_{BCD}$ $= (?)_5$	03 03 04 05	BTL5	Evaluating
3(a)	Short notes on 1's and 2's complement	05	BTL1	Remembering
3 (b)	Explain the rules for Binary Addition and Subtraction using 1's & 2's complement. Give examples.	08	BTL5	Evaluating
4	Explain about common postulates used to formulate various algebraic structures.	13	BTL1	Remembering
5	Simplify the following switching function using karnaugh map method and realize expression using gates F(A,B,C,D) = ∑(0,3,5,7,8,9,10,12,15)	13	BTL2	Understanding
6	Examine how to minimize the function: F(A, B, C, D)=∑m(0,4,6,8,9,10,12) +∑d(2,13) and implement it using only NOR gates.	13	BTL 1	Remembering
7(a)	Simplify the Boolean function in Sum of Products(SOP) and Product of Sum(POS) F(w,x,y,z)=∑m(0,1,2,5,8,9,10).	08	BTL4	Analyzing
7(b)	Design the Boolean function in Karnaugh map and simplify it F(w,x,y,z)=∑m(0,1,2,4,5,6,8,9,12,13,14).	05	BTL6	Creating
8	Simplify the following Boolean expression in (a) Sum of Product (b) Product of Sum using Karnaugh map AC' + B'D + A'CD + ABCD.	06+07	BTL4	Analyzing
9(a)	Express the following function in sum of min-terms and product of max-terms: F(x,y,z)=x+yz.	08	BTL2	Understanding
9(b)	Convert the following logic system in to NAND gates only. 	05	BTL3	Applying

10(a)	Implement the following Boolean function with NAND-NAND logic F(A,B,C)= ∑m(0,1,3,5)	07	BTL6	Creating
10(b)	Define prime implicate and essential prime implicate.	04	BTL1	Remembering
10(c)	Convert $(78.5)_{10}$ into binary	02	BTL3	Applying
11(a)	Plot the logical expression: ABCD + AB'C'D' + AB'C + AB on a 4 variable K-map; obtain the simplified expression from the map	07	BTL 3	Applying
11(b)	Express the function Y = A + B'C in canonical SOP and canonical POS form.	06	BTL 3	Applying
12(a)	Explain the procedure for obtaining NOR- NOR circuit for any AND-OR network with a suitable example.	08	BTL5	Evaluating
12(b)	Simplify the given Boolean function in POS form using k-map F(A,B,C,D) =ΠM(0,1,4,7,8,10,12,15)+d(2,6,11,14)	05	BTL4	Analyzing
13	Simplify the following switching function using Quine Mc Cluskey method and realize expression using gates F(A,B,C,D) = ∑(0,5,7,8,9,10,11,14,15)	13	BTL3	Applying
14	Simplify the function F(w,x,y,z)=∑m(2,3,12,13,14,15) using Tabulation method. Implement the simplified function using gates.	13	BTL4	Analyzing
15	Minimize the following function using Karnaugh map F(A,B,C,D) = ∑m(0,1,2,3,4,5,6,11,12,13) and implement with logic gates.	13	BTL4	Analyzing
16	Minimize the expression using K-map and Quine Mccluskey method Y= A'BC'D + A'BC'D+ABC'D'+ABC'D'+AB'C'D+A'B'CD'	13	BTL2	Understanding
17(a)	Explain the procedure for obtaining NAND- NAND circuit for any AND-OR network with a suitable example.	08	BTL5	Evaluating
17(b)	Implement Y= (A'B+AB') (C+D') using NOR gates.	05	BTL3	Applying

PART-C

Q.no	Question	Mark	BTL	Competence
1(a)	Deduce $FACE_{16}$ in its binary, octal and decimal equivalent.	03	BTL 5	Evaluating
1(b)	Simplify the function F=xy+x'y'z'+x'yz'.	02		
1©	Interpret the logical expression using K-map in SOP and POS form : F (A, B, C, D) =∑m (0, 2, 3, 6, 7) + d (8, 10, 11, 15).	10		
2	Minimize the expression using K-map F=∑m(0,1,9,15,24,29,30) + ∑d (8,11,31**) (OR)** Reduce the expression using K-map $F(X_1,X_2,X_3,X_4,X_5)$ = ∑m(0,2,4,5,6,7,8,10,14,17,18,21,29,31) + ∑d(11,20,22)	15	BTL5	Evaluating
3	Express the following function in a simplified manner using K map Technique (i) G=πM(0,1,3,7,9,11). (ii) f(W,X,Y,Z)=∑m(0,7,8,9,10,12) + ∑d(2,5,13).	15	BTL6	Creating
4	Simplify the following function using five variable K- map F(A,B,C,D,E)=A'B'CE'+B'C'D'E'+A'B'D'+B'C'D'+A'CD+A'BD	15	BTL5	Evaluating
5	Simplify the following expression using Quine Mc Cluskey method & K map technique Y= $m_1+m_3+m_4+m_7+m_8+m_9+m_{10}+m_{11}+m_{12}+m_{14}$	15	BTL5	Evaluating

UNIT II - COMBINATIONAL LOGIC

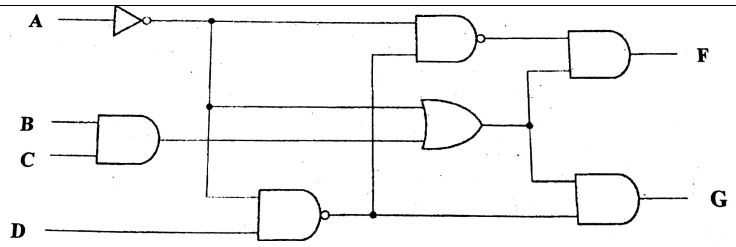
Combinational Circuits – Analysis and Design Procedures - Binary Adder-Sub tractor - Decimal Adder - Binary Multiplier - Magnitude Comparator - Decoders – Encoders – Multiplexers.

PART-A

Q.no	Question	BTL	Competence
1	Define combinational circuits	BTL1	Remembering
2	Mention the dependency of output in combinational circuits.	BTL4	Analysing
3	Obtain the truth table for BCD to Excess-3 code converter	BTL1	Remembering
4	Draw the full adder circuit as a collection of two half adders.	BTL3	Applying
5	Realize the combinational circuit of half subtractor.	BTL2	Understanding
6	What is half adder?. Draw the truth table of half adder	BTL1	Remembering
7	List the truth table of full subtractor.	BTL1	Remembering
8	Determine the exact number of half adders and full adders required for performing the addition of two binary numbers of 5 bits length each.	BTL 3	Applying
9	Write the Data flow description of a 4 bit comparator.	BTL2	Understanding
10	What is priority encoder?	BTL1	Remembering
11	Write short notes on propagation delay	BTL2	Understanding
12	Implement (solve) the function G=∑m (0, 3) using a 2x4 decoder.	BTL6	Creating
13	Draw the truth table and circuit diagram of 4 to 2 encoder.	BTL3	Applying
14	Differentiate between encoder and decoder.	BTL4	Analyzing
15	How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?	BTL6	Creating
16	Show the truth table of 2:1 MUX.	BTL 3	Applying
17	Implement (solve) a full adder with 4x1 multiplexer.	BTL2	Understanding
18	Draw (design) the circuit diagram for 2 to 1 line multiplexer.	BTL3	Applying
19	Implement (solve) the following Boolean function using 8:1 multiplexer F(A,B,C)=∑(1,3,5,6).	BTL5	Evaluating
20	Differentiate between Multiplexer and Demultiplexer.	BTL4	Analyzing
21	List out the application of multiplexer.	BTL1	Remembering
22	How many number of 2X1 multiplexers are required to implement 4x1 multiplexer.	BTL5	Evaluating
23	State the difference between decoder and demultiplexer.	BTL4	Analyzing
24	Give one application each for Multiplexer and Decoder.	BTL 1	Remembering

PART-B

Q.no	Question	Mark	BTL	Competence
1(a)	Explain the design procedure for combinational circuits with suitable examples	07	BTL5	Evaluating
1(b)	Explain the Analysis procedure. Analyse the following logic diagram.	06	BTL5	Evaluating

				
2	Design Full subtractor and derive expression for difference and borrow. Realize using two half subtractor.	13	BTL6	Creating
3	Design the full adder with inputs x,y,z and two outputs S and C. The circuits perform x+y+z is the input carry, C is the output carry and S is the Sum & realize it's using only NOR gates	13	BTL6	Creating
4	Design a 4 bit BCD to Excess-3 code converter.	13	BTL6	Creating
5	Describe the process involved in converting 8421 code to Excess 3 code with neat sketch.	13	BTL2	Understanding
6	Design a code converter for BCD to gray code conversion.	13	BTL6	Creating
7	Design a logic circuit that accepts a 4-bit gray code and converts it to 4-bit binary code	13	BTL6	Creating
8	Describe the procedure of converting 8421 to Gray code converter also realize the converter using only NAND gates.	13	BTL2	Understanding
9(a)	Recall the design procedure for binary multiplier	07	BTL1	Remembering
9(b)	Design a 2 bit binary multiplier to multiply two binary numbers and produce a 4-bit result.	06	BTL1	Remembering
10(a)	Construct a 4-bit odd parity generator circuit using gates	06	BTL3	Applying
10(b)	Construct a 5 to 32 line decoder using 3 to 8 line decoders and 2 to 4 line decoder.	07	BTL3	Applying
11	Find the design procedure for a 4 –bit parallel binary adder / subtractor.	13	BTL1	Remembering
12	With neat diagram explain the 4 bit adder with Carry look ahead.	13	BTL5	Evaluating
13(a)	Examine the following Boolean functions with a multiplexer. $F(W,X,Y,Z) = \sum (2,3,5,6,11,14,15)$	06	BTL4	Analyzing
13(b)	Implement the following function using 74LS138 and gates. $F1(A,B,C) = \Pi(0,1,3,7)$ and $F2(A,B,C) = \Pi(2,3,7)$	07	BTL2	Understanding
14(a)	Examine the following Boolean function using 8 to 1 Multiplexer. F(A,B,C,D)=A'BD' + ACD + B'CD + A'C'D.	06	BTL4	Analyzing
14(b)	Discover the above function using 16 to 1 Multiplexer.	07	BTL4	Analyzing
15	Define priority encoder and design 8 to 3 priority encoder	13	BTL1	Remembering
16	Implement the following function using multiplexer f(a,b,c,d)=	13	BTL6	Creating

	∑m(0,1,3,4,8,9,15)			
17	Draw the logic diagram of a 2-to-4 decoder using NOR gates only. Include an enable input.	**13**	**BTL 4**	**Analysing**

PART-C

Q.no	Question	Mark	BTL	Competence
1	Design a binary to gray code converter circuit &	15	BTL6	Creating
2	Design a BCD to 7- Segment code converter circuit	15	BTL6	Creating
3	Find the design procedure for a combinational circuit to perform BCD addition.	15	BTL6	Creating
4	How to design a 4 bit magnitude comparator with 3 outputs A>B,A=B,A<B	15	BTL2	Understanding
5a	Implement the following function using 8 to 1 multiplexer f(a,b,c,d)= ∑m(0,1,3,5,9,12,14,15)	07	BTL5	Evaluating
5b	Construct 16X1 multiplexer with two 8X1 and 2X1 multiplexer. Use Block diagrams	08	BTL3	Applying

UNIT III - SYNCHRONOUS SEQUENTIAL LOGIC

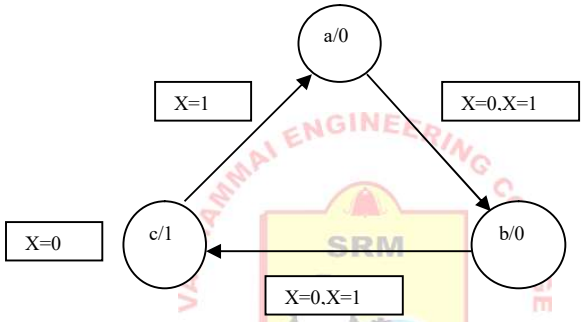
Storage Elements- Latches - Flip-Flops- Registers - Analysis and Design Procedure of Sequential Circuits - State Reduction and Assignment - Shift register - Sequence generator/detector- Counters.

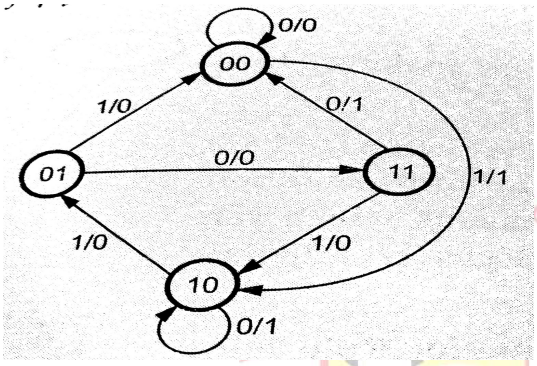
PART-A

Q.no	Question	BTL	Competence
1	Generalize the differences between combinational and sequential circuits.	BTL6	Creating
2	Summarize the characteristic table and equation of JK flip flop.	BTL2	Understanding
3	Construct the truth table and state diagram of SR Flip Flop.	BTL6	Creating
4	Draw the diagram of T- Flip flop and discuss its working.	BTL3	Applying
5	Give the characteristic equation and characteristic table of a T- flip-flop	BTL2	Understand
6	State the excitation table of JK-flip flop	BTL6	Creating
7	Differentiate between latches and flip flop.	BTL4	Analyzing
8	Give the excitation table for T Flip Flop.	BTL2	Understand
9	Realize a JK flip flop using D flip flop.	BTL3	Applying
10	Analyse how can a D FF can be converted into a T FF.	BTL4	Analysing
11	Select and list any two mechanisms to achieve edge triggering of flip flop	BTL2	Understanding
12	Give block diagram of Master -Slave D Flip flop.	BTL1	Remembering
13	Write down the steps involved in the design of synchronous sequential circuits.	BTL2	Understanding
14	What is shift register?	BTL1	Remembering
15	Classify the types of shift registers.	BTL4	Analyzing
16	Explain the difference between the performance of asynchronous and synchronous counter	BTL5	Evaluating
17	Design a 2 bit binary synchronous counter with D flip flops.	BTL6	Creating
18	Identify how many JK- flip-flops are required to design a MOD 35 counter?	BTL3	Applying
19	Analyse how many flip-flops are required to design a synchronous MOD 60 counter?	BTL4	Analyzing

20	Define Ripple counter	BTL1	Remembering
21	What is ring counter?	BTL1	Remembering
22	How many states are there in a 3-bit ring counter and list the states?	BTL5	Evaluating
23	State the rules for state assignment	BTL1	Remembering
24	What are the significances of state assignment?	BTL1	Remembering

PART-B

Q.no	Question	Mark	BTL	Competence
1	Implement T flip-flop using D flip-flop and JK using D flip flop.	13	BTL5	Evaluating
2(a)	Explain about synchronous and asynchronous sequential Circuit.	06	BTL3	Applying
2(b)	Explain the working procedure of 3 bit parallel- in serial-out shift register construct the state table.	07	BTL1	Remembering
3(a)	How a race condition can be avoided in a flip-flop.	06	BTL1	Remembering
3(b)	Realize the sequential circuit for the state diagram shown below. 	07	BTL4	Analyzing
4	Explain the different types of shift registers with neat diagram.	13	BTL2	Understanding
5(a)	What is meant by state diagram? Define how state assignment is important in a sequential circuit design. Describe with a suitable example.	07	BTL5	Evaluating
5(b)	Implement D and T FFs using JK flip flop. Tabulate the characteristics equation of the three flip flops.	06		
6	Draw the block diagram of Johnson counter and explain.	13	BTL5	Evaluating
7	Consider the design of a 4 bit BCD counter that counts in the following way: 0000 , 0010 , 0011 , ……. , 1001 , and back to 0000. (i) Draw the state diagram.(04) (ii) List the next state table. (04) (iii) Draw the logic diagram of the circuit.(05)	13	BTL3	Applying
8	Design a synchronous counter with the following sequence: 0, 1, 3, 7, 6, 4 and repeats. Use JK Flip flop.	13	BTL6	Creating
9	Design MOD 6 an asynchronous counter circuit	13	BTL6	Creating
10	Design a MOD-10 Synchronous counter using JK flip-flop. Write execution table and state table.	13	BTL6	Creating

11	Write the design procedure for a three-bit synchronous counter with T flip flop and draw the diagram. (OR) Write the design procedure for a 3-bit synchronous down counter using JK flip flop and draw the diagram.	13	BTL1	Remembering
12	Explain in detail about the working procedure of 4bit up/down counter.	13	BTL2	Understanding
13	Illustrate state diagram of T Flip-flop and construct it using JK Flip-flop. Explain about the excitation table and its application.	13	BTL2	Understanding
14	Explain the operation of master slave flip flop and show how the race around condition is eliminated in it.	13	BTL5	Evaluating
15	Design the sequential circuit specified by the following state diagram using T flip flops 	13	BTL6	Creating
16	Design a sequence detector to detect the input sequence 101(overlapping).Use JK Flip flops.	13	BTL6	Creating
17(a)	Analyse the difference between a state table, characteristic table and an excitation table.	03	BTL4	Analyzing
17(b)	Show the state transition diagram of a sequence detector circuit that detects '1010' from input data stream.	10	BTL 3	Applying

PART-C

Q.no	Question	Mark	BTL	Competence
1	Design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000 using D flip-flop.	15	BTL6	Creating
2	Design sequence detector that detects a sequence of three or more consecutive 1's in a string of bits coming through an input line and produces an output whenever this sequence is detected.	15	BTL6	Creating
3	A sequential circuit with two D flip-flops A and B, one input x , and one output z is specified by the following next state and output equations: A(t+1) = A'+B; B(t+1)=B'X; Z =A+B' (i)Draw the logic diagram of the circuit. (05) (ii)Derive the state table. (05) (iii)Draw the state diagram of the circuit. (05)	15	BTL5	Evaluating
4	Analyze and design a sequential circuit with two T Flip flop A and B, one input x and one output z is specified by the following next state	15	BTL6	Creating

	and output equation is A(t+1)= BX'+B'X B(t+1)=AB+BX+AX Z=AX'+A'B'X (i)Draw the logic diagram of the circuit (05) (ii) List the state table for the sequential circuit (05) (iii) Draw the Corresponding state diagram (05)			
5	A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations: A (t+1) = AX+BX; B (t+1) = A'X; Y= (A+B) X'. (i) Draw the logic diagram. (05) (ii) Construct the state table. (05) **(iii)** Draw the state diagram. (05)	15	BTL 6	Creating

UNIT IV- ASYNCHRONOUS SEQUENTIAL LOGIC

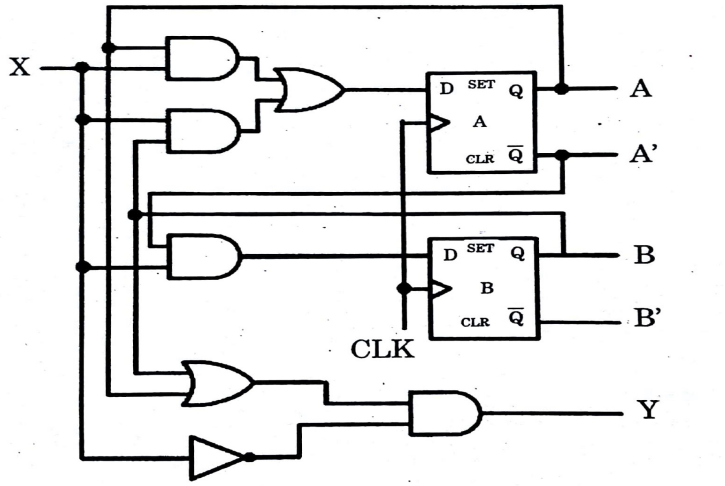
Analysis and Design of Asynchronous Sequential Circuits – Reduction of State and Flow Tables – Race-free State Assignment – Hazards.

PART-A

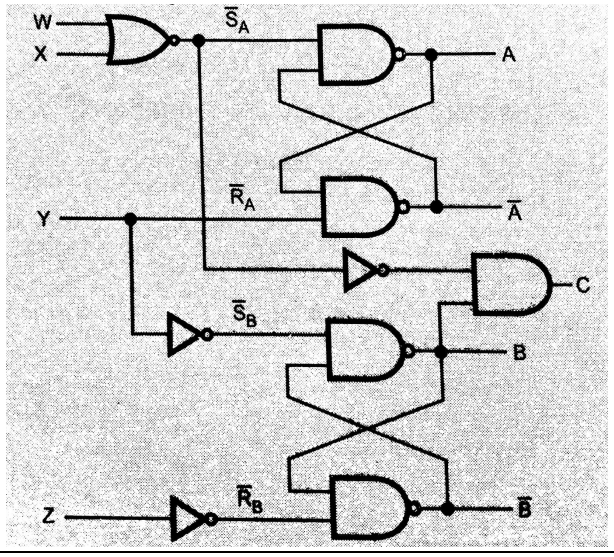
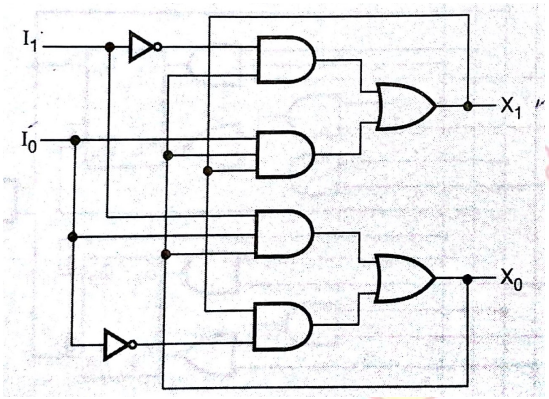
Q.no	Question	BTL	Competence
1	Point out the steps involved in the designing an asynchronous sequential circuits.	BTL1	Remembering
2	Compare asynchronous and synchronous sequential circuit.	BTL3	Applying
3	Summarize the advantages and disadvantages of asynchronous sequential circuits.	BTL5	Evaluating
4	Distinguish between fundamental mode circuit and pulse mode circuit.	BTL4	Analyzing
5	Define flow table in asynchronous sequential circuits	BTL1	Remembering
6	List the characteristics of fundamental mode circuit.	BTL2	Understanding
7	Define primitive flow table	BTL2	Understanding
8	Differentiate transition table and flow table.	BTL4	Analyzing
9	Differentiate conventional flow table and primitive flow table.	BTL4	Analyzing
10	How the Moore circuit differ from Mealy circuit?	BTL1	Remembering
11	Define race around conditions.	BTL1	Remembering
12	Define state reduction	BTL1	Remembering
13	What are race?	BTL2	Understanding
14	Is it essential to have race free assignment? Justify.	BTL5	Evaluating
15	Compare the critical race and non-critical race	BTL3	Applying
16	What is lockout? How it is avoided?	BTL2	Understanding
17	Show the diagram for debounce circuit.	BTL3	Applying
18	Define Merger graph.	BTL1	Remembering
19	Define hazards. What are the types of hazards?	BTL1	Remembering
20	Estimate the wave forms showing static 1 hazards	BTL6	Creating

21	State the difference between static 0 and static 1 hazard.	BTL4	Analysing
22	How can we change the hazards into hazards free circuit?	BTL5	Evaluating
23	Compare static and dynamic hazards.	BTL4	Analyzing
24	Design a hazard free circuit to implement the following function. F (A, B, C, D) = ∑m (1,3,4,5,6,7,9,11,15)	BTL 6	Creating

PART-B

Q.no	Question	Mark	BTL	Competence
1	Explain the steps for the design of asynchronous sequential circuits with an example.	13	BTL5	Evaluating
2	Discuss about Pulse mode & Fundamental mode asynchronous sequential circuits	13	BTL6	Creating
3	Discuss in detail the procedure for reducing the flow table with an example.	13	BTL6	Creating
4(a)	Explain the two types of asynchronous sequential circuit with suitable example.	06	BTL2	Understanding
4(b)	What is flow table? Explain with suitable example.	07	BTL1	Remembering
5	Analyze the following clocked sequential circuit and obtain the state equation and state diagram 	13	BTL4	Analyzing
6(a)	Describe the race free state assignment procedure.	05	BTL1	Remembering
6(b)	Reduce the number of state in the following state diagram. Tabulate the reduced state and draw the reduced diagram.	08	BTL3	Applying
7	Consider the asynchronous sequential circuits which is driven by the pulses, as in the following figure. Analyse the circuit	13	BTL4	Analyzing

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

				
8	Analyze the fundamental mode asynchronous sequential circuit given in the following figure. 	13	BTL4	Analyzing
9	Explain the minimization of primitive flow table with suitable examples.	13	BTL4	Analyzing
10	Design a circuit with inputs A and B to give an output Z=1 when AB=11 but only if A becomes 1before B, by drawing total state diagram, primitive flow table and output map in which transient state is included.	13	BTL6	Creating
11	Construct the switching function F=∑m(1,3,5,7,8,9,14,15) by a static hazard free two level AND-OR gate network.	13	BTL3	Applying
12	What are hazards and its types? How can you design a hazard free circuits, explain with example.	13	BTL1	Remembering
13(a)	What are static-0 and static-1 hazards? Show the removal of hazards using hazard covers in K-map.	07	BTL 3	Applying
13(b)	Examine cycles and races in asynchronous sequential circuits.	06		
14	Explain the hazards in combinational circuit and sequential circuit and also demonstrate a hazards and its removal with example.	13	BTL2	Understanding
15(a)	What is the objective of state assignment in asynchronous circuit? Explain how race to be avoided with an example.	06	BTL1	Remembering
15(b)	Summarize about static, dynamic and essential hazards in asynchronous sequential circuits	07	BTL2	Understanding
16	Consider an asynchronous sequential circuit described by			Understand

	$Y= x_1 x'_2 + (x_1 + x'_2)\, y$; $Z=Y$, where Y and Z are excitation and output functions respectively. **(i)** Give the logic diagram of the circuit. **(ii)** Interpret the transition table and output map. **(iii)** Obtain its flow table.	(03) (07) (03)	BTL 2	
17	Analyze a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z=1 it will remain so until A goes to 0. Draw the total state diagram, primitive flow table for designing this circuit.	13	BTL4	Analysing

PART-C

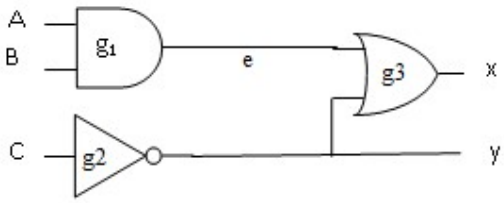
Q.no	Question	Mark	BTL	Competence
1	An asynchronous sequential circuit is described by the following excitation and output function**.** $Y=X_1X_2+(X_2+X_3)Y$ and $Z=Y$ i. Draw the logic diagram of the circuit. (06) ii. Derive the transition table and output map.(06) iii. Describer the behaviour of the circuit.(03)	15	BTL5	Evaluating
2	Design an asynchronous sequential circuit with inputs X1 and X2 and one output Z. Initially and at any time if both the inputs are 0, output is equal to 0.When X_1 or X_2 becomes 1, Z becomes 1. When Second input also becomes 1, Z=0; The output stays at 0 until circuit goes back to initial state.	15	BTL6	Creating
3	An asynchronous sequential circuit is described by the following excitation and output function. $X = (Y_1Z_1'W_2)X + (Y_1'Z_1W_2')$ & $S = X'$ (i) Draw the logic diagram of the circuit. (06) (ii) Derive the transition table and output map. (06) (iii) Describe the behavior of the circuit. (03)	15	BTL5	Evaluating
4	Design an asynchronous sequential circuit with two input x and y and with one output z whenever y is 1, input x is transferred to z. When y is 0, the output does not change for any change in x. Use SR latch for implementation of the circuit.	15	BTL6	Creating
5	Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows: $Y_1=x_1 x_2 +x_1y_2 +x_2y_1$ $Y_2=x_2+x_1y_1y_2 +x_1y_1$ $Z= x_2+y_1$ **(i)** Predict the logic diagram of the circuit**.** (04) **(ii)** Interpret the transition table and the output map. (07) **(iii)** Obtain its flow table. (04)	15	BTL 6	Creating

UNIT V - HDL & MEMORY AND PROGRAMMABLE LOGIC

Introduction to HDL – HDL Models of Combinational circuits and Sequential Circuits- RAM – Memory Decoding - ROM - Programmable Logic Array – Programmable Array Logic – Sequential Programmable Devices.

PART-A

Q.no	Question	BTL	Competence
1	Write any two advantages of HDL.	BTL1	Remembering
2	Name the modeling techniques available in HDL.	BTL1	Remembering
3	Write the HDL data flow description of 4 bit adder	BTL1	Remembering

4	Develop the HDL code to realize a D - flip flop	BTL2	Understanding
5	Determine the HDL description for the following circuit 	BTL1	Remembering
6	Write the VHDL code for a 2X1 multiplexer using behavioural modelling.	BTL5	Evaluating
7	Give the HDL code for half adder.	BTL2	Understanding
8	What is memory decoding?	BTL1	Remembering
9	What is volatile memory? Give example.	BTL1	Remembering
10	Differentiate between EEPROM and PROM.	BTL4	Analyzing
11	Compare DRAM and SRAM.	BTL5	Evaluating
12	Give the details about write and read operations in RAM.	BTL2	Understanding
13	Design the logic diagram of a memory cell.	BTL6	Creating
14	Develop the maximum range of a memory that can be accessed using 10 address lines.	BTL3	Applying
15	Draw the structure of PAL.	BTL1	Remembering
16	Demonstrate the function $F_1=\sum$ (0, 1, 2, 5, 7) and $F_2=\sum$ (1, 2, 4, 6) using PROM.	BTL3	Applying
17	Define PLA. How it differs from PROM?	BTL1	Remembering
18	Justify whether PAL is same as PLA.	BTL5	Evaluating
19	Write short notes on PLA.	BTL2	Understanding
20	Define combinational PLD.	BTL1	Remembering
21	Identify the comparison between EPROM and PLA	BTL3	Applying
22	Write down the different types of PLDs.	BTL2	Understanding
23	Differentiate between PLA and ROM.	BTL4	Analyzing
24	Differentiate error detection and correction technique.	BTL4	Analyzing

PART-B

Q.no	Question	Mark	BTL	Competence
1	Describe the modelling techniques available in HDL. Give the HDL code to realize a full adder using Behavioural modelling.	13	BTL2	Understanding
2	Summarize in detail the concept of structural modelling in HDL with an example of full subtractor	13	BTL2	Understanding
3	Analyze a full adder and half subtractor in data flow modelling using HDL. Explain in detail	13	BTL4	Analyzing
4	Write the HDL description of T flip-flop , JK flip-flop ,SR flip flop and D flip-flops	13	BTL1	Remembering
5(a)	Give the Internal block diagram of 4 x 4 RAM.	07	BTL2	Understanding
5(b)	Compare SRAM and DRAM.	06	BTL4	Analyzing
6	Implement the following using PAL F1(A,B,C)= ∑(1,2,4,6); F2(A,B,C) =∑(0,1,6,7) ; F3(A,B,C)= ∑(1,2,3,5,7)	13	BTL5	Evaluating
7	Design a combinational circuit using ROM that accepts a three bit	13	BTL6	Creating

	binary number and outputs a binary number equal to the square of the input number.			
8(a)	How to implement the two following Boolean functions using 8X2 PROM	05	BTL1	Remembering
8(b)	Construct the following two Boolean functions using PLA with 3 inputs, 4 Product terms, and 2 outputs. F1=∑m(3,5,6,7) and F2=∑m(1,2,3,4)	08	BTL3	Applying
9	Implement the following function using PLA A(X,Y,Z)=∑m(1,2,4,6), B(X,Y,Z)=∑m(0,1,6,7), C(X,Y,Z)=∑m(2,6)	13	BTL5	Evaluating
10	Explain in detail about the Programmable Logic Array & Programmable array logic.	13	BTL1	Remembering
11	Design a BCD to Excess 3 code converter and implement using suitable PLA.	13	BTL6	Creating
12	Draw a neat sketch showing implementation of Z1= ab'd'e + a'b'c'e+bc+de; Z2= a'c'e; Z3=bc+de+c'd'e+db and Z4=a'c'e +ce Using 5*8*4 PLA.	13	BTL3	Applying
13	Implement the following using PAL W(A,B,C,D) = ∑(0,2,6,7,8,9,12,13); X(A,B,C,D) =∑(0,2,6,7,8,9,12,13,14) ; Y(A,B,C,D) = ∑(2,3,8,9,10,12,13); Z(A,B,C,D)= ∑(1,3,4,6,9,12,14);	13	BTL5	Evaluating
14	List the features of PROM, PAL and PLA & Discuss the sequential programmable devices	13	BTL1	Remembering
15(a)	Compare PROM, PLA, PAL	07	BTL4	Analyzing
15(b)	Discuss the various types of RAM and ROM with architecture.	06	BTL2	Understanding
16(a)	Write the HDL gate level description of the priority encoder circuit.	06	BTL2	Understanding
16(b)	Briefly discuss the sequential programmable devices.	07	BTL2	Understanding
17(a)	Implement the following Two Boolean function with a PLA F1=AB'+AC'+A'BC' F2=(AC+BC+AB)'	05	BTL5	Evaluating
17(b)	A combinational logic circuit is generalized by the following function $F_1(A,B,C) = \sum m(0,1,6,7)$, $F_2(A,B,C) = \sum m(2,3,5,7)$. Assess the circuit with a PAL having three inputs, product terms and two outputs.	08	BTL 4	Analyzing
PART-C				
1	Design the following Boolean function using 8X2 PROM. F1=∑m(3,5,6,7) F2=∑m(1,2,3,4)	06	BTL6	Creating
2	Design a 16 bit RAM array (4X4 RAM) and explain the operation.	09	BTL6	Creating
3	Analyze a BCD to Excess-3 code converter and implement using suitable PLA	15	BTL4	Analyzing
4	Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions. $F_1(A,B,C) = \sum (0, 1, 2, 4)$	15	BTL6	Creating

	$F_2(A,B,C)=\sum (0, 5, 6, 7)$			
5	Explain about error detection and correction using Hamming codes.	15	BTL5	Evaluating
6	The following message have been coded in the even parity hamming code and transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each codeword. i) 1001001 **(04)** ii) 0111001 **(04)** iii) 1110110 **(04)** iv) 0011011 **(03)**	15	BTL5	Evaluating