SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF

ELECTRICAL AND ELECTRONICS ENGINEERING

QUESTION BANK

III SEMESTER

1905302 DIGITAL ELECTRONICS

Regulation – 2019

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Prepared by

Ms. Bency. P, Assistant Professor (O. G)

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SUBJECT & SUBJECT CODE: 1905302- Digital Electronics SEM / YEAR: II / III

UNIT-I NUMBER SYSTEMS, BOOLEAN ALGEBRA AND COMBINATIONAL CIRCUITS

Number system, error detection, corrections & codes conversions, Boolean algebra: De-Morgan's theorem, switching functions and minimisation using K-maps & Quine McCluskey method

PART-A

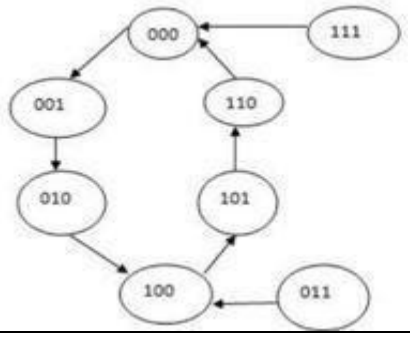
Q. No	Questions	BT Level	Competence	CO
1.	Label the different types of number system.	BTL1	Remembering	CO1
2.	Convert decimal to binary. i. 35 ii. 25	BTL2	Understanding	CO1
3.	Renovate decimal to octal. i. 45 ii. 65	BTL1	Remembering	CO1
4.	Infer the rules of successive multiplication method.	BTL2	Understanding	CO1
5.	Determine the following i. $(110011)_2 = (\_\_\_\_\_)_{10}$ ii. $(43)_8 = (\_\_\_\_\_)_{10}$	BTL3	Applying	CO1
6.	Build the rules for binary to octal conversion with an example.	BTL3	Applying	CO1
7.	Bring out the rules for binary to hexadecimal conversion with an example.	BTL1	Remembering	CO1
8.	Deduct the rules for octal to hexadecimal conversion with an example.	BTL5	Evaluating	CO1
9.	Illustrate binary codes.	BTL2	Understanding	CO1
10.	Explore the different types of binary codes.	BTL4	Analyzing	CO1
11.	Define gray code.	BTL1	Remembering	CO1
12.	Convert binary to gray code 1001.	BTL4	Analyzing	CO1
13.	Outline Excess-3 code.	BTL2	Understanding	CO1
14.	Switch the gray code 1101 to binary code.	BTL4	Analyzing	CO1
15.	Identify error detection and correction code.	BTL3	Applying	CO1
16.	Recall about Boolean algebra.	BTL1	Remembering	CO1
17.	What do you meant by postulates?	BTL1	Remembering	CO1
18.	Compose the meaning of literals.	BTL6	Creating	CO1
19.	Compile about product term and sum term.	BTL6	Creating	CO1
20.	Criticize SOP form & POS form.	BTL5	Evaluating	CO1
21.	Recollect canonical form.	BTL1	Remembering	CO1

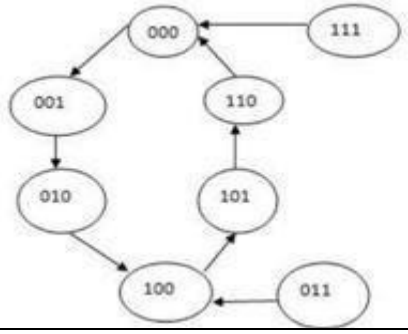
22.	Infer about octet, quad, pair and isolated ones.		BTL2	Understanding	CO1
23.	f(A,B,C)=ABC+AB'C+ABC'+A'BC express in M-notation.		BTL3	Applying	CO1
24.	Analyze the limitations while using Boolean postulates and theorems for simplifying Boolean function.		BTL4	Analyzing	CO1
	PART-B				
1.	What are the different types of number system and give short note on conversion between number systems. i. Integer part ii. Fraction part	(3) (5) (5)	BTL1	Remembering	CO1
2.	Convert the following. i. $(1100)_2 = (\_\_\_\_\_)_{10}$ ii. $(137)_{10} = (\_\_\_\_\_)_8$ iii. $(56)_{10} = (\_\_\_\_\_)_8$ iv. $(223)_{10} = (\_\_\_\_\_)_{16}$ v. $(DF)_{16} = (\_\_\_\_\_)_{10}$ vi. $(62.625)_{10} = (\_\_\_\_\_)_2$	 (2) (2) (2) (2) (2) (3)	BTL2	Understanding	CO1
3.	Explain the procedure to form hamming code and how to detect error and correct the message as well as determine hamming code for the binary word 1001 for odd parity.	(13)	BTL3	Applying	CO1
4.	Summarize the postulates of Boolean algebra and prove idempotency theorem and associative law.	(13)	BTL2	Understanding	CO1
5.	Write involution theorem and prove the following i. A+A'B=A+B ii. AB+BC+B'C=AB+C	(3) (5) (5)	BTL1	Remembering	CO1
6.	Apply the rules and convert the following SOP to standard SOP. i. F(A,B,C)=AC+AB+BC ii. F(A,B,C)=A+ABC	 (7) (6)	BTL3	Applying	CO1
7.	Analyze the rules for converting POS to standard POS. i. F(A,B,C)=(A+B).(B+C).(A+C) ii. F(A,B,C)=(A+B+C).A	 (7) (6)	BTL4	Analyzing	CO1
8.	State the rules for converting SOP &POS in its canonical form with examples.	(13)	BTL1	Remembering	CO1
9.	Indulge the min terms and max terms and express the following in M-notation i. F(A,B,C)=ABC+AB'C+ABC'+A'BC ii. F(A,B,C)=(A+B+C).(A+B+C').(A'+B+C).(A+B'+C)	(3) (5) (5)	BTL2	Understanding	CO1
10.	Obtain the truth table for the following function f(x,y,z)=xy+x'z and write it in M-notation and	(13)	BTL1	Remembering	CO1

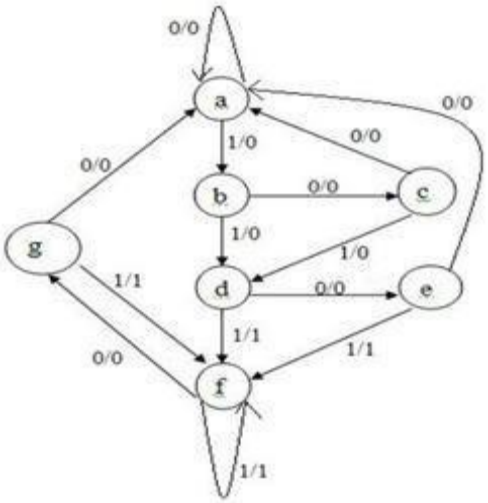
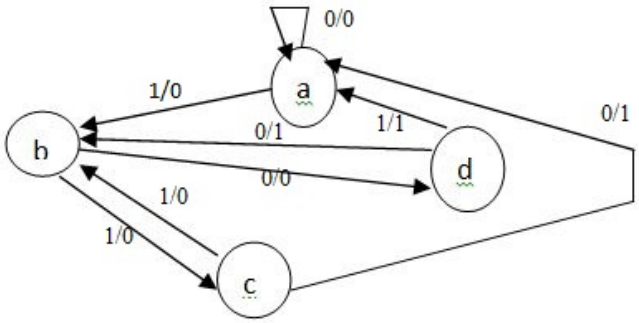
	canonical form.				
11.	Minimize the following function $F(a,b,c,d)=\pi M(0,3,4,7,8,10,12,14)+d(2,6)$ $F(a,b,c,d)=\sum m(0,4,6,8,9,10,12)$ with d(2,13).	(13)	BTL4	Analyzing	CO1
12.	Make clear about the procedure to form hamming code and how to detect error and correct the message as well as determine hamming code for the binary word 1001 for even parity.	(13)	BTL3	Applying	CO1
13.	Prove that F=A'B+AB' is exclusive OR operation and it equals (((AB)'.A)'.((AB)'.B)')'	(13)	BTL5	Evaluating	CO1
14.	Reduce the following using K map $f(A,B,C,D)=\sum M(4,5,6,7,8,10,11,14)$ F(x,y,z)=xy'z'+xyz+xyz'+xy'z+xy'z'	(13)	BTL6	Creating	CO1
15.	Recall the postulates of Boolean algebra and prove any two theorems.	(13)	BTL1	Remembering	CO1
16.	Reduce using K-map $f(a,b,c,d)=\sum m(7,8,9)+d(2,3,10,11,12,13,14,15)$	(13)	BTL2	Understanding	CO1
17.	Obtain the truth table for the following function f(a,b,c)=ab+a'c and write it in M-notation and canonical form.	(13)	BTL3	Applying	CO1
	PART-C				
1.	Interpret the general idea of number system with suitable examples.	(15)	BTL5	Evaluating	CO1
2.	Evaluate error detection and correction code with examples.	(15)	BTL5	Evaluating	CO1
3.	Compose the details of Boolean algebra with postulates and prove i. Absorption theorem ii. Associative law iii. Demorgan's theorem	 (5) (5) (5)	BTL6	Creating	CO1
4.	With use of K-map find the simplest form of SOP F=f.g where f=xy+z; g=yz+zx	(15)	BTL6	Creating	CO1
5.	Simplify the Boolean function using Quine McCluskey's tabulation method:F(A,B,C,D)= $\sum m(0,5,7,8,9,10,11,14,15)$	(15)	BTL4	Analyzing	CO1
	UNIT-II DESIGN OF COMBINATIONAL LOGIC CIRCUITS USING GATES AND MSI DEVICES				
Design of adder, subtractor, comparators, code converters, encoders, decoders, multiplexers and demultiplexers, Realisation of Boolean Functions using MSI devices, memories and PLA.					
	PART-A				
Q. No	**Questions**		**BT Level**	**Competence**	**CO**
1.	Give the Gray code for the binary number $(1011)_2$.		BTL1	Remembering	CO2
2.	Infer the basic logic gates.		BTL2	Understanding	CO2
3.	What is gray code and mention its advantages.		BTL1	Remembering	CO2

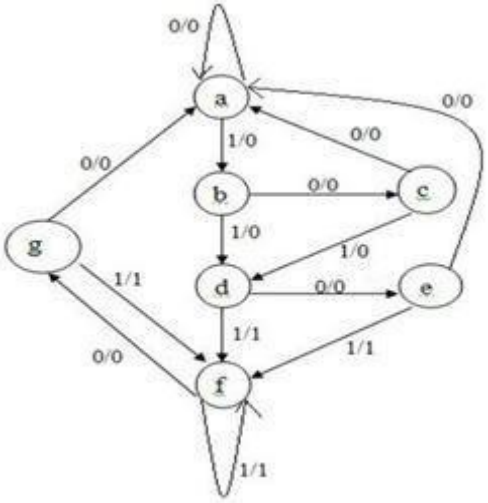
4.	Annotate the block diagram of encoder.		BTL2	Understanding	CO2
5.	Articulate the merits of code converters?		BTL3	Applying	CO2
6.	Interpret about magnitude comparator.		BTL3	Applying	CO2
7.	Bring out the applications of multiplexer.		BTL1	Remembering	CO2
8.	Draw the logic diagram of a half adder.		BTL5	Evaluating	CO2
9.	Sketch the block diagram of decoder.		BTL2	Understanding	CO2
10.	Analyze half subtractor with logic diagram.		BTL4	Analyzing	CO2
11.	Recall the working of demultiplexer.		BTL1	Remembering	CO2
12.	Investigate the reason why multiplexer is called data selector.		BTL4	Analyzing	CO2
13.	Describe combinational logic circuit.		BTL2	Understanding	CO2
14.	Erect OR gate using only NAND gates.		BTL4	Analyzing	CO2
15.	Apply the function F=∑(0,2,3,7) to form a logic diagram.		BTL3	Applying	CO2
16.	Mention the dependency of the output in combinational circuits.		BTL1	Remembering	CO2
17.	Interpret the block diagram of encoder.		BTL1	Remembering	CO2
18.	Compare and compile the difference between decoder and demultiplexer.		BTL6	Creating	CO2
19.	Draw the NAND gate circuit using NOT, AND & OR gates.		BTL6	Creating	CO2
20.	Draw the truth table of 2:1 MUX		BTL5	Evaluating	CO2
21.	Define multiplexer.		BTL1	Remembering	CO2
22.	What is a PLA?		BTL2	Understanding	CO2
23.	Outline about PLA.		BTL3	Applying	CO2
24.	Draft the block diagram of decoder.		BTL4	Analyzing	CO2
PART-B					
1.	Design a half adder and half subtractor.	(13)	BTL1	Remembering	CO2
2.	Interpret full adder and full subtractor.	(13)	BTL2	Understanding	CO2
3.	Use two half adder to form a full adder.	(13)	BTL3	Applying	CO2
4.	Design a 4-bit gray to binary code converter and implement it using logic gates.	(13)	BTL2	Understanding	CO2
5.	Recall the implementation procedure using multiplexer and also implement the switching function using 8:1 multiplexer f(A,B,C,D)=∑m(0,1,3,4,8,9,15)	(13)	BTL1	Remembering	CO2
6.	Design a BCD to Excess 3 code converter and implement it using logic gates.	(13)	BTL3	Applying	CO2
7.	Analyze and implement the switching function f(a,b,c)= ∑m(3,4,5,7) using suitable multiplexer.	(13)	BTL4	Analyzing	CO2
8.	Outline short notes on i. Demultiplxer ii. Encoder iii. Decoder iv. Magnitude comparator	 (3) (4) (3) (3)	BTL1	Remembering	CO2

9.	Propose the combinational circuit for a half adder and half subtractor.	(13)	BTL2	Understanding	CO2
10.	Form full subtractor employing half subtractor.	(13)	BTL1	Remembering	CO2
11.	Articulate the realization procedure using multiplexer and also implement the switching function using 8*1 multiplexer $f(A,B,C,D)=\sum m(0,2,3,4,8,9,14,15)$	(13)	BTL4	Analyzing	CO2
12.	Describe magnitude comparator and explain two bit magnitude comparator.	(13)	BTL3	Applying	CO2
13.	Evaluate a BCD to Excess 3 code converter and execute it using logic gates.	(13)	BTL5	Evaluating	CO2
14.	Create a combinational circuit for full adder and full subtractor.	(13)	BTL6	Creating	CO2
15.	Design a full adder and half adder using 4*1 multiplexer.	(13)	BTL1	Remembering	CO2
16.	Summarize the following v. Demultiplxer vi. Encoder vii. Decoder viii. Magnitude comparator	(13)	BTL2	Understanding	CO2
17.	Propose a 4-bit gray to binary code converter and realize it using logic gates.	(13)	BTL3	Applying	CO2
	PART-C				
1.	Implement $f(a,b,c,d)=\sum m(1,4,5,7,9,12,13)$ using three 2:1 multiplexer.	(15)	BTL5	Evaluating	CO2
2.	Design a combinational circuits with three inputs x, y and z, and the three outputs A, B, C. when the binary input is 0,1,2 or 3, the binary output is one greater than the input. When the binary input is 4,5,6,7 the binary output is one less than the input.	(15)	BTL5	Evaluating	CO2
3.	Assume a 3 input AND gate with output F and one 3 input OR gate with G output. Show the signals of the outputs F and G as functions of the three inputs ABC. Use all 8 possible combinations of inputs ABC.	(15)	BTL6	Creating	CO2
4.	Design a PLA structure using AND & OR logic for the following function. $F1=\sum m(0,1,2,3,4,7,8,11,12,15)$ $F2=\sum m(2,3,6,7,8,9,12,13)$ $F3=\sum(1,3,7,8,11,12,15)$ $F4=\sum(0,1,4,8,11,12,15)$	 (4) (4) (4) (3)	BTL6	Creating	CO2
5.	Design a Binary to Excess-3 code converter and implement it using logic gates.	(15)	BTL4	Analyzing	CO2
	UNIT-III ANALYSIS AND DESIGN OF SYNCHRONOUS SEQUENTIAL				

CIRCUITS					
Flip flops - SR, D, JK and T, shift registers, counters, state assignments analysis and design of synchronous sequential circuits, state diagram; state reduction.					
PART-A					
Q. No	**Questions**		**BT Level**	**Competence**	**CO**
1.	Convert T Flip Flop to D Flip Flop.		BTL1	Remembering	CO3
2.	Infer the rules for state assignment.		BTL2	Understanding	CO3
3.	State truth table for SR flip flop.		BTL1	Remembering	CO3
4.	Interpret the benefits of state reduction.		BTL2	Understanding	CO3
5.	Show how the JK flip-flop can be modified into a D flip-flop or a T flip-flop.		BTL3	Applying	CO3
6.	Give the characteristic equation and state diagram of JK flip-flop.		BTL3	Applying	CO3
7.	What is a self-starting counter?		BTL1	Remembering	CO3
8.	Compare combinational and sequential circuits.		BTL5	Evaluating	CO3
9.	Inspect the drawback of RS flip-flop.		BTL2	Understanding	CO3
10.	Implement T flip-flop using JK flip-flop.		BTL4	Analyzing	CO3
11.	What is a preset table counter and ripple counter?		BTL1	Remembering	CO3
12.	Deduce the drawback of SR flip-flop.		BTL4	Analyzing	CO3
13.	Describe synchronous sequential circuit.		BTL2	Understanding	CO3
14.	Analyze state assignment.		BTL4	Analyzing	CO3
15.	Identify the truth table for T flip-flop.		BTL3	Applying	CO3
16.	Give the characteristic equation and characteristic table of T flip flop.		BTL1	Remembering	CO3
17.	Design the excitation table for JK flip-flop.		BTL1	Remembering	CO3
18.	Give the characteristic equation and state diagram of T flip-flop		BTL6	Creating	CO3
19.	Design the excitation table for T flip-flop.		BTL6	Creating	CO3
20.	Design the excitation table for D flip-flop.		BTL5	Evaluating	CO3
21.	Bring out truth table for SR flip flop.		BTL1	Remembering	CO3
22.	Recognize the truth table for T flip-flop.		BTL2	Understanding	CO3
23.	Realize T flip-flop using JK flip-flop.		BTL3	Applying	CO3
24.	Contrast sequential and combinational circuits.		BTL4	Analyzing	CO3
PART-B					
1.	Propose a counter for the following state diagram 	(13)	BTL1	Remembering	CO3
2.	Explain the operation, state diagram and	(13)	BTL2	Understanding	CO3

	characteristics of T flip flop and master slave JK flip flop.				
3.	Draw the logic diagram of 4-bit synchronous counter. Explain the operation of the counter using the timing diagram	(13)	BTL3	Applying	CO3
4.	Explain the types of shift register in detail.	(13)	BTL2	Understanding	CO3
5.	A sequential circuit has two JK flip-flop A and B, two inputs x and y, and one output z. the equations are JA=Bx+B'y'; KA= B'xy' JB= A'x; KB=A+xy' Z=Ax'y'+Bx'y. Draw the logic diagram and state table.	(13)	BTL1	Remembering	CO3
6.	i. Estimate a sequential circuit with two D-flip-flops A and B and one output x. When x=0, the state of the circuit goes through the state transitions from 00 01 11 10 00 and repeats. ii. Estimate mod 7 counter using D flip-flops.	(7) (6)	BTL3	Applying	CO3
7.	A sequential circuit has two JK flip-flops A and B. The flipflop input functions are: JA=B; JB=x KA= B x ; KB=A⊕x i. Draw the logic diagram of the circuit ii. Tabulate the state table iii. Draw the state diagram	 (5) (4) (4)	BTL4	Analyzing	CO3
8.	Design a counter for the following state diagram 	(13)	BTL1	Remembering	CO3
9.	Estimate a sequential circuit for the following state equations A(t+1)= C⊕D; B(t+1) = A; C(t+1) = B; D(t+1)=C.	(13)	BTL2	Understanding	CO3
10.	Using JK flip-flops, design a synchronous counter which counts in the sequence, 000,001,010,011,100,101,110,111,000.	(13)	BTL1	Remembering	CO3
11.	Design a 4-bit BCD ripple counters.	(13)	BTL4	Analyzing	CO3
12.	Design a 3 bit binary counter using T flip-flop.	(13)	BTL3	Applying	CO3
13.	Implement JK FF using SR FF.	(13)	BTL5	Evaluating	CO3
14.	Compile the logic diagram and state table for a sequential circuit has two JK flip-flop A and B,	(13)	BTL6	Creating	CO3

	two inputs x and y, and one output z. the equations are JA=Bx+B'y'; KA= B'xy' JB= A'x; KB=A+xy' Z=Ax'y'+Bx'y.				
15.	Differentiate asynchronous and synchronous type counters.	(13)	BTL1	Remembering	CO3
16.	Design a 5-bit ring counter and mention its applications.	(13)	BTL2	Understanding	CO3
17.	Construct reduced state diagram for the following state diagram.  	(13)	BTL3	Applying	CO3
	PART-C				
1.	Design a clocked sequential circuit using T-FF for the following state diagram. Use state reduction if possible. Also use straight binary assignment.  	(15)	BTL5	Evaluating	CO3
2.	Design a sequential circuits with two D flip flops A and B and one input x. When x=0,the state of the circuit remains the same. When x=1, the circuits goes through the state transition from 00 to 01 to 11 to 10 back to 00,and repeats.	(15)	BTL5	Evaluating	CO3
3.	Explain the realization of JK flipflop from T flipflop	(15)	BTL6	Creating	CO3
4.	Create reduced state diagram for the following state diagram.	(15)	BTL6	Creating	CO3



5.	Design a sequential circuit using T-flip-flop. The state table of the circuit is as given below.				(15)	BTL4	Analyzing	CO3

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

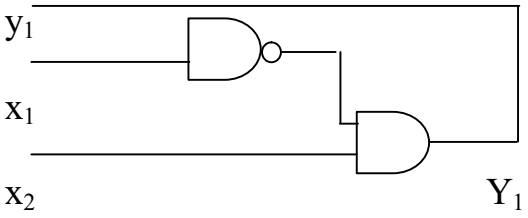
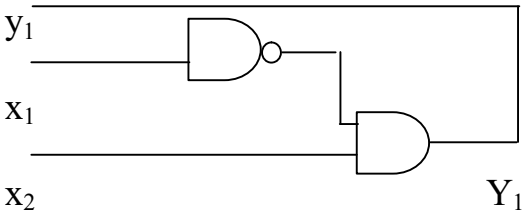
UNIT-IV ANALYSIS AND DESIGN OF ASYNCHRONOUS SEQUENCTIAL CIRCUITS

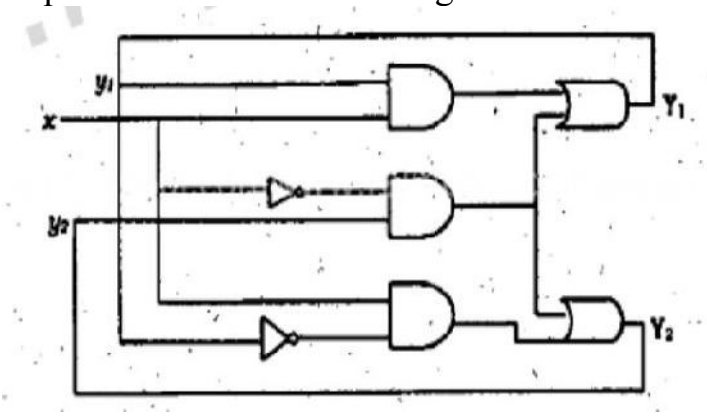
Latches - SR - D ,Asynchronous sequential logic circuits-Transition table, flow table – race conditions – circuits with latches, analysis of asynchronous sequential logic circuits – introduction to design – implication table.

PART-A

Q. No	Questions	BT Level	Competence	CO
1.	List the disadvantages of asynchronous sequential circuit?	BTL1	Remembering	CO4
2.	Infer race around condition in flip-flops.	BTL2	Understanding	CO4
3.	Draw the block diagram of asynchronous sequential circuits.	BTL1	Remembering	CO4
4.	Illustrate transition table?	BTL2	Understanding	CO4
5.	Compare and compile the difference between flow table and transition table.	BTL3	Applying	CO4
6.	Identify races in Asynchronous sequential circuit.	BTL3	Applying	CO4
7.	Show fundamental mode of operation in asynchronous sequential circuits.	BTL1	Remembering	CO4
8.	Describe asynchronous sequential machine.	BTL5	Evaluating	CO4
9.	Compare critical race and non critical race.	BTL2	Understanding	CO4

10.	Analyze flow table with example.		BTL4	Analyzing	CO4
11.	Outline deadlock condition?		BTL1	Remembering	CO4
12.	Deduce the demerits in designing asynchronous sequential machines		BTL4	Analyzing	CO4
13.	Point out the definition for flow table in asynchronous sequential circuit.		BTL2	Understanding	CO4
14.	Analyze about basic storage element.		BTL4	Analyzing	CO4
15.	Point out the characteristic table of SR latch.		BTL3	Applying	CO4
16.	Identify the meaning of latch.		BTL1	Remembering	CO4
17.	How many types of latches are?		BTL1	Remembering	CO4
18.	Compile the application of latches.		BTL6	Creating	CO4
19.	Compose the types of sequential circuits.		BTL6	Creating	CO4
20.	Evaluate the fastest circuit synchronous or asynchronous circuits.		BTL5	Evaluating	CO4
21.	Highlight the characteristic table of SR latch.		BTL1	Remembering	CO4
22.	Interpret he meaning of latch?		BTL2	Understanding	CO4
23.	Categorize types of latches are?		BTL3	Applying	CO4
24.	Investigate about basic storage element.		BTL4	Analyzing	CO4
	PART-B				
1.	Design an asynchronous sequential circuit has two inputs X_2 and X_1 and one output Z. When X_1=0, the output Z is to remain as 0 as long as X_1 is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.	(13)	BTL1	Remembering	CO4
2.	An asynchronous sequential circuit is described by Y=x1x'2+(x1 + x'2) y; z=y. Draw the logic diagram, transition table and output map.	(13)	BTL2	Understanding	CO4
3.	Explain the operation of SR FF,JK FF, D FF and T FF.	(13)	BTL3	Applying	CO4
4.	Discover an asynchronous sequential circuit with two inputs T and C. The output attains a value of 1 when T=1 & C moves from 1 to 0. Otherwise the output is 0.	(13)	BTL2	Understanding	CO4
5.	Describe the steps involved in design of asynchronous sequential circuit in detail with an example.	(13)	BTL1	Remembering	CO4
6.	i. How do you get output specifications from a flow table in asynchronous sequential circuit operating in fundamental mode? ii. When do you get the critical and non- critical races? How will you obtain race free conditions?	(13)	BTL3	Applying	CO4
7.	An asynchronous sequential circuit is described		BTL4	Analyzing	CO4

	by the following excitation and the output function Y=x1x2+(x1+x2)y. i. Draw the logic diagram of the circuit. ii. Derive the transition table and output map. iii. (iii) Describe the behaviour of the circuit.	 (3) (3) (7)			
8.	Check whether the given asynchronous sequential circuit is stable or unstable  	(13)	BTL1	Remembering	CO4
9.	Design a asynchronous sequential circuit with two input D and G and with one output Z. whenever G is 1 input D is transferred to Z. When G is 0 the output does not change for any charge in D. Use SR FF for implementation of the circuit.	(13)	BTL2	Understanding	CO4
10.	Propose an asynchronous sequential circuit has two inputs X_2 and X_1 and one output Z. When X_1=0, the output Z is to remain as 0 as long as X_1 is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.	(13)	BTL1	Remembering	CO4
11.	Analyze whether the given asynchronous sequential circuit is stable or unstable  	(13)	BTL4	Analyzing	CO4
12.	Derive the asynchronous sequential circuit specified by the flow table y \ x_1 x_2 a: a,0 | a,0 | a,0 | b,0 b: a,0 | a,0 | b,1 | b,0	(13)	BTL3	Applying	CO4
13.	Evaluate and sketch the logic diagram, transition table and output mapfor an asynchronous sequential circuit described by $Y=x_1x'_2+(x_1 + x'_2)$ y; z=y.	(13)	BTL5	Evaluating	CO4
14.	Compile an asynchronous sequential circuit with	(13)	BTL6	Creating	CO4

	2 inputs T and C. The output attains a value of 1 when T=1 & C moves from 1 to 0. Otherwise the output is 0.				
15.	Elucidate the operation of SR latch using NAND gate.	(13)	BTL1	Remembering	CO4
16.	Implement D flipflop using JK FF	(13)	BTL2	Understanding	CO4
17.	Elaborate different Types of FF.	(13)	BTL3	Applying	CO4
	PART-C				
1.	Explain the operation of SR latch using NOR gate and discuss its operation with clocked SR latch.	(15)	BTL5	Evaluating	CO4
2.	Design a asynchronous sequential circuit with two input A and B and with one output Z. whenever B is 1 input A is transferred to Z. When B is 0 the output does not change for any charge in A.	(15)	BTL5	Evaluating	CO4
3.	Describe the procedure to design of asynchronous sequential circuit in detail with an example.	(15)	BTL6	Creating	CO4
4.	Derive the asynchronous sequential circuit specified by the flow table y \ x_1 x_2 a: a,0 | a,0 | a,0 | b,0 b: a,0 | a,0 | b,1 | b,0	(15)	BTL6	Creating	CO4
5.	Derive the transition table and primitive flow table for the functional mode asynchronous sequential circuit shown in fig 	(15)	BTL4	Analyzing	CO4
	UNIT-V LOGIC FAMILIES AND VHDL				
Logic families: RTL and DTL Circuits, TTL ECL NMOS and CMOS: Introduction to VHDL: Design – combinational logic – Types – Operators – Packages – Sequential circuit – Sub programs – Test benches. (Examples: adders, counters, flipflops, FSM, Multiplexers / Multiplexers).					
	PART-A				
Q. No	**Questions**		**BT Level**	**Competence**	**CO**
1.	Compare the totem-pole output with open-collector		BTL1	Remembering	CO5

	output?				
2.	List the factors used for measuring the performance of digital logic families.		BTL2	Understanding	CO5
3.	When can RTL be used to represent digital systems?		BTL1	Remembering	CO5
4.	State the important characteristics of TTL family		BTL2	Understanding	CO5
5.	Summarize the advantages of ECL as compared to TTL logic family.		BTL3	Applying	CO5
6.	Which is faster TTL or ECL?		BTL3	Applying	CO5
7.	Sketch the DTL based NAND gate.		BTL1	Remembering	CO5
8.	Evaluate package in VHDL.		BTL5	Evaluating	CO5
9.	Inscribe the VHDL behavioral model for D-flip-flop.		BTL2	Understanding	CO5
10.	Write the VHDL code for a logical gate which gives high output only when both the inputs are high.		BTL4	Analyzing	CO5
11.	Name any four hardware description language test benches.		BTL1	Remembering	CO5
12.	Analyze the syntax for package declaration and package body in VHDL		BTL4	Analyzing	CO5
13.	Write VHDL code for 2*1 MUX using behavioral modeling		BTL2	Understanding	CO5
14.	Illustrate the basic structure of MOS transistor.		BTL4	Analyzing	CO5
15.	Display the function of wait statement in VHDL package?		BTL3	Applying	CO5
16.	Compile VHDL code for half adder in data flow model.		BTL1	Remembering	CO5
17.	Analyze the merits of hardware languages.		BTL1	Remembering	CO5
18.	What is the function of wait statement in VHDL package? Compose the operators used in VHDL.		BTL6	Creating	CO5
19.	Predict the need for VHDL.		BTL6	Creating	CO5
20.	Categorize different test bench.		BTL5	Evaluating	CO5
21.	Which requires more power to operate TTL or ECL?		BTL1	Remembering	CO5
22.	Estimate any hardware description language test benches.		BTL2	Understanding	CO5
23.	Articulate DTL based NAND gate.		BTL3	Applying	CO5
24.	Deduce package in VHDL.		BTL4	Analyzing	CO5
	PART-B				
1.	Discuss about TTL parameters.	(13)	BTL1	Remembering	CO5
2.	i. With circuit schematic, explain the operation of a two port TTL NAND gate with totem-pole output. ii. Compare totem pole and open collector outputs.	(7) (6)	BTL2	Understanding	CO5
3.	With neat sketch explain the circuit diagram of CMOS NOR gate.	(13)	BTL3	Applying	CO5
4.	Explain the characteristics and implementation of the following digital logic families. i. CMOS	(5)	BTL2	Understanding	CO5

	ii. ECL iii. TTL	(5) (3)			
5.	Draw the MOS logic circuit for NOT gate and explain its operation.	(13)	BTL1	Remembering	CO5
6.	Write short notes on following: i. RTL ii. DTL iii. ECL	 (5) (5) (3)	BTL3	Applying	CO5
7.	With neat sketch explain the operation of MOS family.	(13)	BTL4	Analyzing	CO5
8.	Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out power dissipation, propagation delay and noise margin. Compare its advantages over other logic families.	(13)	BTL1	Remembering	CO5
9.	Write the VHDL code to realize a full adder using behavioral modeling and structural modeling.	(13)	BTL2	Understanding	CO5
10.	Write the VHDL code to realize a 3-bit gray code counter using case statement.	(13)	BTL1	Remembering	CO5
11.	Write VHDL code for Binary UP/ DOWN counter using JK flip- flops.	(13)	BTL4	Analyzing	CO5
12.	Design a 3 bit magnitude comparator and write the VHDL coding to realize it using structural modeling.	(13)	BTL3	Applying	CO5
13.	Explain in detail the concept of Structural modeling in VHDL with an example of full adder.	(13)	BTL5	Evaluating	CO5
14.	Design a VHDL code for full adder and 8*1 MUX	(13)	BTL6	Creating	CO5
15.	Write the VHDL code to realize a half adder using behavioral modeling and structural modeling.	(13)	BTL1	Remembering	CO5
16.	Represent with neat diagram about the MOS logic circuit for NOT gate and explicate its operation.	(13)	BTL2	Understanding	CO5
17.	Establish the circuit diagram of CMOS NOR gate.	(13)	BTL3	Applying	CO5
PART-C					
1.	Engrave the VHDL code to realize a full adder using behavioral modeling and structural modeling.	(15)	BTL5	Evaluating	CO5
2.	Explain with an aid of circuit diagram the operation of2 input CMOS NAND gate and list out its advantages over other logic families.	(15)	BTL5	Evaluating	CO5

3.	Compile a 4 X 4 array multiplier and write the VHDL coding to realize it using structural modeling.	(15)	BTL6	Creating	CO5
4.	i. Compose short notes on built-in operators used in VHDL programming. ii. Compose VHDL coding for 4 X 1 Multiplexer	(8) (7)	BTL6	Creating	CO5
5.	i. Discuss briefly the packages in VHDL. ii. Write an VHDL coding for realization of clocked S-R flipflop.	(8) (7)	BTL4	Analyzing	CO5

Course Outcome:

- To understand and examine the structure of various number systems and its application in digital design to solve real world problems.
- Analyze and design combinational logic circuits using gates and MSI devices.
- Analyze and Design synchronous sequential logic circuits using Flip flops and gates.
- Analyze and Design Asynchronous sequential logic circuits using Latches and gates.
- Selection of logic families and skill development for application specific digital circuit design using VHDL.