SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)
SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

III SEMESTER

1906302–ANALOG ELECTRONICS - I

Regulation – 2019

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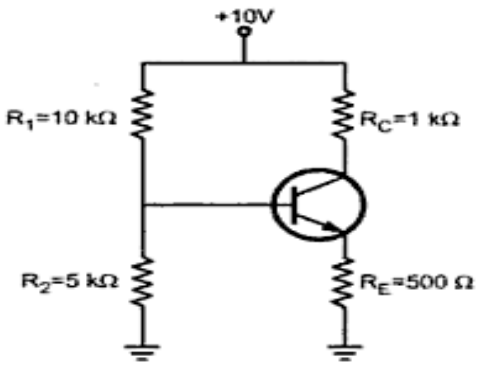
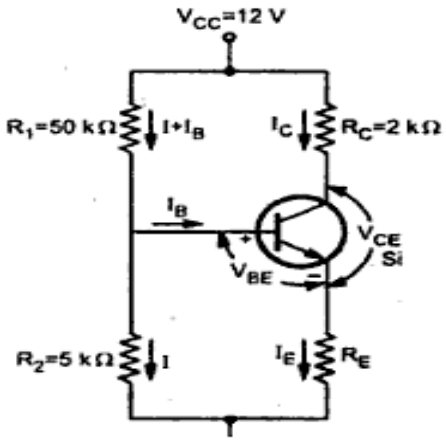
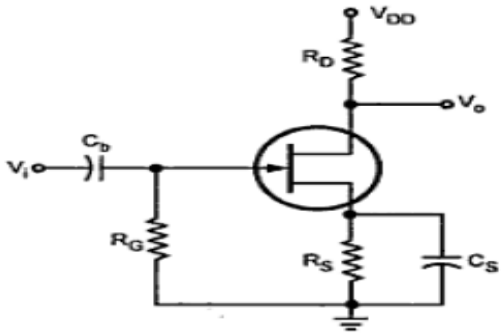
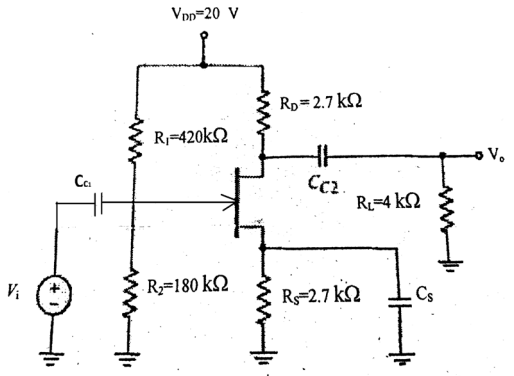
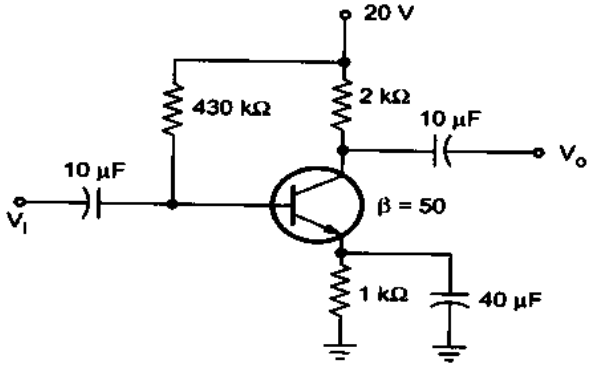
SUBJECT : 1906302–ANALOG ELECTRONICS - I

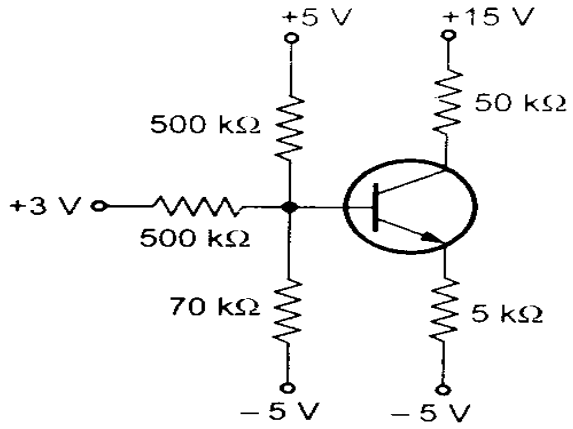
SEM / YEAR : III/ II Year ECE

UNIT I - BIASING OF DISCRETE BJT, JFET AND MOSFET			
BJT– Need for biasing - DC Load Line and Bias Point – DC analysis of Transistor circuits – Various biasing methods of BJT – Bias Circuit Design - Thermal stability - Stability factors - Bias compensation techniques using Diode, thermistor and sensistor – Biasing BJT Switching Circuits- JFET - DC Load Line and Bias Point - Various biasing methods of JFET - JFET Bias Circuit Design - MOSFET Biasing - Biasing FET Switching Circuits.			
PART - A			
Q.No	**Questions**	**BT Level**	**Competence**
1.	What do you mean by thermal runaway?	BTL 1	Remembering
2.	State the importance of selecting the proper operating point.	BTL 1	Remembering
3.	List out the various biasing methods.	BTL 1	Remembering
4.	Draw DC load line.	BTL 1	Remembering
5.	Define the impact of temperature on drain current of MOSFET?	BTL 1	Remembering
6.	How to find the expression for stability factor?	BTL 1	Remembering
7.	Predict the collector and base current for the given specifications h_{fe} =80,$V_{BE(ON)}$ = 0.7v, R_C=5K, R_B=10K, V_{CC}=5V.	BTL 2	Understanding
8.	Illustrate the main idea of compensation techniques.	BTL 2	Understanding
9.	Summarize the concept of operating point.	BTL 2	Understanding
10.	Give outline for compensation techniques.	BTL 2	Understanding
11.	Estimate the DC load line for fixed bias amplifier circuit.	BTL 2	Understanding
12.	State the relation between operating region and biasing of transistor junctions.	BTL 2	Understanding
13.	Identify the operating regions of N-channel MOSFET and how do you identify the operating region.	BTL 3	Applying
14.	Categorize the different methods of biasing a JFET.	BTL 3	Applying
15.	How would you apply various conditions for thermal stability and what are the conditions for thermal stability?	BTL 3	Applying
16.	Show the fixed bias single stage transistor circuit.	BTL 3	Applying
17.	Examine stability factors for BJT.	BTL 3	Applying
18.	Pointout the thermal runaway and condition for thermal stability.	BTL 3	Applying
19.	Analyze the function of Q-point. How it varies the output?	BTL 4	Analyzing
20.	Examine why the operating point selected at the center of the	BTL 4	Analyzing

	active region.			
21.	List out the advantages of using emitter resistance in the context of biasing.		BTL 4	Analyzing
22.	Inspect the importance of selecting the proper operating point.		BTL 4	Analyzing
23.	How would you explain FET is known as voltage variable resistor?		BTL 4	Analyzing
24.	Infer the reason for stabilizing the Q point of transistor.		BTL 4	Analyzing
	PART - B			
1.	Demonstrate the stability factor for voltage divider bias circuit and give reason why it is advantageous than fixed bias circuit.	(13)	BTL 1	Remembering
2.	What is DC load line? How will you select the operating point, explain it using common emitter amplifier characteristics as an example?	(13)	BTL 1	Remembering
3.	For a BJT with a voltage divider bias circuit, find the change in Q-point with the variation in β when the circuit contains an emitter resistor. Let the biasing resistors be R_{B1}=56kΩ, R_{B2}=12.2kΩ, R_C=2kΩ, R_E=0.4kΩ, V_{CC}=10V, $V_{BE(ON)}$=0.7V and β=100.	(13)	BTL 1	Remembering
4.	With neat diagrams, how would you show two bias compensation techniques and state its advantages and disadvantages.	(13)	BTL 1	Remembering
5.	(i) Design a fixed bias circuit to have operating point of (10V,3mA). The circuit is supplied with 20V and uses a silicon transistor of h_{fe} = 250.	(7)	BTL 1	Remembering
	(ii) Describe how DC load line is drawn.	(6)		
6.	Relate the various methods of biasing using BJT in terms of their stability factors.	(13)	BTL 2	Understanding
7.	(i) Illustrate stability and thermal stability.	(7)	BTL 2	Understanding
	(ii) Summarize the biasing FET switching circuits.	(6)		
8.	Interpret the circuit as shown in below. β =100 for this transistor. Calculate V_{CE} for a given circuit. 	(13)	BTL 2	Understanding

9.	(i) Interpret about the meaning of bias stability and what factors affect BJT biasing?	(7)	BTL 2	Understanding
	(ii) Estimate an expression for the stability factor for fixed bias method.	(6)		
10.	For the circuit shown in the figure, I_c=2mA, β =100, Calculate R_E,V_{EC} and stability factor. 	(13)	BTL 3	Applying
11.	The amplifier shown in Fig. an n-channel FET for which, I_D=0.8mA, V_P=-2V,V_{DD}=24V and I_{DSS}=1.6mA. Assume that r_d>Rd. Calculate the parameters V_{GS}, g_m, R_s. 	(13)	BTL 3	Applying
12.	Solve the bias resistor R_B for fixed bias and collector to base bias and compare the stability factor S for both of them. Given V_{CC} =12 V, R_L = 330 Ω, I_B = 0.3 mA, β = 100, V_{CEQ} = 6 V.		BTL 3	Applying
13.	Design the circuit shown below with transistor parameters I_{DSS}=12mA, V_p=-4V and λ=0.008V^{-1}. Determine the small signal voltage gain A_v=V_o/V_i.	(13)	BTL 3	Applying

				
14.	Analyze various techniques of stabilization of Q-point in a transistor	(13)	BTL 4	Analyzing
15.	Explain in detail about various methods of biasing MOSFET.	(13)	BTL 4	Analyzing
16.	(i) Examine the circuit which uses the diode to compensate for changes in I_{co}. Explain how stabilization is achieved in circuit.	(8)	BTL 4	Analyzing
	(ii) Briefly examine the reason for keeping the operating point of transistor as fixed.	(5)		
17.	(i) Inspect the importance of emitter stabilized biasing with necessary circuit diagram.	(5)	BTL 4	Analyzing
	(ii) Determine I_B, I_C, V_{CE}, V_C, V_B, V_E and V_{BC} For the emitter bias network shown below. 	(8)		
PART - C				
1.	With a neat diagram explain the source and drain resistance biasing of MOSFET.	(15)	BTL 1	Remembering
2.	Elaborate the various techniques that use temperature sensitive devices to maintain constant operating point and explain in detail.	(15)	BTL 2	Understanding

3.	The circuit shown in the figure, let h_{fe}= 100.  (i) Solve V_{th} and R_{th} for the base circuit. (ii) Measure I_{CQ} and V_{CEQ}. (iii) Draw the DC Load line.	(5) (5) (5)	BTL 3	Applying
4.	Examine the stability factors for any two biasing methods in detail.	(15)	BTL 4	Analyzing
5.	Analyze about the common source self bias and voltage divider bias for FET.	(15)	BTL 4	Analyzing

UNIT II - BJT AMPLIFIERS

Small Signal Hybrid π equivalent circuit of BJT – Early effect - Analysis of CE, CC and CB amplifiers using Hybrid π equivalent circuits - AC Load Line Analysis- Darlington Amplifier - Bootstrap technique - Cascade, Cascode configurations - Differential amplifier, Basic BJT differential pair – Small signal analysis and CMRR.

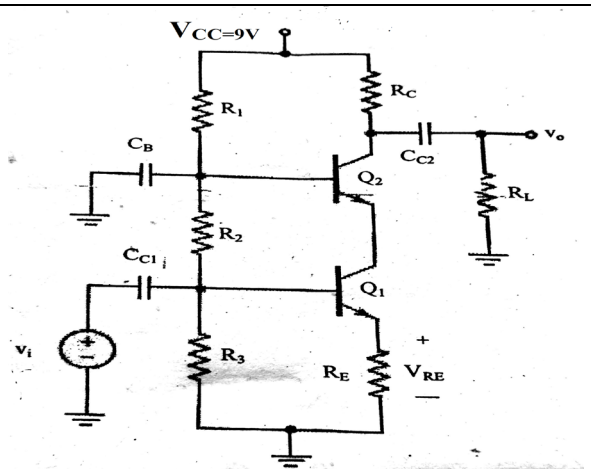
PART - A

Q.No	Questions	BT Level	Competence
1.	Define bypass and coupling Capacitor.	BTL 1	Remembering
2.	What is an amplifier and AC load line?	BTL 1	Remembering
3.	Can you recall transconductance?	BTL 1	Remembering
4.	How would you show Miller effect input capacitance?	BTL 1	Remembering
5.	Define CMRR of BJT differential amplifier.	BTL 1	Remembering
6.	State Miller's theorem.	BTL 1	Remembering
7.	Summarize the amplifiers classification according to the input.	BTL 2	Understanding
8.	Draw the small signal equivalent of CB configuration.	BTL 2	Understanding
9.	Compare cascade and cascode amplifier.	BTL 2	Understanding
10.	Find CMRR of differential amplifier with differential gain 300 and common mode gain of 0.2.	BTL 2	Understanding
11.	Discuss about power gain.	BTL 2	Understanding
12.	Draw the simplified hybrid π equivalent circuit for NPN transistor.	BTL 2	Understanding
13.	Construct the small signal AC equivalent circuit of the BJT.	BTL 3	Applying
14.	Why do you choose emitter bypass capacitor in CE amplifier circuit?	BTL 3	Applying

15.	Show the cascade amplifier and its ac equivalent circuit.	BTL 3	Applying
16.	State the advantages of un bypassed R_E in CE configuration.	BTL 3	Applying
17.	Compare AC and DC load lines.	BTL 3	Applying
18.	Illustrate about diffusion resistance.	BTL 3	Applying
19.	Categorize the different coupling schemes used in multistage amplifiers.	BTL 4	Analyzing
20.	Analyze the bootstrapping technique.	BTL 4	Analyzing
21.	Infer the need of differential amplifier.	BTL 4	Analyzing
22.	Inspect the importance of Darlington circuit.	BTL 4	Analyzing
23.	Assess why R_E is replaced by a constant current bias in a differential amplifier.	BTL 4	Analyzing
24.	Pointout the improvisation methods of CMRR in differential amplifier.	BTL 4	Analyzing

PART - B				
1.	Draw the circuit diagram of common emitter amplifier with voltage divider bias, coupling capacitor and bypass capacitor. With the help of small signal equivalent, obtain the expression for current gain, voltage gain, input and output impedance.	(13)	BTL 1	Remembering
2.	Find the gain, input and output resistance of common collector amplifier with a neat circuit diagram and equivalent circuit.	(13)	BTL 1	Remembering
3.	State and prove the Miller's theorem with example circuit.	(13)	BTL 1	Remembering
4.	What is CMRR? Derive CMRR of differential amplifier with its equivalent circuit.	(13)	BTL 1	Remembering
5.	Draw and explain the hybrid π equivalent circuit for NPN transistor.	(13)	BTL 1	Remembering
6.	Summarize the gain, input impedance and output impedance of single stage BJT amplifier using mid band analysis.	(13)	BTL 2	Understanding
7.	Explain the basic common base amplifier circuit and derive the expressions for its small signal voltage gain, current gain, input impedance and output impedance.	(13)	BTL 2	Understanding
8.	(i) Illustrate bootstrapped Darlington circuit with neat sketch.	(8)	BTL 2	Understanding
	(ii)Outline the transfer characteristics of differential amplifier.	(5)		
9.	Compare CB, CE and CC amplifiers and state their applications.	(13)	BTL 2	Understanding
10.	Construct the Darlington pair circuit with its operation and advantages and also explain its small signal voltage gain and input impedance.	(13)	BTL 3	Applying
11.	Derive the expression for R_i, A_v and R_o for CE amplifier with bypassed R_E.	(13)	BTL 3	Applying
12.	Illustrate the expressions for R_i, A_v and R_o for emitter follower amplifier.	(13)	BTL 3	Applying

13.	(i)Develop the circuit for the following transistor parameters, hfe=125,$V_a=\infty$,V_{CC}=18v,R_L=3KΩ,R_C=4kΩ.R_B=10.4kΩThe input signal is a current source. Identify its small signal voltage gain, current gain, maximum voltage gain and input impedance.	(8)	BTL 3	Applying
	(ii) Develop the circuit diagram of bootstrapped emitter follower with its equivalent circuit, derive for its input and output impedance.	(5)		
14.	Analyze the changes in the AC characteristics of a common emitter amplifier when an emitter resistor and an emitter bypass capacitor are incorporated in the design? Explain with necessary equations.	(13)	BTL 4	Analyzing
15.	Explain the operation of cascade amplifier and derive voltage gain, overall input resistance, overall current gain and output impedance.	(13)	BTL 4	Analyzing
16.	Examine the circuit diagram for a differential amplifier using BJT's and find CMRR through small signal analysis.	(13)	BTL 4	Analyzing
17.	Discuss about the cascode configurations of amplifiers using BJT and compare with cascade configurations.	(13)	BTL 4	Analyzing
	PART - C			
1.	Elaborate the small signal equivalent circuit and derive the transistor parameters of widely used amplifier whose current and voltage gain are greater than unity.	(15)	BTL 1	Remembering
2.	Derive the expression of common mode rejection ratio of dual input, balanced out emitter coupled differential amplifier.	(15)	BTL 2	Understanding
3.	Examine the bootstrapping technique of improving input resistance in common collector circuit.	(15)	BTL 3	Applying
4.	Estimate the input and output resistance of the emitter follower circuit for the given specifications. Assume R_S=0.5kΩ, $r_\pi = 3.28\,k\Omega$, β = 100, R_1 = R_2 = $50\,k\Omega$ and $r_o = 100\,k\Omega$, V_{CC}=5v, R_E= 2kΩ.	(15)	BTL 4	Analyzing
5.	Design the cascode circuit for the following specifications: $V_{CE1} = V_{CE2} = 2.5v$, $V_{BE} = 0.7v$, $I_{C1} = I_{c2} = 1mA$, and $I_{R1} = I_{R2} = I_{R3} = 0.10mA$.	(15)	BTL 4	Analyzing



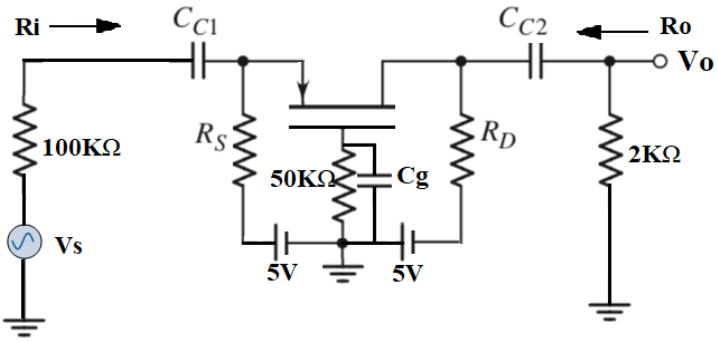
UNIT III – SINGLE STAGE FET, MOSFET AMPLIFIERS

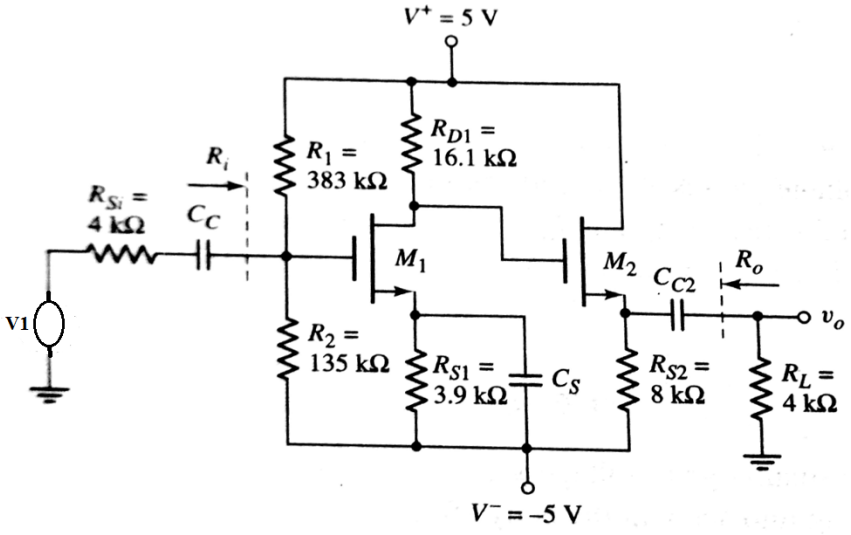
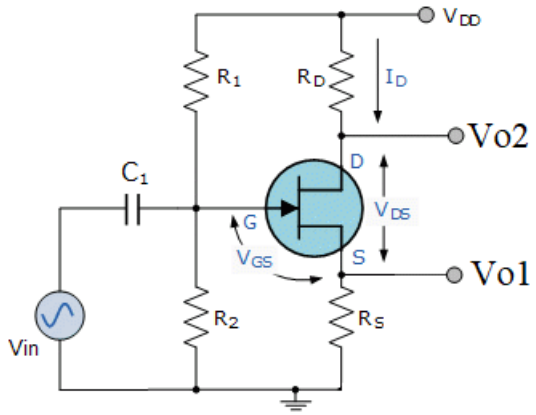
Small Signal Hybrid π equivalent circuit of FET and MOSFET - Analysis of CS, CD and CG amplifiers using Hybrid π equivalent circuits - Basic FET differential pair- BiCMOS circuits.

PART – A

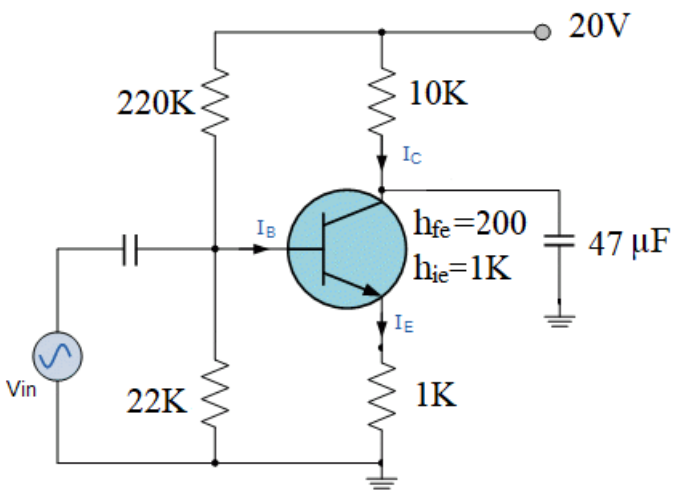
Q. No.	Question	BT Level	Competence
1.	List the advantages of common drain amplifier.	BTL1	Remembering
2.	What is BiCMOS?	BTL1	Remembering
3.	What is meant by voltage swing limitation in JFET?	BTL1	Remembering
4.	How a MOSFET can be used to amplify a time varying voltage?	BTL1	Remembering
5.	Identify the impact of including a source resistor in the FET	BTL1	Remembering
6.	What is the relationship between pinch off voltage and drain resistance?	BTL1	Remembering
7.	Write down the small signal parameters of JFET.	BTL2	Understanding
8.	Mention the effect of bypass capacitor on bandwidth of the amplifier.	BTL2	Understanding
9.	Draw a differential pair using FET.	BTL2	Understanding
10.	Discuss the use of MOSFET to amplify a time varying voltage.	BTL2	Understanding
11.	State the advantages of BiCMOS circuits.	BTL3	Applying
12.	Draw the circuit of JFET common source amplifier.	BTL3	Applying
13.	How will you construct low frequency equivalent circuit of FET?	BTL3	Applying
14.	The parameters for the transistor below are K_n = 0.5mA/V^2, V_{TN} = 1.2V, and λ = 0. Simplify V_{DS} and V_{GS} for I_Q=50 μA.	BTL4	Analyzing
15.	Analyze the transconductance with its expression.	BTL4	Analyzing
16.	Compare the three FET configurations (CS, CD and CG).	BTL4	Analyzing
17.	Explain the importance of multistage amplifiers.	BTL3	Applying
18.	N channel FET's are preferred over P channel FET's. Justify	BTL3	Applying

19.	Determine the output impedance of source follower circuit. Given that R_s=0.75KOhm, r_o = 12.5 KΩ and g_m= 11.3 mA/V.		BTL4	Analyzing
20.	Draw the small signal equivalent circuit for common source NMOS.		BTL4	Analyzing
21.	What are the features of BiCMOS cascode amplifier?		BTL1	Remembering
22.	Compare the features of three MOSFET amplifier configuration.		BTL4	Analyzing
23.	Draw the voltage current characteristics of JFET amplifier.		BTL4	Analyzing
24.	List the merits and demerits of BiCMOS differential amplifiers.		BTL2	Understanding
	PART-B			
1.	(i) How would you describe the expression for the voltage gain of JFET common source amplifier with bypassed R_S. (ii) Derive the expression for the voltage gain of JFET common source amplifier?	(7) (6)	BTL1	Remembering
2.	Explain the expression for common gate circuit of JFET.	(13)	BTL1	Remembering
3.	What is JFET amplifier? Derive gain, input and output impedance of common source JFET amplifier with neat circuit diagram and equivalent circuit.	(13)	BTL1	Remembering
4.	Define the circuit of a basic common source amplifier with voltage divider bias and derive the expressions for voltage gain, input impedance and output impedance using small signal model.	(13)	BTL1	Remembering
5.	(i) Explain the voltage gain of BiCMOS cascode amplifier. (ii) Draw a discrete common gate JFET amplifier and derive voltage gain A_v, input impedance R_{in}, and output impedance R_{out} with small signal equivalent circuit.	(8) (5)	BTL2	Understanding
6.	Derive the gain, input and output impedance of MOSFET source follower with neat circuit diagram and equivalent circuit.	(13)	BTL2	Understanding
7.	Calculate the voltage gain of the circuit, assuming the following parameters: V_{DD}=3.3V, R_D=10KΩ, R_{G1}=140KΩ, R_{G2}=60KΩ, R_{Si}=4KΩ. The transistors parameters are V_{tn} =0.4V, K_n=0.5mA/V^2 and λ=0.02V^{-1}	(13)	BTL2	Understanding
8.	(i) Explain how JFET can be used as an amplifier. (ii) Describe the small signal low frequency model of JFET.	(7) (6)	BTL3	Applying
9.	With the equivalent circuit of a common gate MOSFET amplifier, derive for A_v, A_i and R_i .	(13)	BTL3	Applying
10.	Analyze a simple JFET source-follower amplifier circuit and discuss the general AC circuit characteristics.	(13)	BTL4	Analyzing
11.	(i) Explain on voltage swing limitations, general conditions under which a source follower amplifier would be used. (ii) Describe the characteristics of BiCMOS circuits.	(10) (3)	BTL4	Analyzing
12.	(i) Mention the small signal parameters of MOSFET. (ii) Explain the configuration of a common-source amplifier with source resistor.	(7) (6)	BTL4	Analyzing

13.	(i) Consider the PMOS amplifier.The transistor parameters are V_{tp}=-1v,β_p=($\mu_p C_{ox}$(W/L)=1mA/v^2 and λ=0. (a) Determine R_D and R_S, such that I_{DQ} =0.75mA and V_{SDQ}=6V. (b) Determine input impedance R_i and output impedance R_o. (c) Voltage gain, Current gain and maximum Output voltage swing. (ii) Determine the current gain of JFET source follower amplifier. 	(4) (3) (4) (3)	BTL4	Analyzing
14.	Derive the expression for gain of NMOS source follower along with small signal equivalent circuit. Also explain cascade NMOS amplifier.	(13)	BTL4	Analyzing
15.	Compare the features and small signal equivalent circuits of three MOSFET amplifier configurations.	(13)	BTL4	Analyzing
16.	Enumerate in detail and derive the expression for voltage gain of CS and CD MOSFET amplifier.	(13)	BTL4	Analyzing
17.	Derive the expression for the following: (i) Voltage gain for common gate MOSFET amplifier, (ii) Current gain for common gate MOSFET amplifier.	(7) (6)	BTL4	Analyzing
	PART-C			
1.	What are the voltage swing limitations and general conditions under which a source amplifier would be used and explain common source amplifier with source resistor and source bypass capacitor?	(15)	BTL2	Understanding
2.	Design and analyze the characteristics of BiCMOS cascode amplifier, and explain graphically the amplification process in a simple MOSFET amplifier circuit.	(15)	BTL4	Analyzing
3.	Determine the small signal voltage gain of a multistage cascade circuit shown in the figure below. The transistor parameters are K_{n1}=0.5mA/V^2, K_{n2}=0.2mA/V^2, V_{TN1}=V_{TN2}=1.2V and λ_1=λ_2=0. The Quiescent drain currents are I_{D1}=0.2mA and I_{D2}=0.5mA.	(15)	BTL4	Analyzing

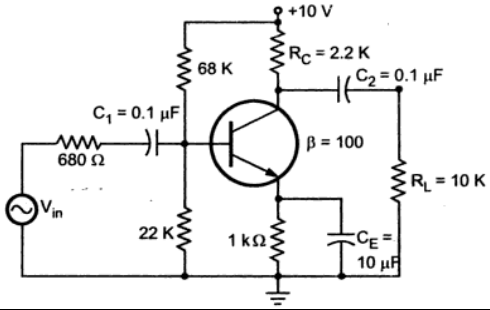
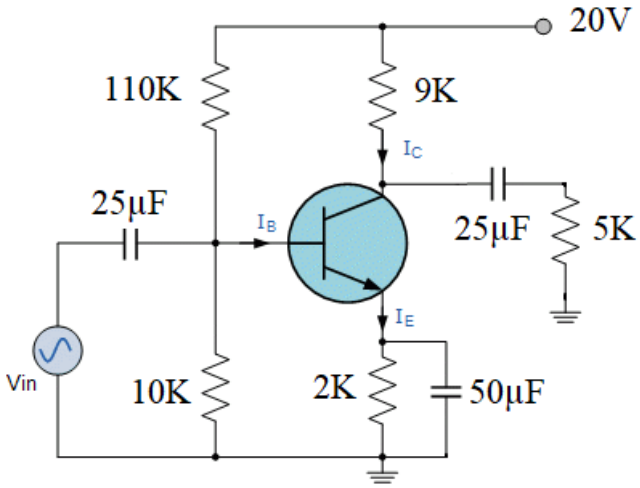
				
4.	Draw the small signal equivalent circuit for FET shown in the figure given below and hence find V_{O1}/V_i and V_{O2}/V_i in terms of circuit constants. 	(15)	BTL4	Analyzing
5.	Determine the small-signal voltage gain and input and output resistances of a common source MOSFET amplifier has the parameter are V_{DD} = 10 V, R_1 = 70 KΩ, R_2 = 29 KΩ, R_D = 5 KΩ, V_{TN} = 2 V, K_n = 0.5 mA/V^2 and λ = 0.01 V^{-1}. Assume R_s = 4 KΩ.s	(15)	BTL4	Analyzing

UNIT IV – FREQUENCY RESPONSE OF AMPLIFIERS			
Amplifier frequency response – Frequency response of transistor amplifiers with circuit capacitors – BJT frequency response – short circuit current gain - cut off frequency – fα, fβ and unity gain bandwidth – Miller effect - frequency response of FET - High frequency analysis of CE and MOSFET CS amplifier - Transistor Switching Times.			
PART – A			
Q. No.	**Question**	**BT Level**	**Competence**
1.	What is the effect of miller's capacitance on the frequency response of an amplifier?	BTL1	Remembering
2.	Define rise time. Give the relationship between bandwidth and rise time.	BTL1	Remembering
3.	List out the advantages of hybrid parameter.	BTL1	Remembering
4.	What is the need of cascading multistage amplifiers?	BTL1	Remembering
5.	Mention the reason for reduction in gain for lower and higher frequencies in case of amplifiers?	BTL1	Remembering
6.	If the rise time of a BJT is 35ns. Identify the bandwidth that can be obtained using this BJT.	BTL4	Analyzing
7.	Differentiate small signal equivalent & hybrid π equivalent circuit.	BTL2	Understanding
8.	Write the equation of overall lower and upper cutoff frequency of multistage amplifier.	BTL2	Understanding
9.	What is the main reason for the drop in gain at the low frequency region & high frequency region?	BTL2	Understanding
10.	Discuss the limitations of multistage amplifiers.	BTL2	Understanding
11.	For an amplifier, midband gain is 100 and lower cutoff frequency is 10KHz. Find the gain of an amplifier at frequency is 10Hz.	BTL3	Applying
12.	Write about the concept behind drop in gain at the low frequency region and at the high frequency region	BTL3	Applying
13.	Solve for the unity gain bandwidth of MOSFET whose g_m = 1.2m A/V, C_{gs} = 50 pF, C_{gd}= 10 pF, and C_{ds} = 1 pF.	BTL3	Applying
14.	Compare BJT and MOSFET Amplifiers.	BTL4	Analyzing
15.	The Short circuit CE current gain of transistor is 25 at a frequency of 2 MHz if f_β = 200 KHz Examine find $\|A_i\|$ at frequency of 10 MHz and 100 MHz.	BTL4	Analyzing
16.	Calculate the cut-off frequency due to the bypass capacitor in the given circuit.	BTL4	Analyzing

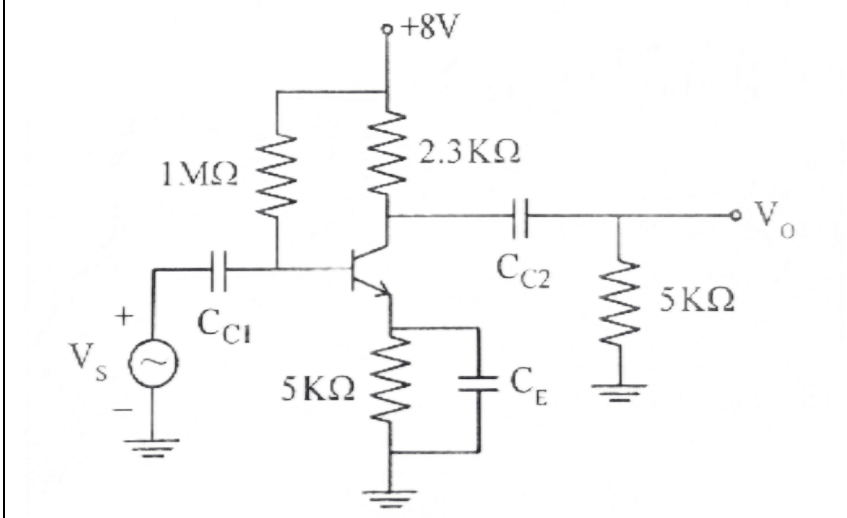
			
17.	Common base amplifier is preferred for high frequency signal when compared to CE amplifier. Justify.	BTL4	Analyzing
18.	What is meant by unit gain frequency and β cutoff frequency?	BTL1	Remembering
19.	Draw the hybrid π equivalent model of the BJT.	BTL3	Applying
20.	Write down the high frequency equivalent circuit model for MOSFET.	BTL4	Analyzing
21.	What are the various types of gate capacitances in MOSFET?	BTL1	Remembering
22.	Draw the general frequency response of an amplifier.	BTL4	Analyzing
23.	What is the relationship between bandwidth and risetime?	BTL1	Remembering
24.	If the rise time of a BJT is 40 ns, what is the bandwidth that can be obtained using this BJT?	BTL3	Applying

PART-B

1.	Describe with neat diagram and derive the expression for cut off frequency of a BJT.	(13)	BTL1	Remembering
2.	Explain the upper and lower cut off frequencies of multistage amplifier with expressions.	(13)	BTL1	Remembering
3.	How would you describe the relation between rise time, upper cut off frequency and bandwidth?	(13)	BTL1	Remembering
4.	Write the operation of high frequency common source FET amplifier with neat diagram? Derive the expression for i) Voltage gain ii) Input admittance iii) input capacitance iv) Output admittance.	 (4) (3) (3) (3)	BTL1	Remembering
5.	Summarize the expressions for the short circuit current gain of common emitter amplifier at a high frequency. Define alpha cut-off frequency, beta cut-off frequency and transition frequency and derive their values in terms of the circuit parameters.	(13)	BTL2	Understanding
6.	(i) Discuss in detail about the bandwidth of single stage amplifiers. (ii) Describe in detail about gain bandwidth product for voltage and current of BJT.	(7) (6)	BTL2	Understanding

7.	(i) Summarize alpha cut-off frequency, beta cut-off frequency and transition frequency. (ii) Summarize the expression for Low Frequency Analysis of BJT.	(7) (6)	BTL2	Understanding
8.	(i) Write a brief outline about multistage amplifiers. (ii) List out the advantages and applications of single stage and multistage amplifiers.	(8) (5)	BTL3	Applying
9.	Solve and obtain the low frequency response of the amplifier shown in fig. $h_{ie}=r_{\pi}=1.1K$. 	(13)	BTL3	Applying
10.	Calculate the bandwidth of the amplifier shown, r_b =100Ω, R_{π}= 1.1 K, Cπ= 3 pF, Cμ= 100 pF, h_{fe} = 225. 	(13)	BTL4	Analyzing
11.	For hybrid – π common emitter transistor model, derive the expression for input conductance (g_{be}) and output resistance (g_{ce}).	(13)	BTL4	Analyzing
12.	Derive the expression for an amplifier rise time and sag and their relation to upper cut-off frequencies	(13)	BTL4	Analyzing
13.	Consider a bipolar transistor that has the parameters f_T =20Ghz at I_C=1mA, β=120, Cμ=0.08pF, V_T=0.026V and g_m=38.5mA/V. Evaluate the values for the bandwidth and capacitance of a bipolar transistor.	(13)	BTL3	Applying
14.	Draw the high frequency equivalent circuit of a MOSFET from its	(13)	BTL4	Analyzing

	geometry and derive the expression for short circuit current gain in the common source configuration.			
15.	Analyze the following: (i) Overall Lower cut-off frequency of Multistage amplifier, (ii) Overall Higher cut-off frequency of multistage amplifier.	(7) (6)	BTL4	Analyzing
16.	A CS amplifier has $C_{C1} = C_S = C_{C2} = 1.2\ \mu F$, $R_G = 10\ M\Omega$, $R_S = 100\ K\Omega$, $g_m = 2$ mA/V, $R_D = R_L = 10\ K\Omega$. Find A_M, f_{p1}, f_{p2}, f_{p3} and f_L.	(13)	BTL4	Analyzing
17.	For the CE amplifier has the following parameters are $R_B = 100\ K\Omega$, $R_C = 8\ K\Omega$, $R_L = 5\ K\Omega$, $R_S = 5\ K\Omega$, $\beta_0 = 40$ mA/V, $r_\pi = 2.5\ K\Omega$, and $f_L = 100$ Hz. Determine C_{C1}, C_{C2} and C_E.	(13)	BTL4	Analyzing
	PART-C			
1.	Obtain the low frequency response and high frequency response of an amplifier, derive its cutoff frequency & discuss the terms rise time and sag.	(15)	BTL3	Applying
2.	Design the high frequency analysis of JFET with necessary circuit diagram& gain bandwidth product and explain the frequency response of MOSFET CS amplifier.	(15)	BTL3	Applying
3.	Determine the midband gain Am and upper 3dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance R_S=100KΩ. The amplifier has R_G=4.7MΩ, R_D=R_L=15KΩ, g_m=1mA/V, r_o=150KΩ, c_{gs}=1pF and c_{gd}=0.4pF.	(15)	BTL4	Analyzing
4.	Estimate the midband gain, input impedance, output impedance, bandwidth and maximum output voltage swing for the given NMOS transistor parameters are $\mu_n Cox(W/L)=0.5mA/V^2$, V_{GSQ}=3.25V, V_{th}=2V, λ=0, C_{gd}=0.1pF, C_{gs}=1pF, R_{G1}=234KΩ, R_{G2}=166KΩ, R_S=10KΩ, R_D=4KΩ, R_L=20KΩ, R_S=0.5KΩ (assume C_G=C_D=C_S=1pF).	(15)	BTL4	Analyzing
5.	For the circuit shown in figure has following parameters: $h_{fe} = 125$, $C_\pi = 24$ PF, $C_\mu = 3$ PF. (i) Determine its midband gain, upper – cut off frequency, (ii) Find the values of C_{c1}, C_{c2}, and C_E by assuming lower cut – off frequency of 100 Hz.	(7) (8)	BTL4	Analyzing



UNIT V – POWER SUPPLIES AND ELECTRONIC DEVICE TESTING

Linear mode power supply - Rectifiers - Filters - Half-Wave Rectifier Power Supply - Full-Wave Rectifier Power Supply - Voltage regulators: Voltage regulation - Linear series, shunt and switching Voltage Regulators - Over voltage protection - BJT and MOSFET – Switched mode power supply (SMPS) - Power Supply Performance and Testing - Troubleshooting and Fault Analysis, Design of Regulated DC Power Supply.

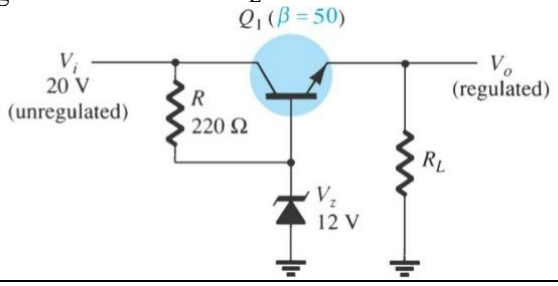
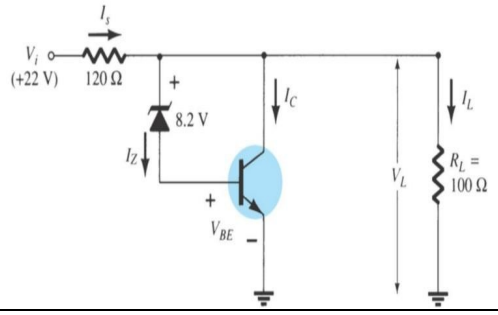
PART-A

Q.No.	Question	BT Level	Competence
1.	What is the necessity of bleeder resistor?	BTL 4	Analyzing
2.	What is meant by ripple factor?	BTL 1	Remembering
3.	List the advantages and disadvantages of Half wave rectifier.	BTL 1	Remembering
4.	Write the expression for ripple factor of FWR.	BTL 1	Remembering
5.	What is filter?	BTL 1	Remembering
6.	Why capacitor input filter is not suitable for variable loads?	BTL 1	Remembering
7.	Describe operation of CLC filter.	BTL 2	Understanding
8.	Using a dc and ac voltmeter to measure the output signal from a filter circuit, we obtain readings of 25V DC and 1.5V rms. Solve the ripple of the filter output voltage.	BTL 2	Understanding
9.	Estimate the ripple voltage of a full-wave rectifier with a100mF filter capacitor connected to a load drawing 50 mA.	BTL 2	Understanding
10.	Write down the Transformer Utilization Factor TUF of HWR and FWR.	BTL 2	Understanding
11.	Define Voltage regulation?	BTL 1	Remembering

12.	A DC voltage supply provides 60V when the output is unloaded. When connected to a load, the output drops to 56V. Calculate the value of voltage regulation.	BTL 4	Analyzing
13.	Why unregulated power supply is notsuitable for many application.	BTL 2	Understanding
14.	How to decrease the ripple factor?	BTL 3	Applying
15.	Why protection circuit is required for the regulator?	BTL 2	Understanding
16.	What is meant by switched mode power supply?	BTL 3	Applying
17.	Compare the SMPS with linear power supply.	BTL 4	Analyzing
18.	Why a simple capacitor filter is not suitable for heavy loads.	BTL 3	Applying
19.	How shunt regulator is differentiated from series regulator?	BTL 4	Analyzing
20.	Draw the circuit diagram of RPS.	BTL 3	Applying
21.	List the Application of full wave rectifier.	BTL 2	Understanding
22.	What are the advantage of SMPS?	BTL 1	Remembering
23.	Draw the block diagram of SMPS.	BTL 3	Applying
24.	Why capacitor input filter is not suitable for variable load?	BTL 4	Analyzing

PART-B

1.	(i) Explain the construction and operation of Half wave rectifier with suitable diagrams and waveforms. (ii) List its merits and demerits.	(10) (3)	BTL 1	Remembering
2.	(i) Describe the working of a rectifier whose TUF is 0.693 with supporting diagrams. (ii) State its advantages and disadvantages.	(10) (3)	BTL 4	Analyzing
3.	(i)With the help of circuit diagram and waveforms, explain the operation of bridge rectifiers (ii) Point out its advantages and disadvantages	(10) (3)	BTL 1	Remembering
4.	(i) Explain the working of C filter with Full wave rectifier (ii) Derive the expression for its ripple factor.	(7) (6)	BTL 1	Remembering
5.	(i) With a neat diagram describe the operation of L filter? (ii) Derive the expression for its ripple factor.	(7) (6)	BTL 2	Understanding
6.	(i) With a neat diagram describe the operation of CLC filter? (ii) Derive the expression for its ripple factor.	(7) (6)	BTL 2	Understanding

7.	What is shunt voltage regulator? Discuss about itsworking with necessary diagrams.	(13)	BTL 2	Understanding
8.	With the help of neat circuit diagrams, explain the construction and operation of series voltage regulator.	(13)	BTL 3	Applying
9.	Calculate the output voltage and the Zener current in the given regulator circuit for R_L = 1 kΩ.  	(13)	BTL 4	Analyzing
10.	Describe in detail about the following (i)Short circuit Protection (ii)Current limiting circuits	 (7) (6)	BTL 1	Remembering
11.	Calculate the parameters of the regulated voltage and circuit currents for the shown shunt regulator.  	(13)	BTL 3	Applying
12.	Explain how the pulse width modulation is applied in Switched mode Power supply?	(13)	BTL 3	Applying
13.	Analyse the following protection circuit that could be applied to voltage regulator. (i) Fold back limiting circuit (ii) Over Voltage Protection	 (7) (6)	BTL 4	Analyzing
14.	How to do Power Supply Performance and Testing in Power supply unit.	(13)	BTL 3	Applying
15.	A full wave rectifier a signal of 300v at 50 Hz is applied at the input. Each diode has an internal resistance of 800Ω.If the load is 2000Ω, calculate i) Instant peak value of current in the output ii) Output DC current iii) Efficiency of power transfer	 (5) (4) (4)	BTL 4	Analyzing
16.	With neat circuit diagrams, explain the Fault Analysis method.	(13)	BTL 3	Applying

17.	Explain how the power supply unit problem eliminates using the Troubleshooting method.	(13)	BTL 3	Applying
	PART-C			
1.	Drive the full wave rectifiers parameters I_{dc}, E_{dc}, I_{rms}, P_{dc}, P_{ac}, Rectifier efficiency, ripple factor, PIV and TUF parameters.	(15)	BTL 3	Applying
2.	What is Rectifier circuit? Explain full wave rectifier circuit operation with circuit and wave forms.	(15)	BTL 2	Understanding
3.	Estimate a power supply unit for a System needs to be powered with a 12V dc source of maximum load current 150mA. Design a circuit to supply power with the available domestic a.c. line. Assume any data required, but reasonably. Provide short circuit protection.	(15)	BTL 4	Analyzing
4.	Design a bridge rectifier is applied with input from a step down transformer having turns ratio 8:1 and input 230V, 50Hz.If the $R_f = 1\Omega$, $R_S = 1\Omega$ and $R_L = 2k\Omega$. Find DC power output, PIV across each diode, Percentage efficiency and percentage regulation at full load.	(15)	BTL 4	Analyzing
5.	Design a DC power supply unit 9V DC source of maximum load current 100mA with the available domestic AC line assume data required, but reasonably provide short circuit protection.	(15)	BTL 4	Analyzing