# SRM VALLIAMMAI ENGINEERING COLLEGE

**(An Autonomous Institution)**

**SRM Nagar, Kattankulathur – 603 203**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

## QUESTION BANK

**III SEMESTER**

# 1906303 DIGITAL ELECTRONICS

(Common to ECE & Medical Electronics)

Academic Year 2022 – 2023 (ODD Semester)

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**QUESTION BANK**

**SUBJECT CODE/NAME : 1906303 / DIGITAL ELECTRONICS**

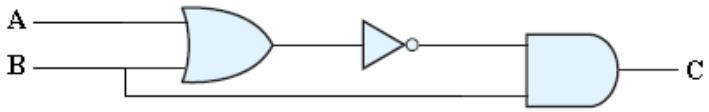
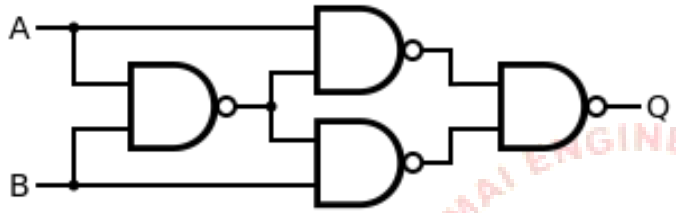
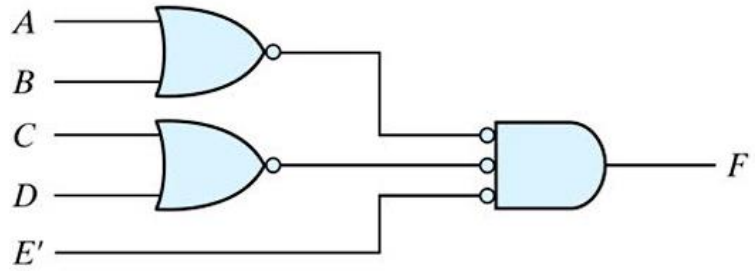
**YEAR / SEMESTER : II / III**

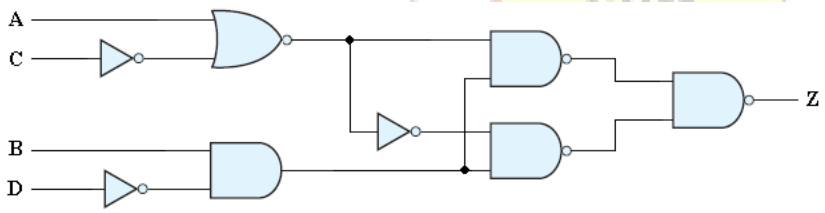
**UNIT I DIGITAL FUNDAMENTALS**

Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map Minimization and Quine-McCluskey method of minimization.

**PART A**

| Q.No | Questions | BT Level | Domain |
|---|---|---|---|
| 1. | Convert the given decimal numbers into their binary equivalent 108.364. | BTL 3 | Applying |
| 2. | Express the function $Y = A + \overline{B}C$ in canonical POS. | BTL 2 | Understanding |
| 3. | Convert the pair of decimal number to BCD and Add $(65)_{10}+(58)_{10}$ | BTL 3 | Applying |
| 4. | Outline the concept of duality in Boolean algebra. | BTL 1 | Remembering |
| 5. | Convert $A3B_H$ and $2F3_H$ into Binary and Octal respectively | BTL 3 | Applying |
| 6. | Simplify the following Boolean expression into one literal.<br>W'X (Z'+YZ) + X (W+Y'Z). | BTL 4 | Analyzing |
| 7. | Convert $(115)_{10}$ and $(235)_{10}$ into hexadecimal numbers. | BTL 4 | Analyzing |
| 8. | Define 'Minterm' and 'Maxterm'. | BTL 1 | Remembering |
| 9. | Find Excess-3 code for the following decimal numbers. $(18)_{10}$ and $(56)_{10}$. | BTL 1 | Remembering |
| 10. | Draw the active high tri-state Gate & write its truth table. | BTL 1 | Remembering |
| 11. | Show how to connect NAND gates to get an AND gate and OR gate? | BTL 2 | Understanding |
| 12. | Write the principle of Distributive law. | BTL 1 | Remembering |
| 13. | What is meant by Prime Implicants and Essential prime implicants? | BTL 1 | Remembering |
| 14. | How can we minimize Boolean expression of the below function?<br>F=XY+X(Y+Z) +Y(Y+Z). | BTL 3 | Applying |
| 15. | Implement the given function using NAND gates only.<br>F(X, Y, Z) =$\sum m(0,6)$. | BTL 2 | Understanding |
| 16. | Identify the equivalent Gray code for $[10110]_2$. | BTL 2 | Understanding |
| 17. | If A & B are Boolean variables and if A=1 &$\overline{A + B}$=0, determine B? | BTL 4 | Analyzing |

| | | | | |
|---|---|---|---|---|
| 18. | Apply De-Morgan's theorem to simplify $\overline{A + B\overline{C}}$. | | BTL 3 | Applying |
| 19. | Implement Y= $\sum(1,4,5,6,7)$ in SOP form using AOI logic. | | BTL 4 | Analyzing |
| 20. | Determine the Boolean expression for the output of the system shown in figure.<br>  | | BTL 2 | Understanding |
| 21. | Perform 2's complement subtraction of 010110 – 100101. | | BTL 4 | Analyzing |
| 22. | Identify the Boolean function and the truth table of the given logic.<br>  | | BTL 2 | Understanding |
| 23. | Write the Boolean expression for the output of the system shown in figure<br>  | | BTL3 | Applying |
| 24. | Reduce the expression $A\overline{B}C + \overline{A}\overline{B}C$ using Boolean theorems. | | BTL 4 | Analyzing |
| | **PART – B** | | | |
| 1. | Find the Minimized logic function using K-Maps.<br>F (A, B, C, D) =$\sum m(1,3,5,8,9,11,15) + d(2,13)$. Implement the minimal SOP using NAND and NOR gates. | (13) | BTL3 | Applying |
| 2. | (i) Simply the function F(A,B,C,D,E) = m(1,4,6,10,20,22,24,26)+d(0,11,16,27) using K-map method. Draw the circuit of the minimal expression using Basic gates.<br>(ii) Write about Excess 3 and Gray Code with an example. | (7)<br>(6) | BTL 1 | Remembering |
| 3. | Analyze the given function Y (M, N, O, P, Q) = $\sum m(0,2,4,6,9,13,21,23,25,29,31)$. Draw the K-map and implement the simplified expression using basic gates. | (13) | BTL 4 | Analyzing |

| | | | | |
|---|---|---|---|---|
| 4. | Minimize the following Boolean expressions using Boolean Algebra and draw the logic diagram.<br>(i) F (X, Y, Z) =$(X+Y)\left(\overline{X(\overline{Y}+\overline{Z})}\right)+\overline{XY}+\overline{XZ}$.<br>(ii) F (X, Y, Z) =$\overline{XY}Z+\overline{X}YZ+X\overline{Y}$<br>(iii) F(X,Y,Z) =$XYZ+\overline{X}Z+YZ$ | (5)<br>(4)<br>(4) | BTL 2 | Understanding |
| 5. | Explain the different types of codes and conversion with your own example. | (13) | BTL 1 | Remembering |
| 6. | Using K-map method, Reduce the following Boolean function F=∑m (0,2,3,6,7) + d (8,10,11,15) and obtain minimal SOP. | (13) | BTL 4 | Analyzing |
| 7. | Write the minimized Boolean expression for the function using K-map and draw the logic diagram.<br>F (w, x, y,z)=$\sum m(0,1,2,4,5,6,8,9,12,13,14)$. | (13) | BTL 1 | Remembering |
| 8. | (i) Plot the following logical Expression on a 4-variable K – map F=ABCD+AB'C'D'+AB'C+AB & realize the SOP using only NAND gates and POS using only NOR gates.<br>(ii) Simplify the logic shown in figure<br>  | (7)<br>(6) | BTL 3 | Applying |
| 9. | Elaborate the minimization of the given Boolean function using Quine-Mc-Cluskey method F=∑m (0,1,2,5,7,8,9,10,13,15). Realize the simplified function using logic gates. | (13) | BTL 4 | Analyzing |
| 10. | Using K-map method, simplify the given Boolean function and obtain minimum POS expression and draw the logic diagram.<br>X=$\prod M(1,3,5,7,9)+\prod d(8,11,15)$. | (13) | BTL 2 | Understanding |
| 11. | Prepare Karnaugh Map for the following functions and draw the logic diagram using basic gates.<br>(i) Y (A, B,C,D)=$\prod M(0,3,4,9,10,12)+\prod d(2,7,8,13)$<br>(ii) Y (A, B, C) =$\prod M(0,2,4,5,6)$ | (7)<br>(6) | BTL 4 | Analyzing |
| 12. | Develop the following Function using Tabulation method F=∑ (1,2,3,7,8,9,10,11,14,15) and realize the circuit using only NAND Gates. | (13) | BTL 4 | Analyzing |
| 13. | (i) Convert $(725.25)_8$ to its decimal, binary and Hexadecimal equivalent.<br>(ii) Find 1's and 2's Complement of 8-digit binary number 10101101. | (7)<br>(6) | BTL 1 | Remembering |

| | | | | |
|---|---|---|---|---|
| 14. | (i) Implement Y=$(A + C)(A + \overline{D})(A + B + \overline{C})$<br>(ii) Solve by perfect induction<br>(a) A+AB = A<br>(b) A(A+B) = A<br>(c) A+A'B = A+B and<br>(d) A(A'+B) =AB | (5)<br>(8) | BTL 3 | Applying |
| 15. | Simplify the following Boolean function using K-map and implement the same using only NAND gates.<br>F(A, B, C, D) = (D'+A'B'C' + AB'C' + A'BC'D). | (13) | BTL 2 | Understanding |
| 16. | Determine simplified SOP for the following Boolean function using Quine- McCluskey Method and realize using NAND gates.<br>F(A, B, C, D) = ∑m(1, 3, 4, 5, 9, 10, 11) + ∑d(6, 8). | (13) | BTL 3 | Applying |
| 17. | Implement the given Boolean function using tabulation method and verify with K-map.<br>F(A, B, C, D) = ∑m(1, 2, 3, 5, 7, 9, 10, 11, 13, 15) | (13) | BTL 4 | Analyzing |
| | **PART C** | | | |
| 1. | Design the given function using Prime implicant method and Verify your result using K map F=$\sum m(0,1,2,4,5,6,8,9,12,13,14)$. | (15) | BTL 3 | Applying |
| 2. | A staircase light is controlled by two switches, one is at the top of the stairs and the other is at the bottom of the stairs:<br>(i) Make a truth table for this system.<br>(ii) Write the logic function in SOP form.<br>(iii) Realize the circuit using AOI logic.<br>(iv) Realize the circuit using minimum number of NAND and NOR gates. | (3)<br>(3)<br>(4)<br>(5) | BTL 4 | Analyzing |
| 3. | Determine the minimal Sum of Products for the following function F(w,x,y,z)=∑m(1,3,4,5,9,10,11)+∑d(3,4,11) using Quine McCluskey method and apply DeMorgan's theorem for NAND -NOR implementation. | (15) | BTL 2 | Understanding |
| 4. | Construct a Karnaugh Map for the following function F(A,B,C,D,E)= $\sum(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)$ and draw the logic diagram. | (15) | BTL 1 | Remembering |
| 5. | Find the MSP and MPS form of the function<br>F = ∑m(0, 2, 6 ,8, 10, 12, 14, 15) and implement using basic gates. | (15) | BTL 4 | Analyzing |

## UNIT II COMBINATIONAL CIRCUIT DESIGN

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Magnitude Comparator, Decoder, Encoder, Priority Encoder.

### PART A

| Q.No | Questions | BT Level | Domain |
|---|---|---|---|
| 1. | What is meant by combinational circuits? | BTL 1 | Remembering |
| 2. | Enumerate some of the combinational circuits. | BTL 2 | Understanding |
| 3. | Summarize the design procedure of combinational circuits. | BTL 2 | Understanding |
| 4. | Write the Boolean expression for a half adder. | BTL 1 | Remembering |
| 5. | How do you draw a full adder circuit? | BTL 3 | Applying |
| 6. | From the truth table derive the logic equation of a half subtractor. | BTL3 | Applying |
| 7. | Suggest a solution to overcome the limitation on the speed of an adder. | BTL 4 | Analyzing |
| 8. | Differentiate between half adder and full adder. | BTL 4 | Analyzing |
| 9. | Why is MUX called data selector? | BTL 4 | Analyzing |
| 10. | List out the applications of multiplexer. | BTL 1 | Remembering |
| 11. | Mention the uses of demultiplexer. | BTL 2 | Understanding |
| 12. | Can a decoder function as a demultiplexer? | BTL 4 | Analyzing |
| 13. | What do you mean by comparator? | BTL 1 | Remembering |
| 14. | What will be the maximum number of outputs for a decoder with a 6-bit data word? | BTL3 | Applying |
| 15. | Identify the function of select inputs of a MUX. | BTL 2 | Understanding |
| 16. | Draw the schematic diagram of 2X1 multiplexer. | BTL 2 | Understanding |
| 17. | Distinguish between a demultiplexer and decoder. | BTL 4 | Analyzing |
| 18. | Implement the given function using multiplexer. $F(x,y,z)=\sum(0,2,6,7)$. | BTL3 | Applying |
| 19. | What is a priority encoder? | BTL 1 | Remembering |
| 20. | State the uses of encoder. | BTL 1 | Remembering |
| 21. | Outline the characteristics of a priority encoder and how it differs from a regular encoder? | BTL 4 | Analyzing |
| 22. | Sketch the logic diagram of 2 to 4 decoder. | BTL 2 | Understanding |
| 23. | Implement the Boolean function $F=\sum m(1,2,3,7)$ using 3:8 decoder. | BTL3 | Applying |
| 24. | Design a 1-bit comparator using basic gates. | BTL3 | Applying |

| PART – B | | | | |
|---|---|---|---|---|
| 1. | (i)Explain the design procedure for combinational circuits.<br>(ii) Design a combinational logic circuit with three input variables that will produce a logic 1 output when more than one input variables are logic 1. | (3)<br>(10) | BTL3 | Applying |
| 2. | Write the truth table for full adder, reduce the equation using k-map and design full adder using logic gates. | (13) | BTL 1 | Remembering |
| 3. | Explain how full adder can be designed by using two half adder circuits. Draw the circuit diagram. | (13) | BTL 2 | Understanding |
| 4. | Write a brief note on the following combinational circuits:<br>(i) Half subtractor<br>(ii) Full subtractor | (5)<br>(8) | BTL 1 | Remembering |
| 5. | Explain the working of 4-bit parallel adder with necessary diagram and example. | (13) | BTL 1 | Remembering |
| 6. | Design a 4-bit BCD adder and compute the circuit to add 1001 and 0101. Write the sum and carry output of the given binary number. | (13) | BTL 4 | Analyzing |
| 7. | From the truth table derive the Boolean expression for 4:1 MUX and 8:1 MUX and implement using basic gates. | (13) | BTL 2 | Understanding |
| 8. | Implement the following Boolean function using 8X1 multiplexer.<br>F(A,B,C,D)=$\bar{A}B\bar{D}$+ACD+$\bar{B}$CD+$\bar{A}\bar{C}$D | (13) | BTL 3 | Applying |
| 9. | (i) Analyze the design of 8 x 1 multiplexer using only 2 x 1 multiplexer.<br>(ii) Formulate the following Boolean function using 4 x 1 multiplexers.<br>$F(A,B,C,D) = \sum(1,2,3,6,7,8,11,12,14)$ . | (7)<br>(6) | BTL 4 | Analyzing |
| 10. | Realize the function F(w, x, y, z)= Σ (1,4,6,7,8,9,10,11,15) using 4 to 1 Multiplexer. | (13) | BTL 2 | Understanding |
| 11. | Describe about multiplexer and Simplify the following function using 8x1 Mux F(A,B,C,D)=∑m(0,2,6,10,11,12,13)+d(3,8,14) | (13) | BTL 4 | Analyzing |
| 12. | (i) Draw and explain the working of 1:8 demultiplexer and realize it using basic gates?<br>(ii) Implement the following functions using demultiplexer:<br>F1(A,B,C)=∑m(0,3,7)<br>F2(A,B,C)=∑$m(1,2,5)$ | (7)<br>(6) | BTL 4 | Analyzing |
| 13. | Discuss the concept of priority encoder with truth table, Boolean expression and logic diagram. | (13) | BTL 1 | Remembering |
| 14. | Design a certain logic circuit using 4x1 Multiplexer which has four inputs A, B, C, and D. The output X of the circuit is logic 1 if two or more inputs are logic 1. | (13) | BTL 3 | Applying |
| 15. | Derive the circuit that implements an 8-to-3 binary encoder with neat diagram. | (13) | BTL 2 | Understanding |

| | | | | |
|---|---|---|---|---|
| 16. | Discuss about the purpose of decoder and implement a full adder and full subtractor using decoder. | (13) | BTL 3 | Applying |
| 17. | (i) Design and implement the circuit using multiplexer which has 3 inputs (A,B,C) and one output Z. The output is HIGH, when the input is less than 3, otherwise 0.<br>(ii) Implement the function f(w1, w2, w3) = ∑m(0, 1, 3, 4, 6, 7) by using a 3-to-8 binary decoder and an OR gate. | (7)<br><br>(6) | BTL 4 | Analyzing |
| | **PART C** | | | |
| 1. | With necessary diagrams, explain in detail about the working of a 4-bit look ahead carry adder. Also mention its advantages over conventional adder. | (15) | BTL 4 | Analyzing |
| 2. | Implement the following Boolean function using an 8:1 multiplexer considering D as the input and A,B,C as selection lines :<br>F( A, B, C, D) =AB'+BD+B'CD' | (15) | BTL 3 | Applying |
| 3. | Develop the following functions:<br>(i) Full adder using multiplexer.<br>(ii) Full subtractor using demultiplexer. | (8)<br>(7) | BTL 2 | Understanding |
| 4. | Find the Boolean expression from the truth table of 2 to 4 decoder & 3 to 8 decoder and draw the logic diagram. | (15) | BTL 1 | Remembering |
| 5. | Design a 2-bit magnitude comparator with three outputs: A>B, A=B and A<B. | (15) | BTL 4 | Analyzing |

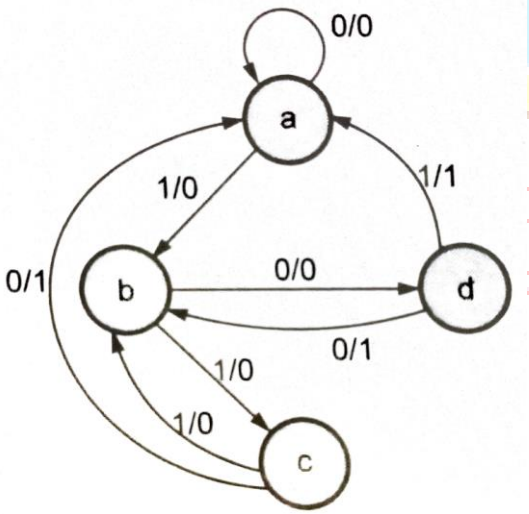
**UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS**

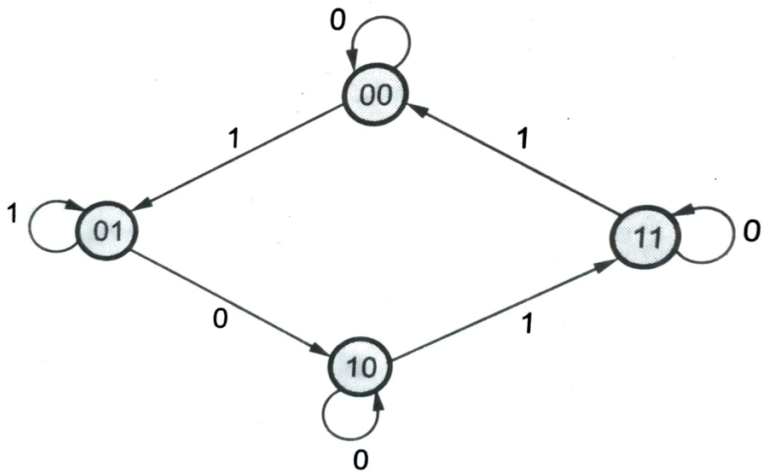
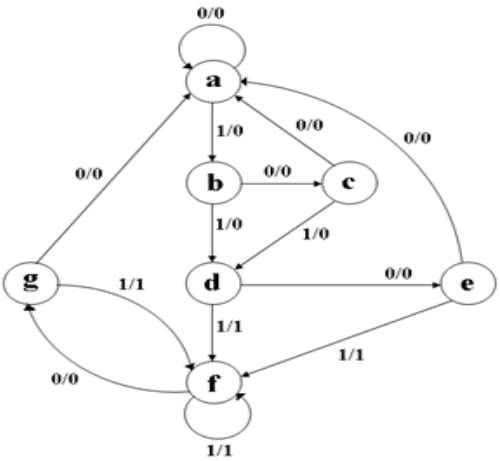
Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, state minimization, state assignment, circuit implementation – Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

**PART A**

| Q.No | Questions | BT Level | Domain |
|---|---|---|---|
| 1. | List the classification of Sequential circuits. | BTL 1 | Remembering |
| 2. | Distinguish between combinational and sequential circuits. | BTL 2 | Understanding |
| 3. | Define a flip-flop. | BTL 1 | Remembering |
| 4. | What are the four types of flip-flop? | BTL 1 | Remembering |
| 5. | Differentiate between latch and flip-flop. | BTL 2 | Understanding |
| 6. | Write the excitation table for JK Flip flop. | BTL 1 | Remembering |

| | | | | |
|---|---|---|---|---|
| 7. | Draw the state transition diagrams of flip-flops. | | BTL 2 | Understanding |
| 8. | Derive the characteristic equation from the truth table of SR flip-flop. | | BTL 2 | Understanding |
| 9. | Convert D flip-flop to T flip-flop. | | BTL3 | Applying |
| 10. | Mention any two differences between the edge triggering and level triggering. | | BTL 2 | Understanding |
| 11. | Write down the characteristic equation and truth table for D flip-flop. | | BTL 1 | Remembering |
| 12. | Interpret the significance of state assignment. | | BTL 2 | Understanding |
| 13. | Draw the state diagram of Mod-10 counter. | | BTL 4 | Analyzing |
| 14. | Sketch the circuit diagram of ring Counter. | | BTL 4 | Analyzing |
| 15. | How many flip-flops are required to build a binary counter that counts from 0 to 1023? | | BTL3 | Applying |
| 16. | State the difference between Mealy and Moore state machines. | | BTL 4 | Analyzing |
| 17. | Compute the minimum number of flip-flops needed to design a counter of Modulus 10. | | BTL3 | Applying |
| 18. | List out the applications of shift registers. | | BTL 1 | Remembering |
| 19. | Distinguish between synchronous sequential circuits and asynchronous sequential circuits. | | BTL 4 | Analyzing |
| 20. | Model a NAND based logic diagram of JK FF. | | BTL3 | Applying |
| 21. | Define universal shift register. | | BTL 1 | Remembering |
| 22. | Classify the types of shift registers. | | BTL3 | Applying |
| 23. | A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. calculate the Q output. | | BTL 4 | Analyzing |
| 24. | Draw the 4-bit Johnson counter. | | BTL 4 | Analyzing |
| | **PART – B** | | | |
| 1. | (i)What is Flip flops? Write about the operations of different flip flops.<br>(ii) List the application of Flip flop. | (10)<br>(3) | BTL 1 | Remembering |
| 2. | Describe about JK flip-flop with truth table, characteristic equation and input & output waveforms. | (13) | BTL 2 | Understanding |
| 3. | Realize SR flip-flop using D flip-flop and JK flip-flop. | (13) | BTL3 | Applying |
| 4. | (i) Explain the steps for the design of clocked synchronous sequential circuit.<br>(ii) Reduce the following state table and tabulate the reduced state table. | (6)<br>(7) | BTL 2 | Understanding |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | Present state | Next State | | Output | | | |
| | | | X = 0 | X =1 | X =0 | X=1 | | |
| | | a | f | b | 0 | 0 | | |
| | | b | d | c | 0 | 0 | | |
| | | c | f | e | 0 | 0 | | |
| | | d | g | a | 1 | 0 | | |
| | | e | d | c | 0 | 0 | | |
| | | f | f | b | 1 | 1 | | |
| | | g | g | h | 0 | 1 | | |
| | | h | g | a | 1 | 0 | | |
| 5. | Explain the functions with the state diagram and characteristics equation of T FF. | | | | | | (13) | BTL 1 | Remembering |
| 6. | Develop a state table, characteristic table and an excitation table for SR Flip Flop. | | | | | | (13) | BTL 1 | Remembering |
| 7. | Design a clocked sequential machine using T flip-flops for the following state diagram. Use state reduction if possible. Also use straight binary state assignment.   | | | | | | (13) | BTL 4 | Analyzing |
| 8. | Illustrate the design procedure of a MOD-5 synchronous counter using JK flip-flops and implement it. | | | | | | (13) | BTL 4 | Analyzing |
| 9. | Using D flip-flop, design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000. | | | | | | (13) | BTL3 | Applying |
| 10. | Using SR flip flops, design a counter which counts in the following sequence 000,111,1101,100,011,010,001, 000,….. | | | | | | (13) | BTL3 | Applying |

| | | | | |
|---|---|---|---|---|
| 11. | Develop a counter to count the sequence 0,1,2,4,5,6 using SR FFs. | (13) | BTL 4 | Analyzing |
| 12. | Implement a J-K counter for the states 3, 4, 6, 7 and 3. | (13) | BTL3 | Applying |
| 13. | Describe the operation of universal shift register with neat block diagram. | (13) | BTL 1 | Remembering |
| 14. | Explain in detail about the working of mod-3 counter with neat diagram. | (13) | BTL 2 | Understanding |
| 15. | Discuss about the operation of 4-bit ring counter with waveforms. | (13) | BTL 2 | Understanding |
| 16. | Illustrate the design of a synchronous decade counter using D flip-flop. | (13) | BTL3 | Applying |
| 17. | Design a synchronous sequential circuit using JK Flip-flop for the given state diagram.<br>  | (13) | BTL 4 | Analyzing |
| | **PART C** | | | |
| 1. | Design a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible.<br>  | (15) | BTL 3 | Applying |

| | | | | |
|---|---|---|---|---|
| 2. | Design a BCD ripple counter using JK flip-flop and draw the logic diagram. | (15) | BTL 3 | Applying |
| 3. | Devise a model of a D FF counter for the states 1, 5, 8,9,10, 11 with necessary diagram. | (15) | BTL 2 | Understanding |
| 4. | Design and implement 4-bit binary counter (using D flip-flop) which counts all possible odd numbers only. | (15) | BTL 1 | Remembering |
| 5. | Analyze the operation of 4-bit SISO SIPO, PIPO and PISO shift register and draw its waveforms. | (15) | BTL 4 | Analyzing |

## UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

Stable and Unstable states, output specifications, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Pulse mode sequential circuits, Design of Hazard free circuits.

**PART A**

| Q.No | Questions | BT Level | Domain |
|---|---|---|---|
| 1. | Mention the steps for the design of asynchronous sequential circuit. | BTL 2 | Understanding |
| 2. | Classify Asynchronous sequential circuits. | BTL 3 | Applying |
| 3. | Differentiate between fundamental mode and pulse mode sequential circuits | BTL 4 | Analyzing |
| 4. | Define dynamic hazard. When do they occur? | BTL 1 | Remembering |
| 5. | What are pulse mode circuits? | BTL 1 | Remembering |
| 6. | Distinguish between stable and unstable state. | BTL 3 | Applying |
| 7. | Specify the significance of state assignment. | BTL 2 | Understanding |
| 8. | What is the role of asynchronous sequential circuit in digital design? | BTL 1 | Remembering |
| 9. | Draw the general model of ASM. | BTL 3 | Applying |
| 10. | Define Hazards. How it can be avoided? | BTL 1 | Remembering |
| 11. | Compare the ASM chart with a conventional flow chart. | BTL 4 | Analyzing |
| 12. | With an example interpret the critical race condition in asynchronous sequential circuits. | BTL 4 | Analyzing |
| 13. | Outline the causes of essential Hazard. | BTL 2 | Understanding |
| 14. | Distinguish between critical race and non-critical race. | BTL 2 | Understanding |
| 15. | Outline the characteristics of critical race. | BTL 2 | Understanding |
| 16. | List the different techniques used in State assignment. | BTL 1 | Remembering |

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| 17. | Identify the most important consideration in making state assignments for asynchronous network. | | BTL 1 | Remembering |
| 18. | List the types of hazards. | | BTL 1 | Remembering |
| 19. | Summarize the methods for critical-race free state assignment. | | BTL 4 | Analyzing |
| 20. | How can a race in digital circuits can be avoided? | | BTL 3 | Applying |
| 21. | State the term state machine. | | BTL 2 | Understanding |
| 22. | Why Hazard free design is preferred? | | BTL 4 | Analyzing |
| 23. | Contrast cycles and races. | | BTL 1 | Remembering |
| 24. | Is the state reduction modifies the circuit operation? Justify your answer. | | BTL 3 | Applying |
| | **PART – B** | | | |
| 1. | Analyze an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 and C moves from 1 to 0. Otherwise, the output is 0. | (13) | BTL 4 | Analyzing |
| 2. | What are the types of hazards? Check whether the following circuit contains a hazard or not $Y = X_1X_2 + X_2'X_3$. If the hazard is present, Demonstrate its removal. | (13) | BTL 2 | Understanding |
| 3. | An asynchronous sequential circuit is described by the following excitation and output function. Y= X1X2+(X1+X2) Y, Z=Y.<br>(i) Draw the logic diagram.<br>(ii) Derive the transition table and output map.<br>(iii) Illustrate the behavior of the circuit | <br>(3)<br>(5)<br>(5) | BTL 3 | Applying |
| 4. | (i) What is a Hazard? Give hazard free realization for the following Boolean function. F (A, B, C, D) = ∑m (1,5,6,7) using AND- OR gate network.<br>(ii) Define Essential Hazards. | (10)<br>(3) | BTL 1 | Remembering |
| 5. | (i) Summarize the design procedure for an asynchronous sequential circuit.<br>(ii) Deduce the state table of serial binary adder with neat diagram. | (10)<br>(3) | BTL 4 | Analyzing |
| 6. | Design a circuit that has no static hazards and implement the Boolean function F(A,B,C,D) = Σ (0,2,6,7,8,10,12) using AND-OR logic. | (13) | BTL 3 | Applying |
| 7. | Identify the problems arises in an asynchronous sequential circuit and explain any two problems in detail. | (13) | BTL 1 | Remembering |
| 8. | (i) Illustrate in detail about Races.<br>(ii) Explain the different methods of state assignment. | (5)<br>(8) | BTL 2 | Understanding |

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| 9. | (i) Explain ASM chart for binary multiplier.<br>(ii) What is Hazard? Explain about Static hazard, dynamic hazard and essential hazard. | (7)<br>(6) | BTL 3 | Applying |
| 10. | Describe how a state graph for a sequential machine can be convened to an equivalent ASM chart? | (13) | BTL 1 | Remembering |
| 11. | Illustrate about different hazards that occur in sequential circuits and also about the way to eliminate them. | (13) | BTL 2 | Understanding |
| 12. | What is the objective of state assignment in an asynchronous circuit? Give example circuit for hazard free realization. | (13) | BTL 1 | Remembering |
| 13. | Classify the methods of Race Free State assignment and explain in detail. | (13) | BTL 3 | Applying |
| 14. | Design an Asynchronous sequential circuit with input A and B and an output Y. Initially at any time if both the inputs are 0, the output, Y=0. When A or B = 1, Y =1. When the other input also become 1, Y=0. The output stays at 0 until circuit goes back to initial state. | (13) | BTL 4 | Analyzing |
| 15. | Explain in detail about state table, stable and unstable state with examples. | (13) | BTL 4 | Analyzing |
| 16. | Write note about the following with example:<br>(i) State Machine<br>(ii) Cycles<br>(iii) Races<br>(iv) Hazards | <br>(3)<br>(3)<br>(3)<br>(4) | BTL 2 | Understanding |
| 17. | How the Hazard free circuit is designed? Explain with suitable example. | (13) | BTL 3 | Applying |
| | **PART C** | | | |
| 1. | Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X. | (15) | BTL 4 | Analyzing |
| 2. | With suitable state reduction table and state diagram explain an asynchronous sequential circuit. | (15) | BTL 2 | Understanding |
| 3. | Develop an asynchronous D- type latch with two inputs C and D and output Q. Assume fundamental mode of operation. | (15) | BTL 4 | Analyzing |
| 4. | Construct a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z = 1 it will remain so until A goes to 0. Draw timing diagram, state diagram and Primitive flow table for designing the circuit. | (15) | BTL 3 | Applying |
| 5. | Assess an asynchronous circuit that will output only the first pulse received and will ignore any other pulses. | (15) | BTL 3 | Applying |

## UNIT - V MEMORY DEVICES AND INTRODUCTION TO HDL PROGRAMMING

Basic memory structure- ROM-PROM-EPROM-EEPROM-EAPROM, RAM – Static and Dynamic RAM-Programmable Logic Devices-Programmable Logic Array (PLA) – Programmable Array Logic (PAL). Introduction to HDL: Behavioral – data flow, and algorithmic and structural description, lexical elements, data objects types, attributes, operators for Verilog HDL. Examples for Combinational and Sequential circuits.

### PART A

| Q.No | Questions | BT Level | Domain |
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| 1. | Write the difference between ROM and RAM. Also list the types of ROMs. | BTL 1 | Remembering |
| 2. | Distinguish between volatile and non-volatile memory. | BTL 2 | Understanding |
| 3. | Mention the advantages of DRAM cell over SRAM cell. | BTL 4 | Analyzing |
| 4. | What is programmable logic array? Analyze how it differs from ROM? | BTL 4 | Analyzing |
| 5. | A certain memory has a capacity of 32k x 16. How many bits are there in each word? How many words are being stored and how many memory cells does this memory contain? | BTL 2 | Understanding |
| 6. | What is memory decoding? | BTL 1 | Remembering |
| 7. | Show the circuitry used to realize 2-bit multiplier using ROM. | BTL 3 | Applying |
| 8. | Realize the Ex OR function into the PROM. | BTL 3 | Applying |
| 9. | Enumerate the advantages of EEPROM over EPROM. | BTL 4 | Analyzing |
| 10. | How programmable logic devices are classified? | BTL 3 | Applying |
| 11. | Distinguish between PAL and PLA. | BTL 2 | Understanding |
| 12. | List the operators used in Verilog HDL. | BTL 1 | Remembering |
| 13. | What are the primitive gates supported by Verilog HDL? Also specify which gates are tristate gates? | BTL 1 | Remembering |
| 14. | Express the modelling styles used in Verilog HDL along with the way they are realized. | BTL 2 | Understanding |
| 15. | Develop the Verilog HDL code for half subtractor in data flow model. | BTL 4 | Analyzing |
| 16. | Differentiate logical AND and bitwise AND operation in Verilog HDL with example. | BTL 2 | Understanding |
| 17. | Explain how top-down and bottom-up design followed in Verilog HDL. | BTL 3 | Applying |
| 18. | Write the Verilog HDL code for D-Latch. | BTL 1 | Remembering |
| 19. | Mention the conditional and unconditional loops supported in Verilog HDL. | BTL 3 | Applying |
| 20. | Write the Verilog code for T-flip-flop. | BTL 1 | Remembering |
| 21. | What is a Module? | BTL 1 | Remembering |

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| 22. | List any 2 examples for system task in Verilog. | | BTL 2 | Understanding |
| 23. | Differentiate blocking from nonblocking assignments. | | BTL 3 | Applying |
| 24. | What does the operator === is used in Verilog? | | BTL 4 | Analyzing |
| | **PART – B** | | | |
| 1. | Describe the classification of semiconductor memories in detail. | (13) | BTL 1 | Remembering |
| 2. | Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle. | (13) | BTL 2 | Understanding |
| 3. | Explain how Read operation and Write operation is performed in random Access Memory with suitable timing diagram. | (13) | BTL 4 | Analyzing |
| 4. | Derive a combinational circuit defined by the function, F1 = AB'C'+AB'C+ABC and F2 = A'BC+AB'C+ABC using PLA with minimal AND gates. | (13) | BTL 1 | Remembering |
| 5. | List the types of PLDs and explain the architecture of PLAs. | (13) | BTL 1 | Remembering |
| 6. | Write the simplified form of Boolean functions, F1(x, y, z) = ∑ (0, 1, 3, 5); F2(x, y, z) = ∑ (3, 5, 7) and obtain its circuit using 3×4×2 PLA. | (13) | BTL 1 | Remembering |
| 7. | Obtain the circuitry used to realize the following functions using PAL. F1(A, B, C) = ∑ (1, 2, 4, 6); F2(A, B, C) = ∑ (0, 1, 6, 7); F3(A, B, C) = ∑ (1, 2, 3, 5, 7). | (13) | BTL 2 | Understanding |
| 8. | Analyze the design of BCD to Excess 3 code converter using PLA. Illustrate the design detail along with the PLA program table? | (13) | BTL 4 | Analyzing |
| 9. | Write a Verilog code for Carry Look Ahead (CLA) adder. | (13) | BTL 3 | Applying |
| 10. | (i) Tabulate and explain the different category of operators supported in Verilog HDL along with its symbol.<br>(ii) Describe about the modeling styles available in Verilog HDL with suitable example. | (7)<br>(6) | BTL 1 | Remembering |
| 11. | Write Verilog HDL code for full adder using data flow modeling, and behavioral modelling styles with necessary illustration. | (13) | BTL 3 | Applying |
| 12. | Apply data flow modeling style in Verilog HDL to code for 4:1 multiplexer along with detailed explanation. | (13) | BTL 3 | Applying |
| 13. | Design a 3-bit magnitude comparator and write the Verilog HDL code to realize it using structural modelling. | (13) | BTL 3 | Applying |
| 14. | Write the Verilog HDL code for 4-bit synchronous counter. | (13) | BTL 4 | Analyzing |
| 15. | Use any one modeling style to describe a 3 to 8 decoder in Verilog HDL. | (13) | BTL 4 | Analyzing |

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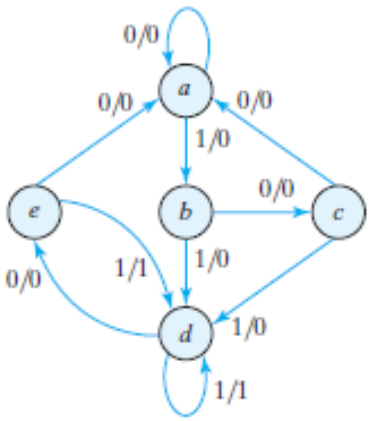
| 16. | Draw the state diagram for Moore state machine with four states, and single input single output. Justify the state diagram chosen. Also write the Verilog HDL code for the state machine and explain. | (13) | BTL 2 | Understanding |
| 17. | Write the Verilog code to construct a 4-bit ripple carry adder from half adders and full adders. | (13) | BTL 4 | Analyzing |
| | **PART C** | | | |
| 1. | Design the following code converters and derive the circuitry used to realize them using PROM device.<br>(i) Binary to gray code<br>(ii) Gray to Binary code | (8)<br>(7) | BTL 3 | Applying |
| 2. | Construct a combinational circuit using ROM that accepts a three-bit binary number and outputs a binary number equal to the square of the input number. | (15) | BTL 4 | Analyzing |
| 3. | Explain the utilization of top down and bottom-up design approach in writing Verilog HDL code for coding 4-bit parallel binary adder design, using full adders and half adders. | (15) | BTL 4 | Analyzing |
| 4. | Evaluate the task carried out by the following state machine and also describe it using Verilog HDL code.<br>  | (15) | BTL 4 | Analyzing |
| 5. | Using 4×3×4 PALS, determine the circuit used to realize the following Boolean functions.<br>(i) W(A,B,C,D) = ∑ (0,2, 6,7,8,9,12,13)<br>(ii) X(A,B,C,D) = ∑ (0, 2, 6, 7, 8, 9, 12, 13, 14)<br>(iii)Y(A, B, C, D) = ∑ ( 2, 3, 8, 9, 10, 12, 13)<br>(iv) Z(A,B,C,D) = ∑ (1, 3, 4, 6, 9, 12, 14) | (15) | BTL 3 | Applying |