SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)
SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

LAB MANUAL

1906304 – ELECTRONIC DEVICES AND CIRCUITS LAB

(Regulation 2019)

II –YEAR / III-SEMESTER ECE

ACADEMIC YEAR: 2022-23 (ODD)

Prepared by,

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SYLLABUS

1906304 ELECTRONIC DEVICES AND CIRCUITS LABORATORY L T P C

0 0 4 2

OBJECTIVES:

The student should be made to:

- To gain hand on experience in basic circuit theorems.
- To learn the characteristics of basic electronic devices such as Diode, BJT, FET, SCR.
- To understand the operation of clipper and clamper & rectifier.
- To analyze the characteristics of an amplifiers.
- Simulate diode characteristics and rectifiers.

LIST OF EXPERIMENTS

1. Verification of Thevenin's & Norton's theorem.
2. Verification of KVL & KCL.
3. Verification of Superposition Theorem.
4. Verification of maximum power transfer & reciprocity theorem.
5. Analyse the Characteristics and application of PN Junction Diode.
6. Analyse the Characteristics of Zener diode & design a Regulator using Zener diode.
7. Common Emitter input-output Characteristics.
8. Common Base input-output Characteristics.
9. Analysis of FET Characteristics.
10. Analysis of SCR Characteristics.
11. Design and test Clipper and Clamper & FWR.
12. Simulation of diode characteristics and Rectifiers using PSPICE.

TOTAL PERIODS:60

OUTCOMES:

On completion of this lab course, the student would be able to,

- Develop the capacity to apply circuit theorems in real time.

- Analyse the characteristics of basic electronic devices such as Diode, BJT, FET, SCR.
- Perform experiment to analyse input-output characteristics of CE and CB amplifiers.
- Test the performance of clipper and clamper & FWR.
- Simulate and analyse diode characteristics and rectifiers using SPICE.

LIST OF EXPERIMENTS
CYCLE I

1. Verification of Thevenin's & Norton's theorem.
2. Verification of KVL & KCL.
3. Verification of Superposition Theorem.
4. Verification of maximum power transfer & reciprocity theorem.
5. Analyse the Characteristics and application of PN Junction Diode.
6. Analyse the Characteristics of Zener diode & design a Regulator using Zener diode.

CYCLE II

7. Common Emitter input-output Characteristics.
8. Common Base input-output Characteristics.
9. Analysis of FET Characteristics.
10. Analysis of SCR Characteristics.
11. Design and test Clipper and Clamper & FWR.
12. Simulation of diode characteristics and Rectifiers using PSPICE.

ADDITIONAL EXPERIMENTS

13. Characteristics of Uni-Junction Transistor
14. Frequency Response Of Series And Parallel Resonance Circuits

Ex.No:1

VERIFICATION OF THEVENIN'S & NORTON'STHEOREM

Preparatory Questions

1. How R_{th} is obtained in any circuit for applying Thevenin's and Norton's theorem?
2. What is V_{th} or Thevenin's voltage?
3. How V_{th} is obtained in any circuit for applying Thevenin's theorem?
4. What is I_N or Norton's current?
5. How I_N is obtained?

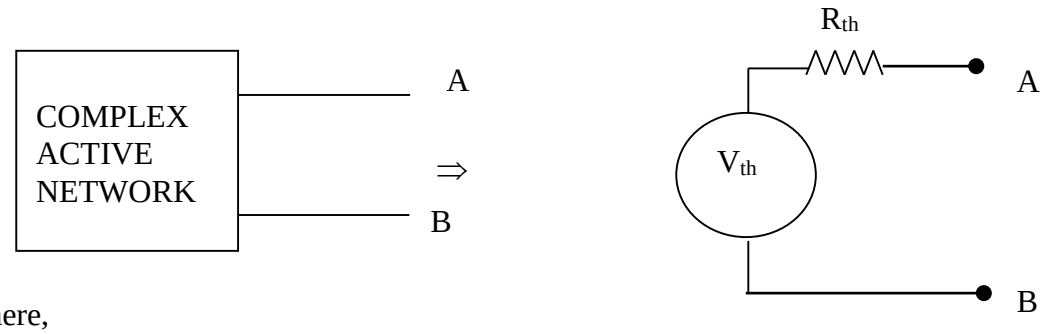
AIM:

a. To verify the Thevenin's theorem for the given electric circuit.
b. To verify the Norton's theorem for the given circuit.

THEVENIN'S THEOREM

STATEMENT:

A one port linear, active, resistive network which contains one or more voltage or current sources can be replaced by a single voltage source V_{th} in series with a single resistance R_{th}.V_{th} is equal to the open circuit voltage across the port terminals of the network & the resistance R_{th} is measured between the port terminals with all the energy sources replaced by their internal resistance.



Where,

R_{th}-Thevenin's resistance, V_{th} -Thevenin's voltage.

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1	RPS (regulated power supply)	(0-30) V	2
2	Ammeter	0-10 mA	1
3	Voltmeter	0 – 25V	2
4	Resistors	1K Ω, 330Ω	Each 2
5	Breadboard		1
6	Connecting wires		Required

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Set a particular value of voltage using RPS and note down the corresponding ammeter readings.

To Find V_{th}:

3. Remove the load resistance and measure the open circuit voltage using multimeter (V_{Th}).

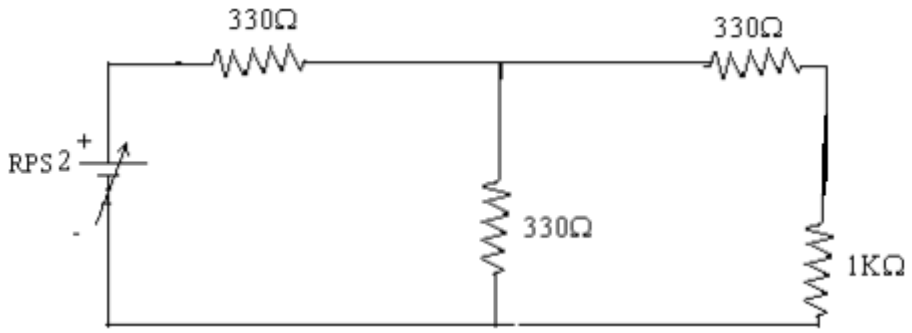
To Find R_{th}:

4. To find the Thevenin's resistance, remove the RPS and short circuit it and find the R_{Th} using multimeter.
5. Give the connections for equivalent circuit and set VTH and RTH and note the corresponding ammeter reading.
6. Verify Thevenins theorem.

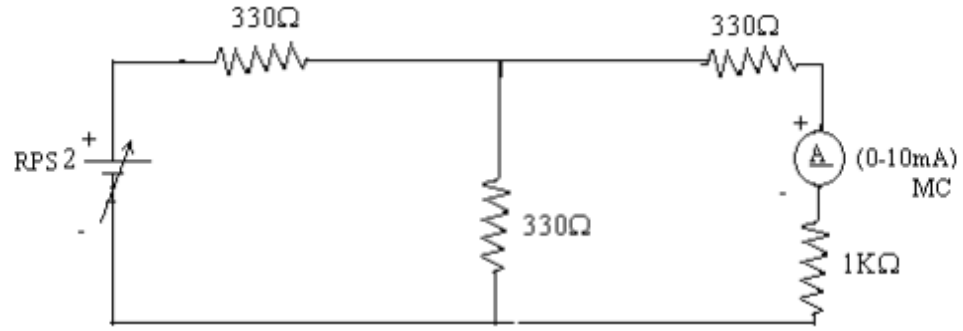
To Find I_L:

7. Vary the RPS to the particular voltage and note down the ammeter reading (I_L).

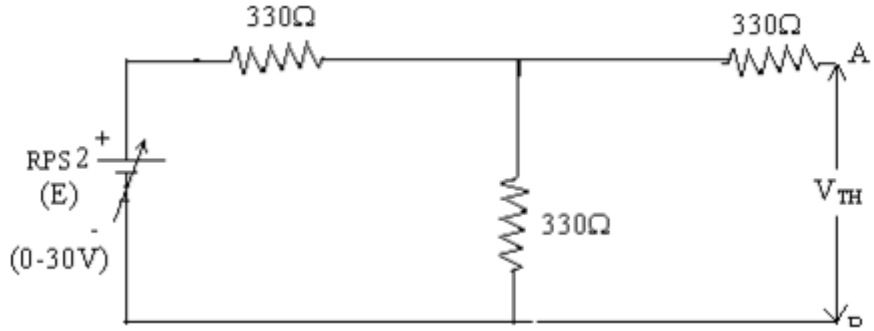
CIRCUIT DIAGRAM: I



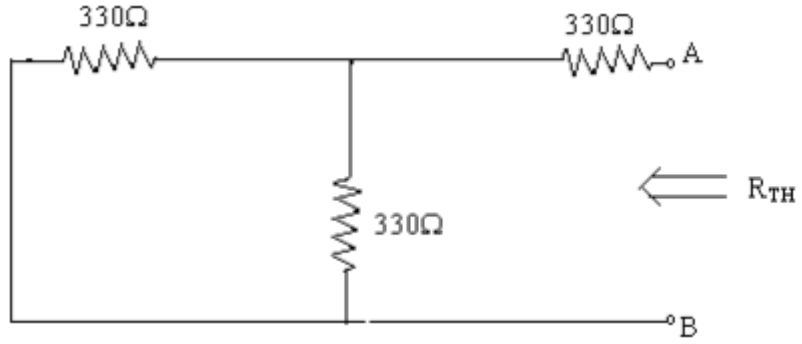
To find load current (I_L)



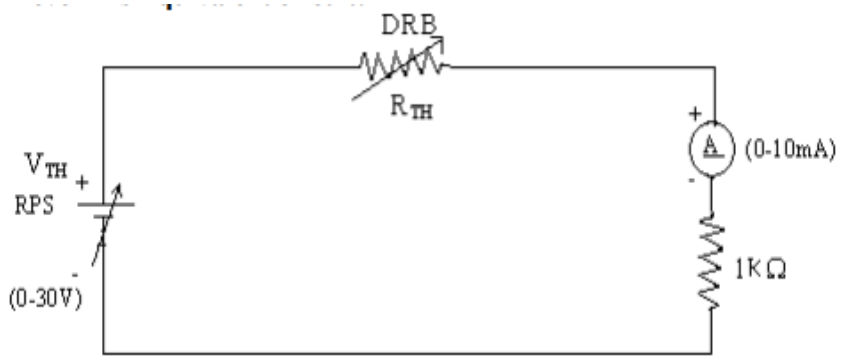
To find V_{th}:



To find R_{th}:



Thevenin's Equivalent circuit:



$$I_L = \frac{V_{th}}{R_{TH} + R_L}$$

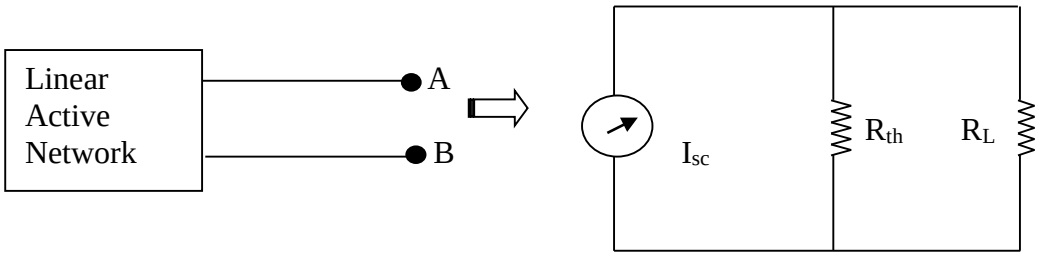
TABULATION:

S.No	Specified voltage E (Volts)	Theoritical			Practical		
		V_{th}	R_{th}	I_L	V_{th}	R_{th}	I_L

B. NORTON'S THEOREM

STATEMENT:

A one port linear, active, resistive network which contains one or more voltage or current sources can be replaced by a single current source I_{SC} in parallel with a single resistance R_{th}. I_{sc} is equal to the short circuit current across the port terminals of the network & the resistance R_{th} is measured between the port terminals with all the energy sources replaced by their internal resistance.



Where,

I_{SC} – Short circuit current at terminals A & B

R_{th}– Thevenin's equivalent Resistance.

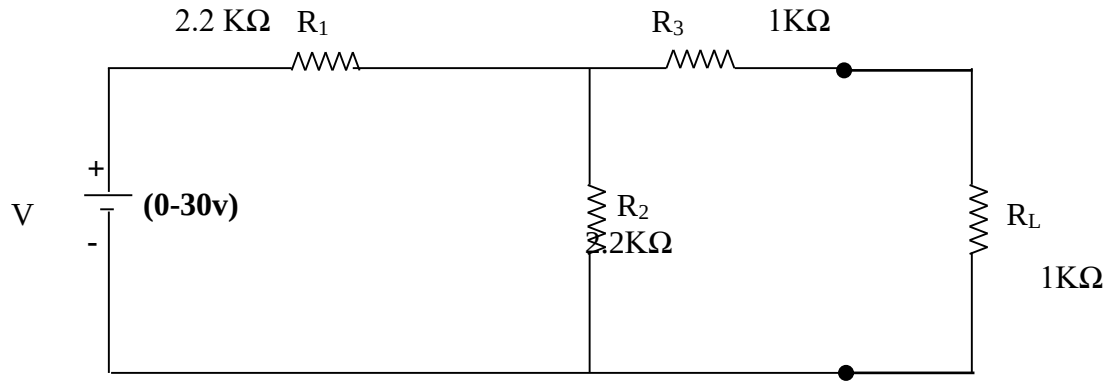
APPARATUS REQUIRED:

S.No	Name	Range	Qty
1	RPS (regulated power supply)	(0-30) V	1
2	Ammeter	0 – 50mA	2
3	Voltmeter	0-25 V	2
4	Resistors	1K Ω, 2.2K Ω,4.7K Ω,6.8K Ω	Each 2
5	Breadboard		1
6	Connecting wires		Required

PROCEDURE:

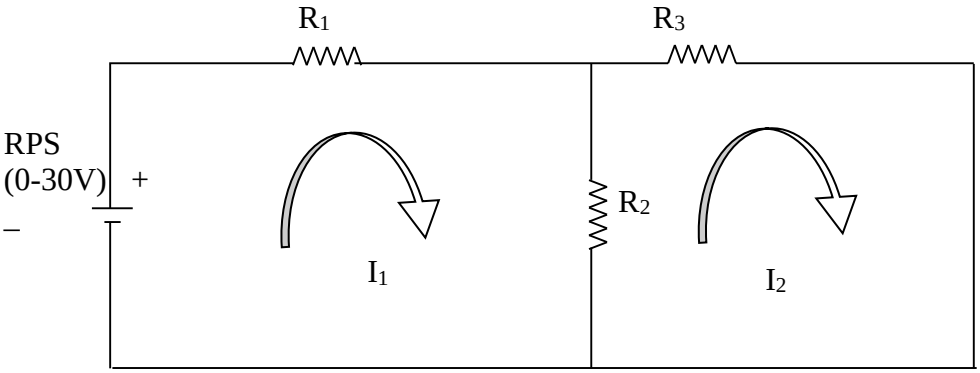
1. **To find I_{SC}(short circuit the load resistance)**
   a) Connections are made as per the circuit diagram.
   b) Note down the ammeter reading (I_{SC})
2. **To find R_{th} (short circuit the voltage source)**
   a) Connections are made as per the circuit diagrams
   b) Supply is switched 'ON'
   c) Vary the RPS to the specified voltage, note down the ammeter and voltmeter readings.
   d) Repeat the step 3 for various R.P.S voltage and the readings are tabulated.
   e) Calculate the R_{Th} using the tabulation.
3. **To Find I_L**
   a) Connections are given as per the circuit diagram.
   b) Switch ON the power supply.
   c) Vary the R.P.S. to the specified voltage and note down the ammeter reading ($I_{L)}$.

CIRCUIT DIAGRAM:



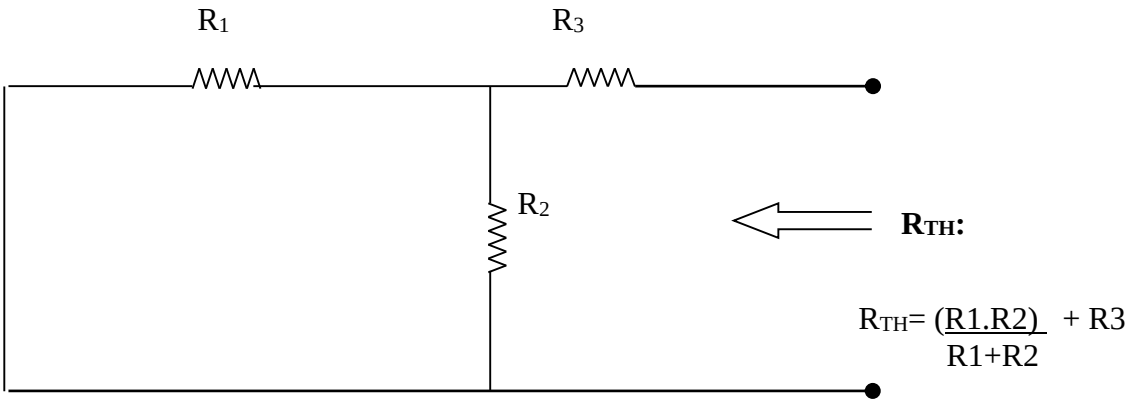
Theoretical Verification:

To Find I_{SC}:

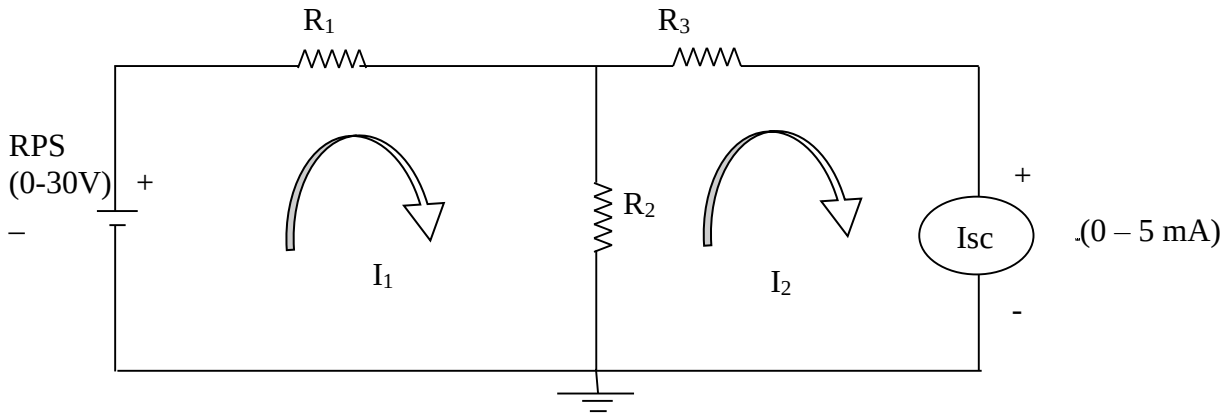


$I_{SC} = I_2 = \Delta_2 / \Delta$

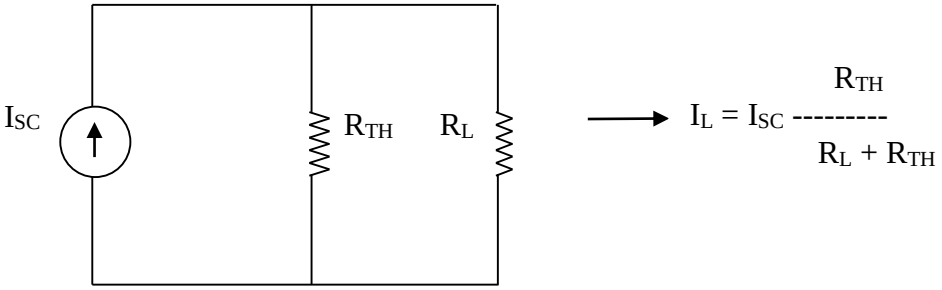
To Find R_{TH}:



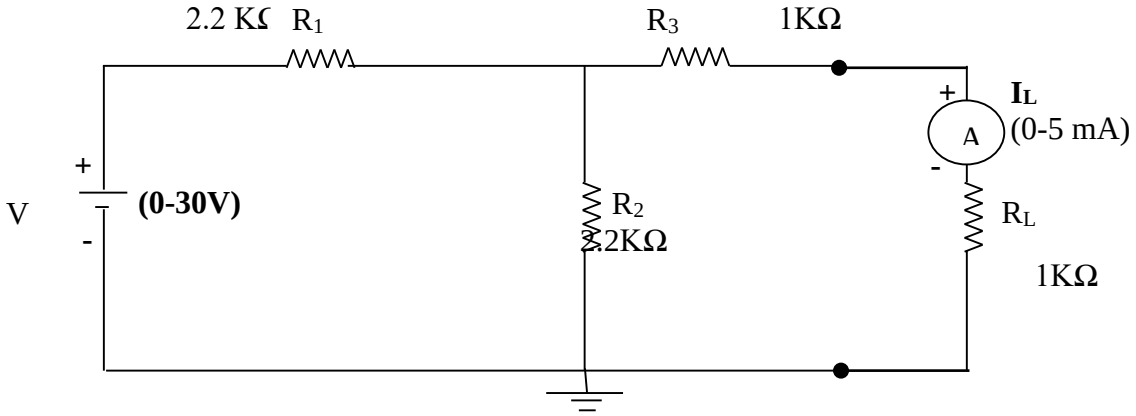
To Find Isc:



To Find I_L:



To Find I_L:

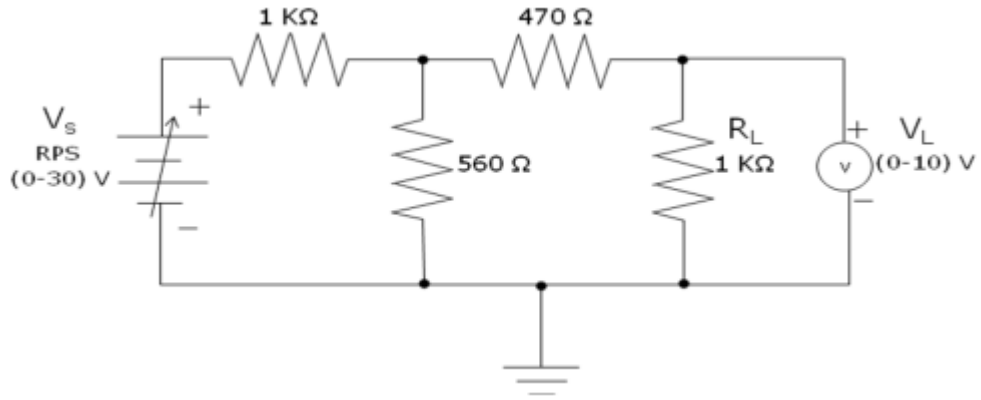


TABULATION:

S.No	Specified voltage (Volts)	Theoritical			Practical		
		Isc	Rth	IL	Isc	Rth	IL

Review Questions:

1. State Thevenin's&Norton's theorem.
2. Draw the Thevenin's& Norton's equivalent circuit for



3. What is duality theorem?
4. Explain dependent sources and sources transformation.
5. Explain Star-Delta conversion

RESULT:

Thus the Thevenin's & Norton's theorems are verified

Ex.No.2

VERIFICATION OF KIRCHOFFS CURRENT LAW AND KIRCHOFF'S VOLTAGE LAW.

Preparatory Questions:

1. State KCL and KVL.
2. What is meant by short circuit and open circuit?
3. Two resistances with the value of R1, R2 are connected in i) series and ii) parallel. What is the equivalent resistance?
4. Two inductors with the value of L1, L2 are connected in i) series and ii) parallel. What is the equivalent inductance?
5. Two capacitors with the value of C1, C2 are connected in i) series and ii) parallel. What is the equivalent capacitance?

AIM:

(a) To verify the Kirchoff's current law.
(b) To verify the Kirchoff'svoltage law.

STATEMENT:

Kirchhoff's Current Law:

The algebraic sum of all the currents at any junction in an electric circuit is zero. In other words, the sum of the current flowing towards a junction is equal to the sum of the currents flowing away from it.

Kirchhoff's Voltage Law:

In any closed circuit, the algebraic sum of all the electromotive forces and the potential drops is equal to zero. In other words, for any closed path in a network, the algebraic sum of voltages is zero.

(i.e) sum of voltage drops = sum of voltage rises.

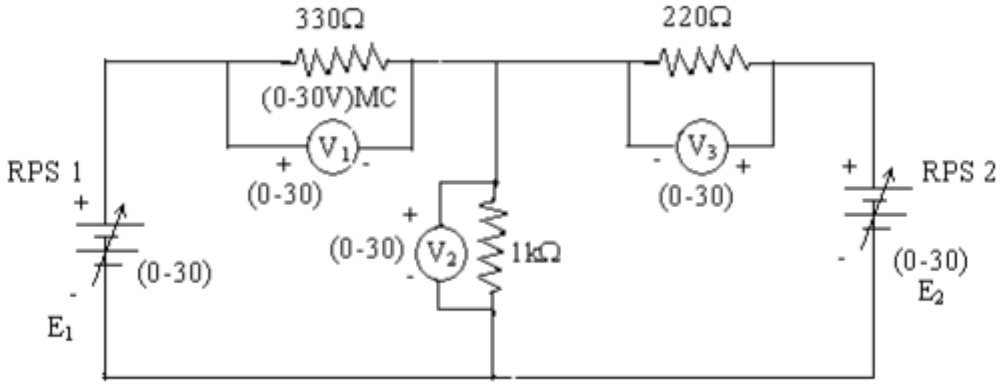
APPARATUS REQUIRED:

S.No	Name	Specification	Qty
1	RPS (Regulated Power Supply)	(0-30)V	1
2	Ammeter	(0–30)mA	3
3	Voltmeter	(0–30)V	3
4	Resistors	330Ω, 220Ω, 1KΩ,	Each 1
5	Bread Board		1
6	Connecting wires		Required

PROCEDURE (Both KCL & KVL)

1. Connections are made as per the circuit diagram.
2. Switch on the power supply.
3. Vary the R.P.S to a specified voltage and note down the corresponding ammeter and voltmeter readings.
4. Repeat the step 3 for various R.P.S voltage and tabulate the readings.
5. Switch off the power supply and remove the connections.

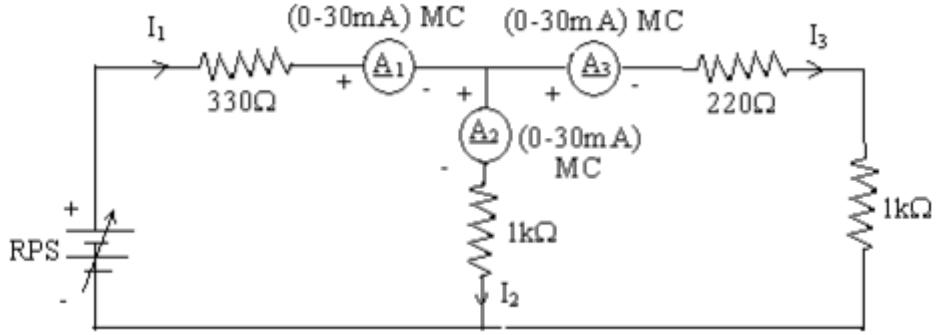
Model circuit of KVL:



TABULATION:

S.No	RPS (V)		Voltage (V)			E_1=V1+V2(Volts)	$E_2=V_2+V_3$(Volts)
	E_1	E_2	V_1	V_2	V_3		

Model Circuit of KCL:



TABULATION:

S.No	Vs(volts)	I_1(A)	I_2(A)	I_3(A)	$I_1=I_2+ I_3$ (A)

Review Questions:

1. Define Resistance, Inductance and capacitance.
2. Explain Colour coding of resistor.
3. Define active and passive elements
4. Define Unilateral and Bilateral elements.
5. Define linear and Non-Linear elements.

RESULT:

Thus the Kirchoff's current law and Kirchoff's voltage law are verified.

Ex.No:3

VERIFICATION OF SUPERPOSITION THEOREM

Preparatory Questions

1. Define Lumped and distributed elements.
2. Define ohm's law.
3. What is the equivalent resistance for the resistor if it is connected in series and parallel?
4. What is the equivalent Capacitance for the capacitor if it is connected in series and Parallel?
5. What is the equivalent Inductance for the Inductor if it is connected in series and Parallel?

AIM:

To verify the superposition theorem for the given electric circuit.

STATEMENT:

In a linear lumped element, bilateral electric circuit energized by two or more sources, the current in any resistor is equal to the algebraic sum of the separate currents in each resistor when each source act, separately.

The Voltage sources are short-circuited and the current sources are open circuited in order to replace the other sources by their respective internal resistances.

APPARATUS REQUIRED:

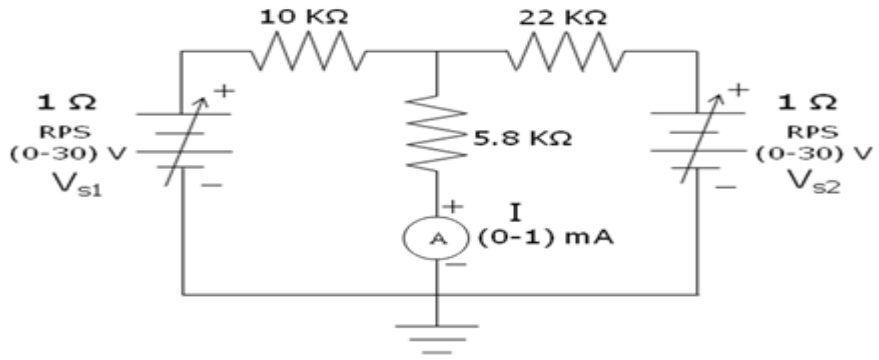
S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30) V	1
2	Ammeter	(0-1) mA	1
3	Resistors	10KΩ, 22KΩ,5.8KΩ	Each 2
4	Connecting wires		Required
5	Breadboard		1

PROCEDURE:

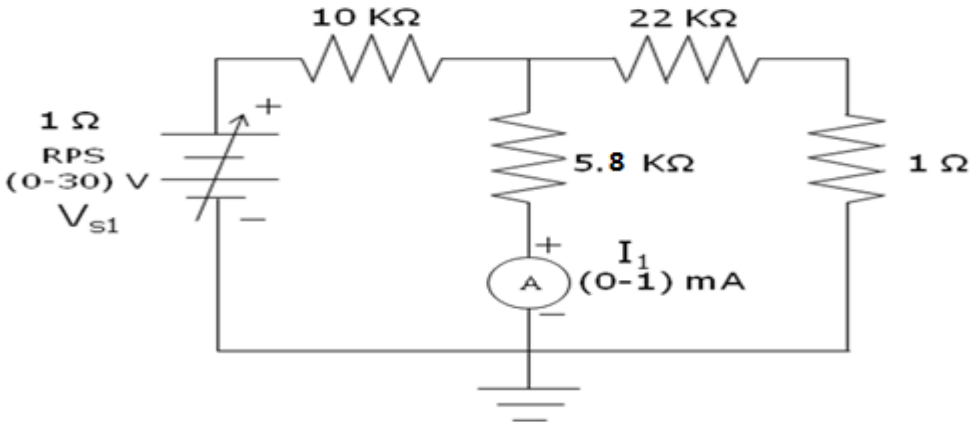
To find I, I_1 & I_2:

1. Connections are given as per the circuit diagram.
2. Switch on the power supply.
3. Set a particular voltage value using V_{S1} and V_{S2} & note down the ammeter reading.
4. Set the same voltage in using V_{S1} alone and short circuit the terminals and note the ammeter reading.
5. Set the same voltage in V_{S2} alone as in circuit I and note down the ammeter reading.
6. Verify superposition theorem.

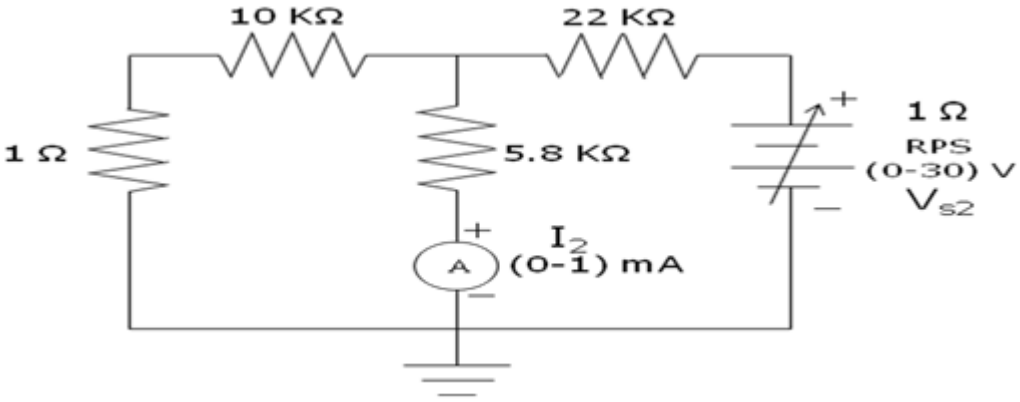
(a) When both V_{S1} & V_{S2} are active



(b) When V_{S1} acts alone



(c) When V_{S2} acts alone



TABULAR COLUMN:

V_{S1} (volts)	V_{S2} (volts)	Theoretical				Practical			
		I (mA)	I_1 (mA)	I_2 (mA)	$I = I_1 + I_2$ (mA)	I (mA)	I_1 (mA)	I_2 (mA)	$I = I_1 + I_2$ (mA)

Review Questions:

1. State superposition theorem.
2. What is duality theorem?
3. Explain dependent sources and sources transformation.
4. Explain Star-Delta conversion
5. State voltage division rule & State current division rule.

RESULT:

Thus the superposition theorem is verified.

Ex.No:4

VERIFICATION OF MAXIMUM POWER TRASNFER AND RECIPROCITY THEOREM

Preparatory Questions

1. Define duality
2. What is transient state?
3. What is transient time?
4. What is natural response?
5. What is transient response?

AIM:

a. To practically verify the maximum power transfer theorem for the network with the theoretical value.
b. To practically verify the reciprocity theorem for the network with the theoretical calculation.

STATEMENT:

Maximum power transfer theorem:

This theorem states that maximum power will be delivered from a voltage source to a load when the load resistance is equal to the internal resistance of the source.

$$\text{Max. Power transferred} = \frac{V^2_{th}}{4\,R_{th}}$$

APPARATUS REQUIRED:

S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30) V	1
2	DRB	(0-10)KΩ	1
3	Voltmeter	0 –5V	1
4	Connecting wires		Required
5	Resistors	1KΩ, 2.2KΩ	Each 1
6	Breadboard		1

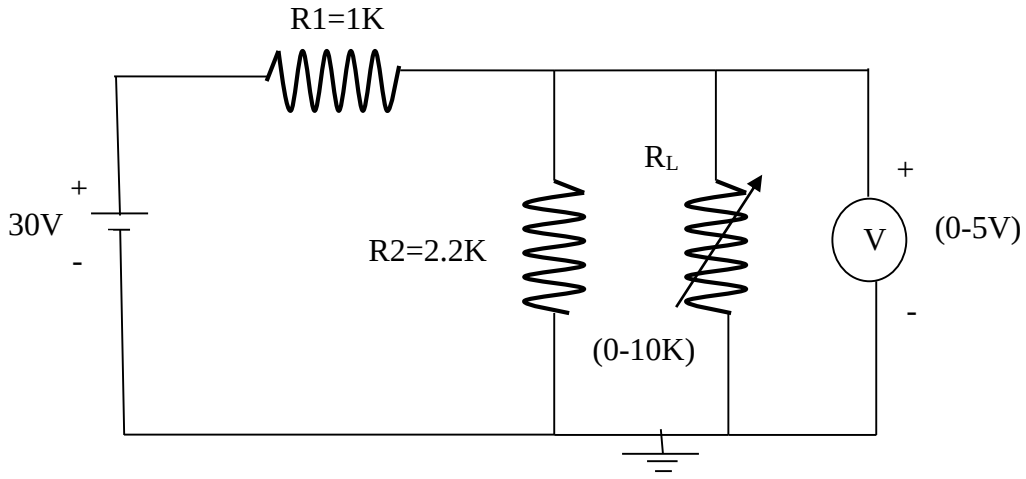
a. MAXIMUM POWER TRANSFER THEOREM:

PROCEDURE:

1. Remove the portion of network through which power has to be transferred.
2. Name those terminals as A and B.
3. Calculate R_{th} by substituting all sources with internal resistance working back at network

4. Give the connections as per the circuit diagram.
5. By varying the DRB (R_L) for values of R_L, measure the current through R_L.
6. Calculate the power delivered to R_L.
7. Verify resistance (R_L) at $P_{L(max)}$ is equal to Rth.

CIRCUIT DIAGRAM:

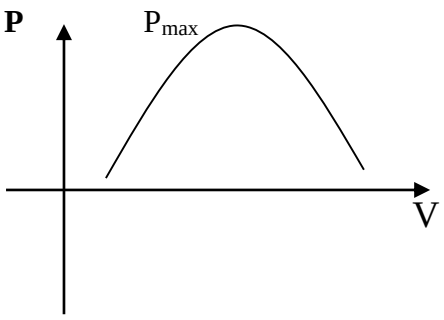


TABULATION

Experimental values:

$R_L\Omega$	**V_{th}(v)**	**$P=V_{th}^2/4R_L$ (w)**

MODEL GRAPH:



RECIPROCITY THEOREM:

In any linear bilateral network the ratio of voltage to current response, in any element to the input is constant even when the position of the input and output are interchanged.

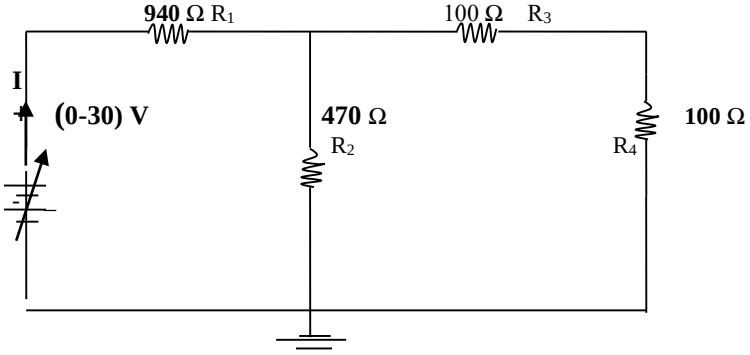
APPARATUS REQUIRED:

S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30) V	1
2	Ammeter	0 – 50 mA	1
3	Voltmeter	0 – 25V	1
4	Connecting wires		Required
5	Resistors	470Ω,100Ω,940Ω	Each 2
6	Breadboard		1

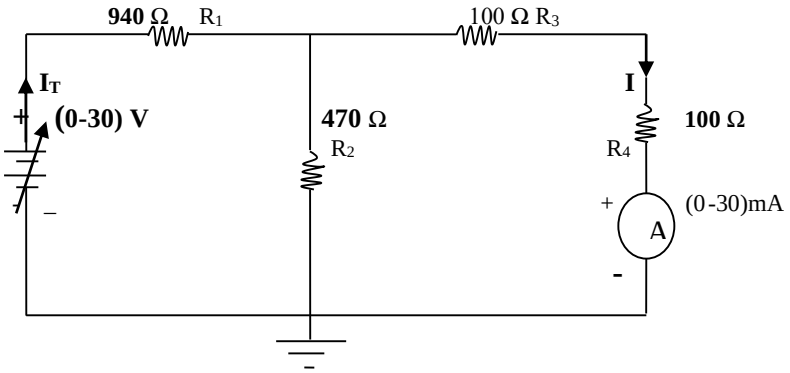
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Note down the ammeter reading and find the ratio of the output current and input voltage.
3. Interchange the position of ammeter and the voltage source.
4. Note down the ammeter reading and find the ratio of the output and input voltage.
5. Compare this value with the value obtained in step 2.

CIRCUIT DIAGRAM:



Circuit 1: To Measure the Load Current



$$R_{eq} = \frac{(R_3+R_4)* R_2}{(R_3+R_4) + R_2} + R_1$$

$$I_T = V/ R_{eq}$$

$$I = \frac{I_T * R_2}{((R_3+R_4) + R_2)}$$

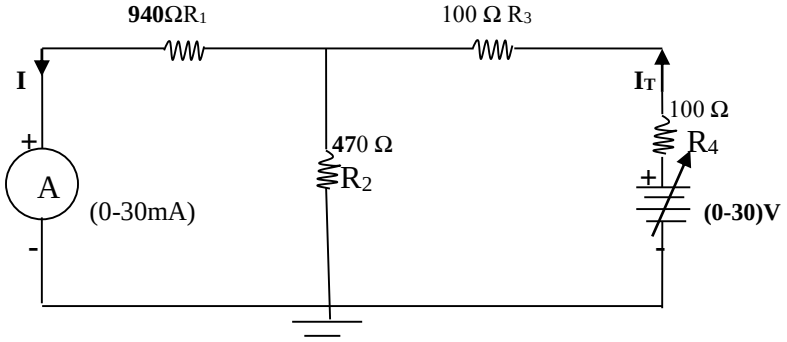
TABULATION

Experimental values: Theoretical values:

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

Circuit 2: After Interchanging Positions of V and I



$$R_{eq} = \frac{R_1* R_2}{R_1+R_2} + R_3+R_4$$

$$I_T = V/ R_{eq}$$

$$I = \frac{I_T * R_2}{R_1+R_2}$$

TABULATION

Experimental values: Theoretical Values

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

V (Volts)	I (mA)	Z = V/I
0		
2		
4		
6		

Review Questions:

1. State Maximum Power transfer theorem.
2. State reciprocity theorem?
3. What is duality theorem?
4. Explain dependent sources and sources transformation.
5. Explain Star-Delta conversion

RESULT:

Hence the maximum power transfer and reciprocity theorem for the given networks are practically verified.

Ex.No.5

CHARACTERISTICS OF PN JUNCTION DIODE

Preparatory Questions

1. What is a semiconductor?
2. Write the Diode current Equation.
3. What is the value of V_t at room temperature
4. What is meant by forward bias
5. What is meant by reverse bias?

AIM:

To determine the VI characteristics of PN Diode.

APPARATUS REQUIRED:

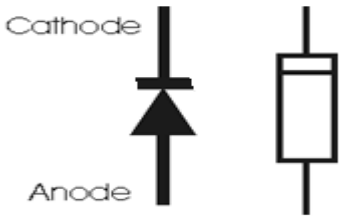
S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30)V	1
2	Ammeter	(0-5)mA, (0-25)mA	1 1
3	Voltmeter	(0-10)V (0-1)V	1 1
4	Connecting wires	-	Required
5	Bread Board		1
6	Resistors	1KΩ	1
7	Diode- PN	BY127	1

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

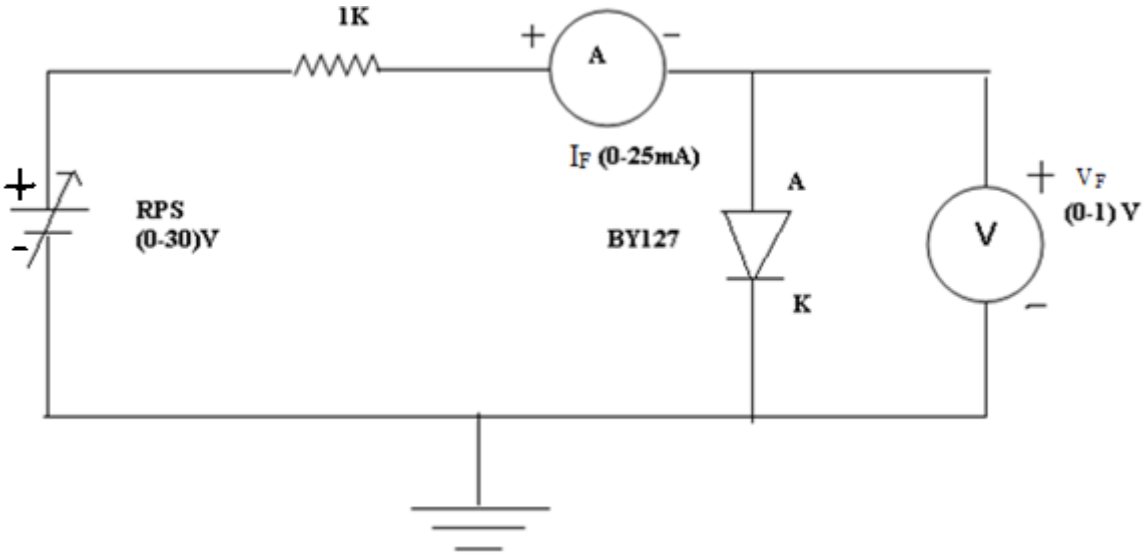
When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannot cross the junction and the diode does not conduct. But there will be a leakage current due to minority carrier. When diode is forward biased, resistance offered is zero, and when reverse biased resistance offered is infinity. It acts as a perfect switch.

PIN DIAGRAM:

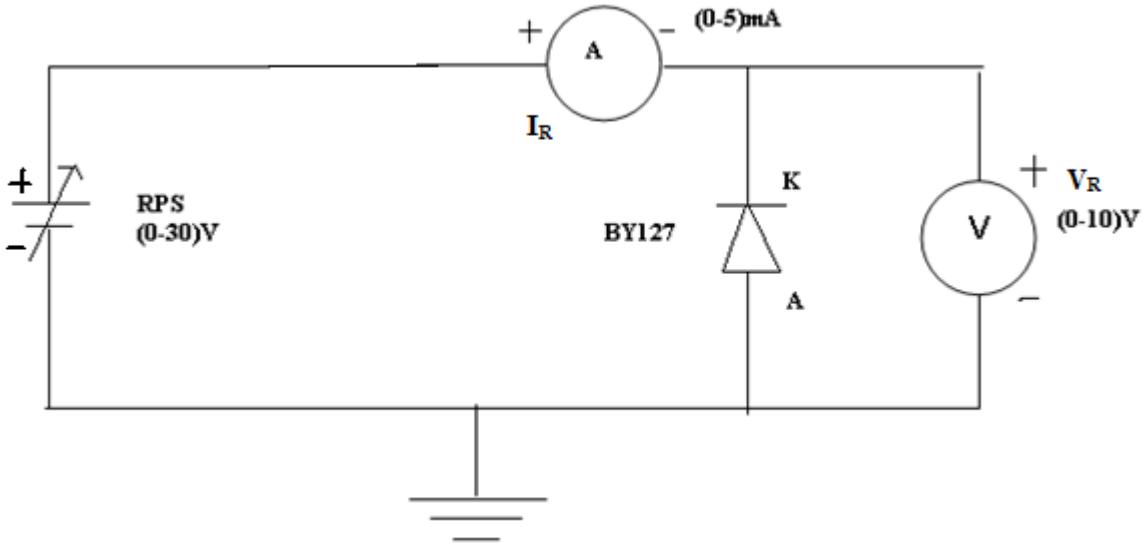


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between $V_f$and I_f.

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

TABULATION:

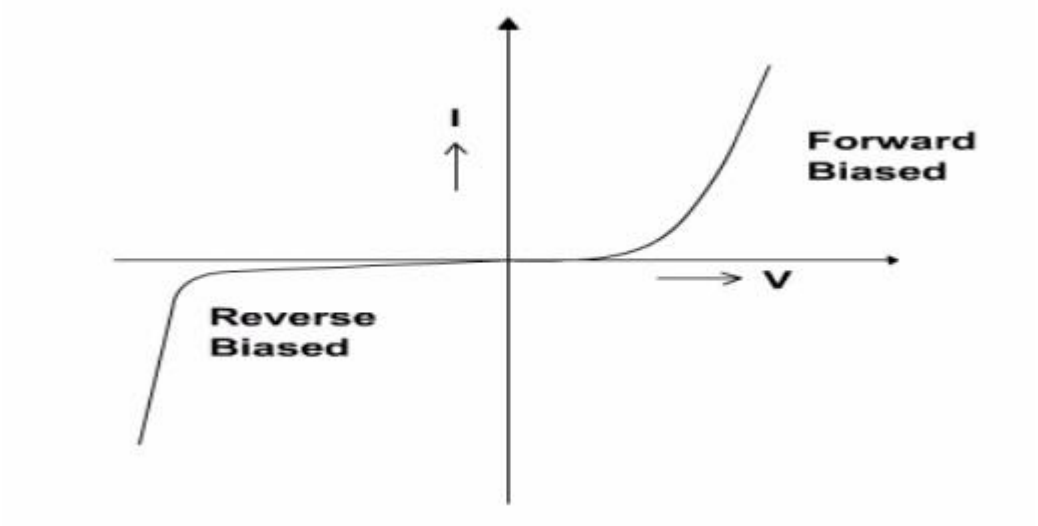
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



Review Questions:

1. How a PN junction is formed?
2. In what way the width of depletion region can be varied?
3. What is potential barrier?
4. In forward bias condition the current condition is due to_____
5. What is reverse saturation current Ico?

RESULT:

Thus the characteristics of PN-Junction diode were drawn**.**

Ex.No.6a

CHARACTERISTICS OF ZENER DIODE

Preparatory Questions

1. How the name of the Zener came?
2. What is cause of reverse breakdown?
3. What is zener voltage?
4. Write the Symbol for the Zener diode.
5. What are the different types of breakdowns in semiconductor junctions?

AIM:

To determine the VI characteristics of Zener Diode

APPARATUS REQUIRED:

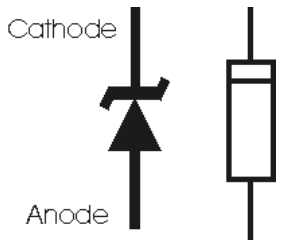
S.No	Name	Range	Type	Qty
1	RPS	(0-30)V		1
2	Ammeter	(0-30) mA		1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires	-		As Required
5	Bread Board			1
6	Resistors	1KΩ		1
7	Diode- Zener	FZ 5V6/ FZ 6V2		1

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

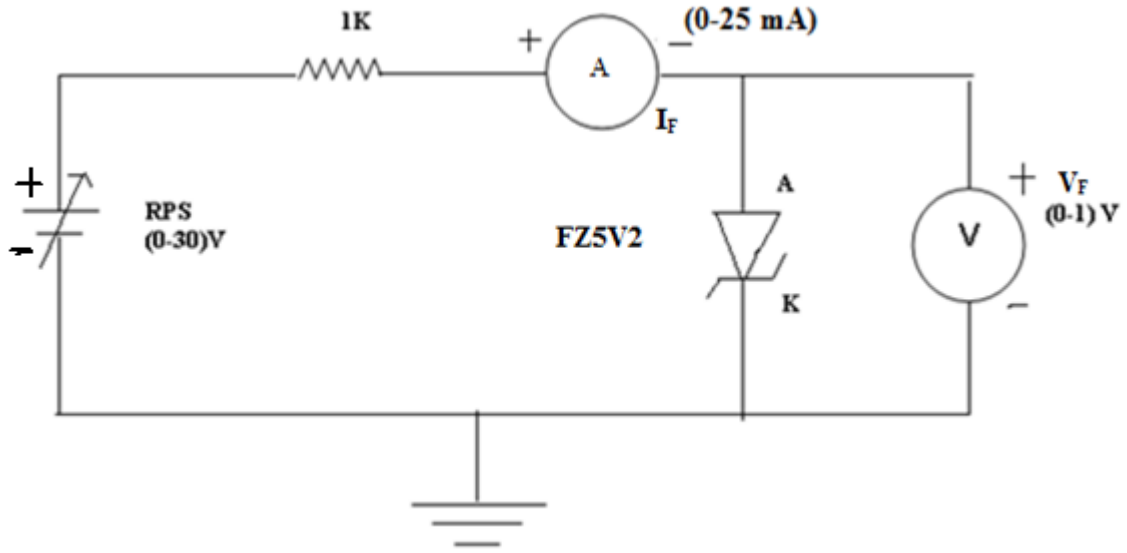
In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:

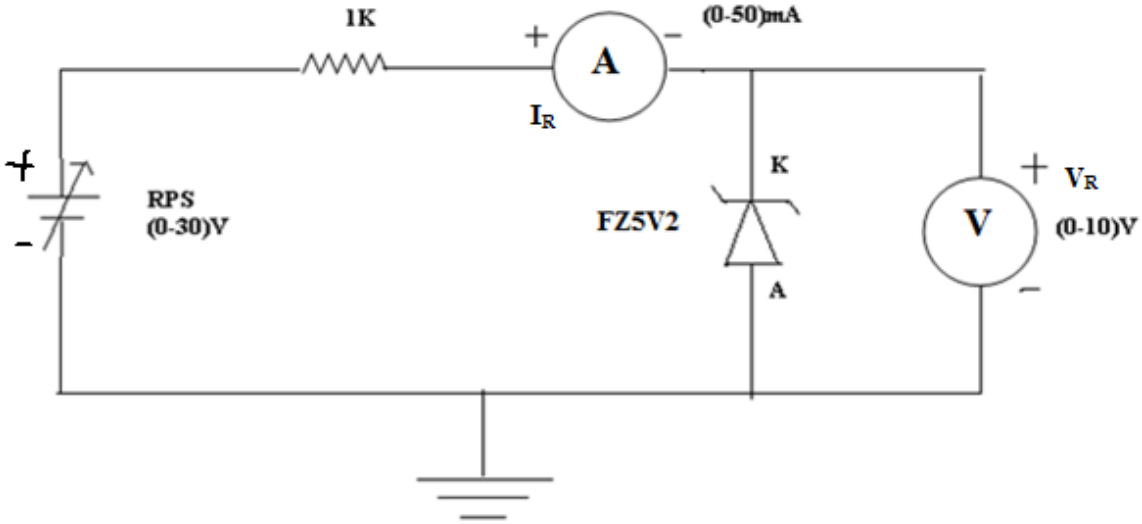


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

TABULAR COLUMN:

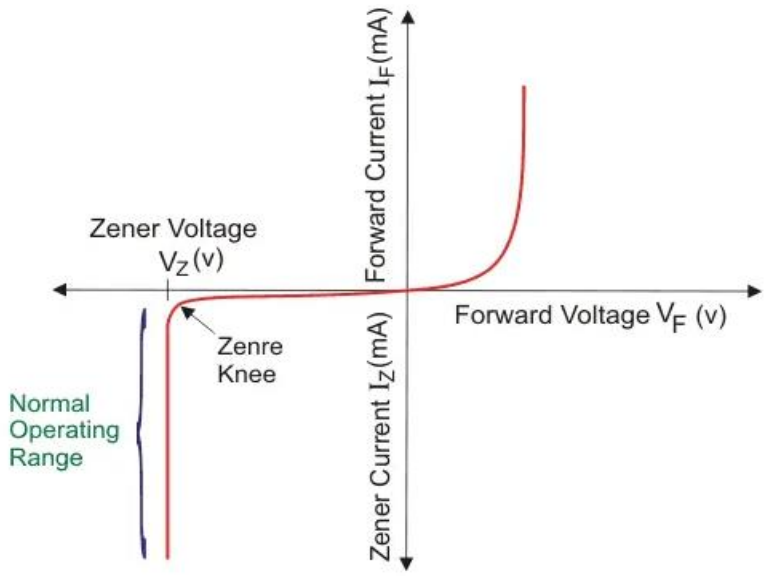
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



Review Questions:

1. What is the difference between p-n Junction diode and zener diode?
2. Can we use Zener diode as a switch?
3. Explain working of a Zener Diode.
4. What is the max value of voltage of Zener breakdown devices?
5. What is cause of reverse breakdown?

RESULT:

Thus the characteristics of Zener diode were drawn**.**

Ex.No.6 b

DESIGN OF VOLTAGE REGULATOR USING ZENER DIODE

Preparatory Questions

1. How Zener diode acts as a voltage regulator?
2. Explain working of a Zener Diode.
3. Explain Zener Breakdown.
4. Explain avalanche breakdown.
5. Compare Zener and avalanche Breakdown.

AIM:

To study the Zener Diode as Voltage Regulator.

APPARATUS REQUIRED:

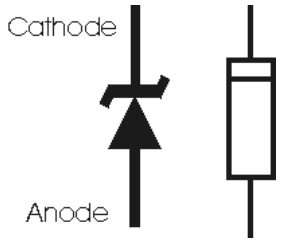
S.No	Name	Range	Qty
1	RPS (Regulated power supply)	(0-30)V	1
2	Ammeter	(0-30) mA	1
3	Voltmeter	(0-10)V (0-1)V	1 1
4	Connecting wires		As Required
5	Bread Board		1
6	Resistors	1KΩ	1
7	Diode- Zener	FZ 5V6/ FZ 6V2	1

THEORY:

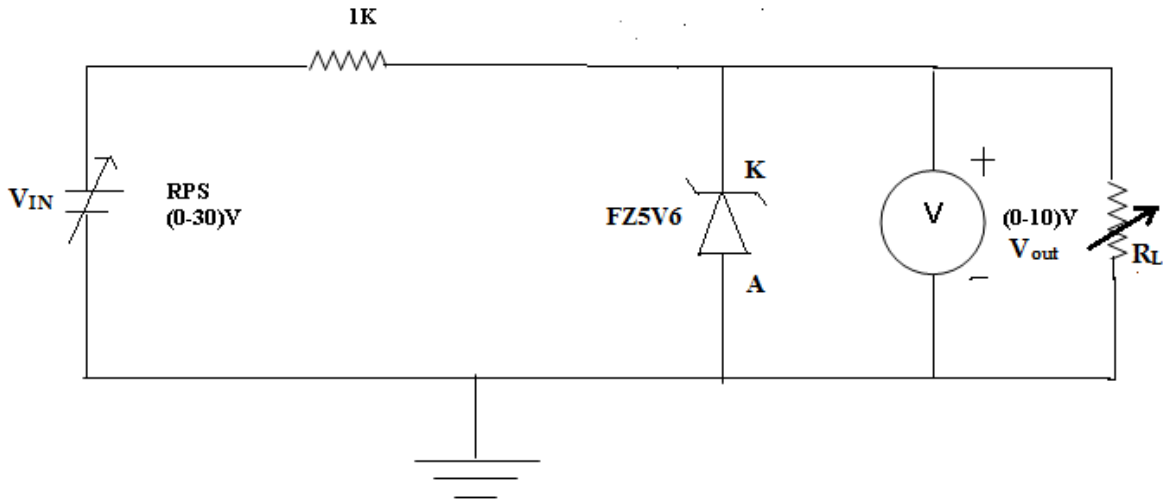
Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased,they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



PROCEDURE:

1. The connections are made as per the circuit diagram.
2. Keep Load resistance R_L constant.
3. Vary the Input voltage and note down the corresponding output voltage.
4. Now keep voltage constant vary the $R_L$and note down the voltmeter corresponding reading.
5. Plot the respective regulations graph.

TABULAR COLUMN:

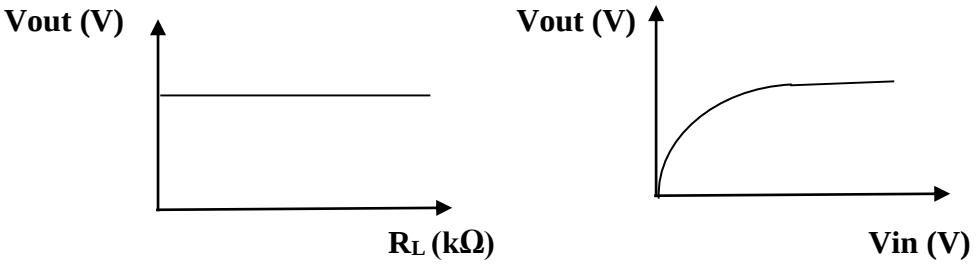
LOAD REGULATION:

R_L (kΩ)	Vout (V)

LINE **REGULATION:**

Vin (V)	Vout (V)

MODEL GRAPH



LOAD REGULATION **LINE REGULATION**

Review Questions:

1. What are the applications of Zener diode?
2. What is voltage regulator?
3. What is cut-in-voltage?
4. What is break down voltage?
5. Draw characteristics of Zener Diode under Forward & Reverse Bias Conditions

RESULT:

Thus the Zener diode as a Voltage Regulator were studied**.**

Ex.No:7

CHARACTERISTICS OF CE CONFIGURATION

Preparatory Questions

1. Explain the operation of CE configuration
2. Determine the output resistance and input resistance
3. What is the relation between α, β and γ?
4. Define current gain in CE configuration?
5. Why CE configuration is preferred for amplification

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CE configuration.

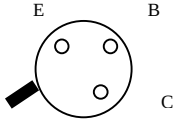
APPARATUS REQUIRED:

S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	10KΩ,100Ω	2
3	RPS (Regulated power supply)	(0-30) V	1
4	Voltmeters	(0-10) V (0-1) V	1 1
5	Ammeters	(0-30) mA (0-100)μA	1 1
6	Bread board		1
7	Connecting wires		Required

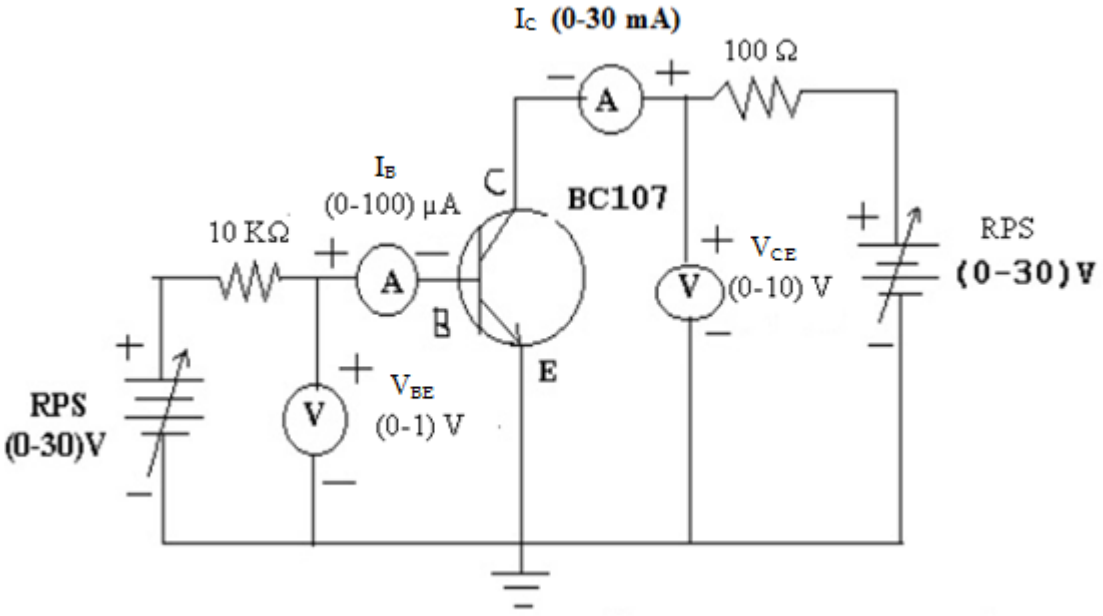
THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CE configuration, Emitter is common to both the Emitter and Base.

PIN DIAGRAM OF BC107



CIRCUIT DIAGRAM:



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction $V_{BE\ vs}$ I_B, where V_{CE} is constant

Output Characteristics:

Voltage across Collector Emitter junction V_{CE} vs I_C where I_B is constant.

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CE} is kept constant (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_B values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between $V_{BE\ vs}$ I_B, where V_{CE} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_B is kept constant, V_{CE} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{CE} and Ic for a constant I_B.

TABULATION:

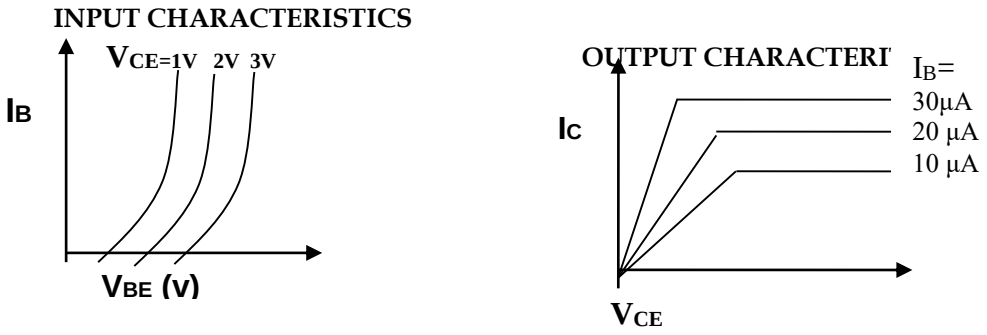
Input Characteristics:

V_{CE} = V		V_{CE} = V	
V_{BE}(V)	I_B (µA)	V_{BE}(V)	I_B(µA)

Output characteristics:

I_B = µA		I_B = µA	
V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C(mA)

MODEL GRAPH:



Review Questions:

1. List the current components of BJT in CE configuration
2. What is Early Effect?
3. Why the doping of collector is less compared to emitter?
4. What do you mean by “reverse active”?
5. What is the difference between CE and Emitter follower circuit?

RESULT:

Thus the input and output characteristic of BJT in Common Emitter mode is drawn.

Ex.No:8

CHARACTERISTICS OF CB CONFIGURATION

Preparatory Questions

1. Explain the operation of CB configuration
2. Determine the output resistance
3. Determine input resistance
4. Explain input characteristics
5. Explain output characteristics

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CB configuration.

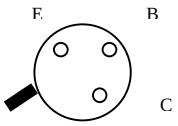
APPARATUS REQUIRED:

S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	470Ω	2
3	RPS (Regulated power supply)	(0-30) V	1
4	Voltmeters	(0-10) V (0-1) V	1 1
5	Ammeters	(0-30) m A	2
6	Bread board	-	1
7	Connecting wires		Required

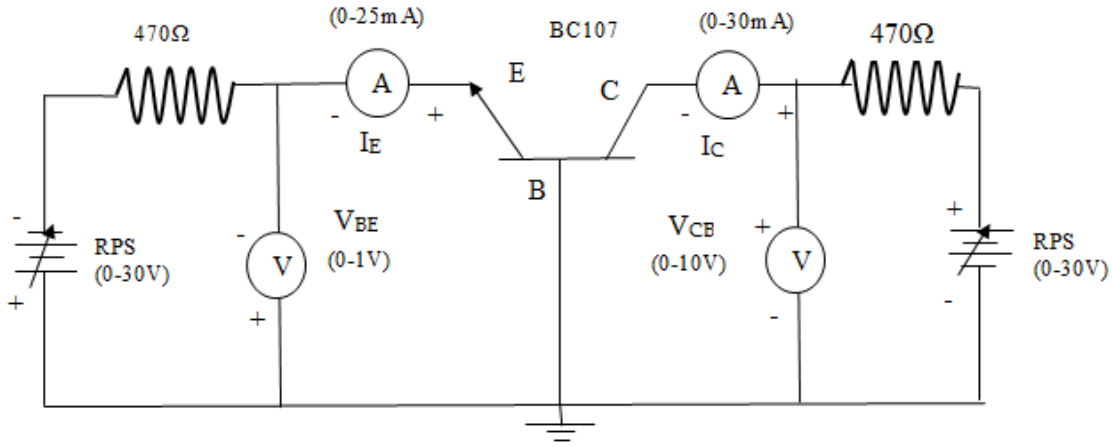
THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CB configuration, base is common to both the emitter and collector.

PIN DIAGRAM OF BC107



CIRCUIT DIAGRAM:



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_E, where V_{CB} is constant

Output characteristics:

Voltage across Collector Emitter junction V_{BC} vs I_C where I_E is constant

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CB} is kept constant (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_E values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_E, where V_{CB} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_E is kept constant, V_{BC} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{BC} and Ic for a constant I_E.

TABULATION:

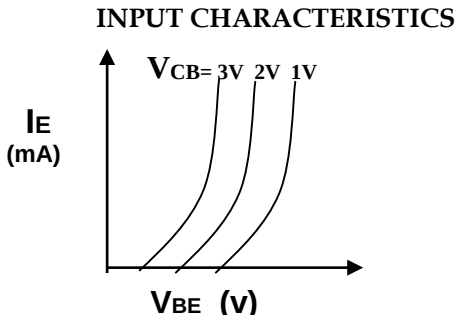
Input Characteristics:

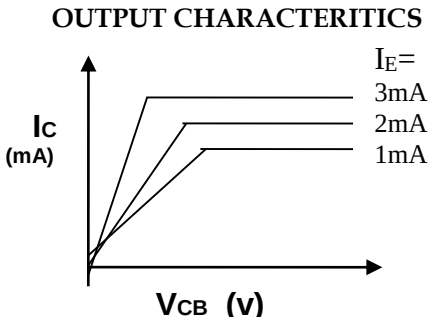
V_{CB} = V		V_{CB} = V	
V_{BE} (V)	I_E (mA)	V_{BE} (V)	I_E (mA)

Output Characteristics:

I_E= mA		IE= mA	
V_{BE} (V)	I_C (mA)	V_{BE} (V)	I_C (mA)

MODEL GRAPH:





Review Questions:

1. Bring out the comparison of CC and CB transistor parameters
2. Give the relation of Ebers moll equation.
3. Bring out the comparison of CE and CB transistor parameters
4. Draw input and output characteristics of CB?
5. Explain Gummen poll model

RESULT:

Thus the input and output characteristic of BJT in Common Base mode is drawn.

EX .NO-9

CHARACTERISTICS OF FET.

Preparatory Questions

1. Why it is called by name "field effect transistor"?
2. What are the advantage of FET OVER BJT?
3. What are the disadvantages of FET?
4. What is the significance of arrowhead in FET symbol?
5. Why FET is called unipolar device

AIM:

To plot the drain and transfer characteristics of JFET & to find drain resistance, transconductance, amplification factor, drain saturation current I_{DSS} and Pinch off voltage.

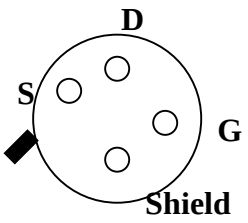
APPARATUS REQUIRED:

S.No.	Components	Specification	Qty
1	FET	BFW10 I_{dss}> 8 mA, Vp<8V	1
2	Resistors	1KΩ	1
3	RPS (Regulated dual power supply)	(0-30)V	1
4	Voltmeters	(0-10)V, (0-25)V	1
5	Ammeters	(0-25) mA	1
6	Bread board		1
7	Connecting wires		Required

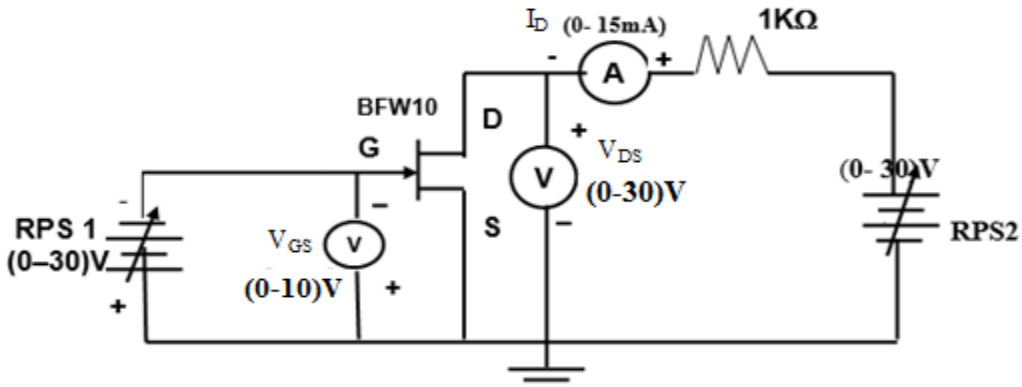
THEORY:

Field effect transistor is a semiconductor device that depends for its operation on the control of current by an electric field. Its operation depends on the flow of majority carriers only. It is therefore a unipolar device. It exhibits a high input resistance. An N- channel JFET consists of a N-type bar is sandwiched between two heavily doped Persians. Due to the concentration gradient, the depletion region formed. On both sides of the semiconductor bar the ohmic contacts are made. One terminal is called source & other is called drain. Both the p-type regions are connected together.

PIN DIAGRAM OF BFW10



CIRCUIT DIAGRAM



DESCRIPTION:

DRAIN CHARACTERISTICS +

INPUT: Drain voltage V_{DS} is varied insteps of 1V, V_{GS} is kept constant

OUTPUT: Drain current I_D

TRANSFER CHARACTERISTICS

INPUT: Gate – source voltage V_{GS} is varied, Drain –source voltage V_{DS} is kept constant

OUTPUT**:** Drain current I_D

PROCEDURE:

Drain Characteristics:

1. Connections are made as per the circuit diagram.
2. Gate –source voltage V_{GS} is kept constant (say –1v), drain voltage V_{DS} is varied insteps of 1v and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{GS}= -2v, 0v.
4. The graph is plotted V_{DS} and I_D for a constant V_{GS}.
5. The drain resistance is found from the graph

$$r_d = \Delta V_{DS} / \Delta I_D$$

Transfer Characteristics:

1. Connections are made as per the circuit diagram.

2. Drain –source voltage V_{DS} is kept constant (say 5v), the gate – source voltage V_{GS} is varied insteps of 1v (-VE voltage) and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{DS} = 10v, 15v,
4. Graph is plotted between V_{GS} and I_D for a constant V_{DS}.
5. The trans conductance is found from the graph

$$g_m = \Delta I_D/\Delta V_G$$

TABULAR COLUMN:

Drain characteristics

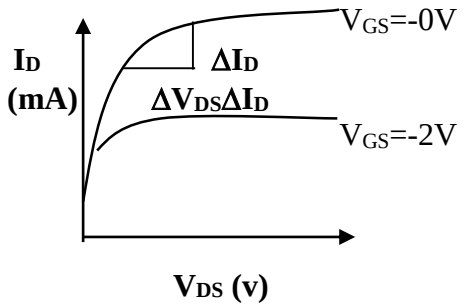
V_{GS} = V		V_{GS} = V	
V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)

Transfer characteristics

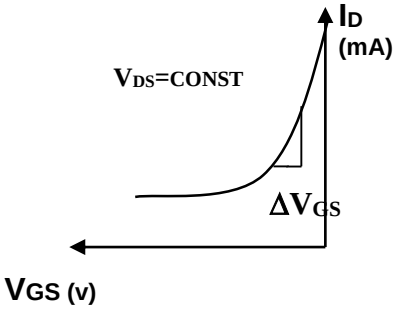
V_{DS} = V		V_{DS} = V	
V_{GS} (V)	I_D (mA)	V_{GS} (V)	I_D (mA)

MODEL GRAPH:

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



CALCULATION

Transconductance $g_m = \Delta I_D/\Delta V_G$

Drain resistance $r_d = \Delta V_{DS}/\Delta I_D$

Amplification factor $\mu = g_m r_d$

Review Questions:

1. Define VVR.
2. Why MOSFET is preferred than FET?
3. What are the differences between FET & MOSFET?
4. What are the applications of FET?
5. Why FET is called us voltage controlled device?

RESULT:

Thus the drain and transfer for characteristics of JFET is drawn.

Drain resistance r_d =

Trans conductance g_m =

Amplification factor =

EX NO: 10

CHARACTERISTICS OF SCR

Preparatory Questions

1. What is an SCR?
2. What are the methods to trigger ON SCR?
3. What is meant by break over voltage of SCR?
4. What is meant by holding current and latching current in SCR?
5. SCR a unidirectional or bidirectional device.

AIM:

To construct a circuit using SCR to draw its Firing Characteristics.

APPARATUS REQUIRED:

S.No	Components	Specification	Quantity
1	SCR	(TYN616)	1
2	Dual RPS	(0-30)V	2
3	Resistor	10KΩ, 1KΩ	1 each
4	Ammeter	(0-200)mA	2
5	Voltmeter	(0-20)V	1
6	Bread board		1

THEORY:

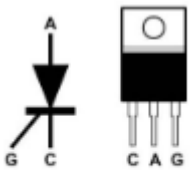
The SCR consists of four layers of semiconductor material alternatively P type and N type. It can be brought of as an ordinary rectifier with a control element .The control element is called GATE. The gate current determines the anode to cathode voltage at which the device starts to conduct.

It means that gate terminal of the SCR is controlled by the applied voltage. Once switched ON the gate has no further control. To switch the SCR the anode current has to be reduced below a certain level called HOLDING CURRENT.

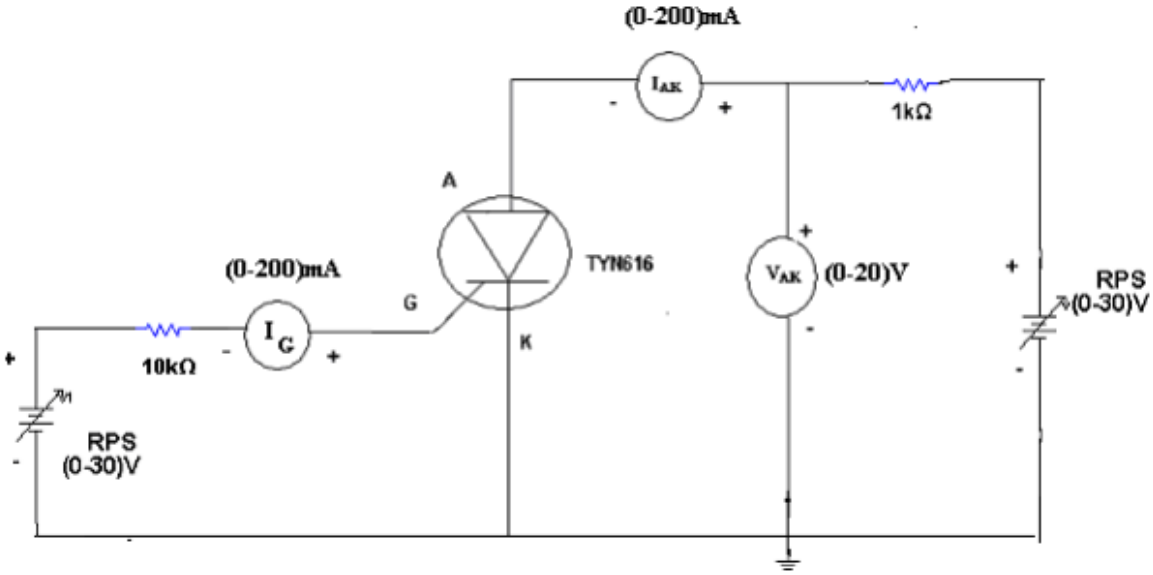
The SCR can be triggered ON with the gate or amplitude triggering, pulse triggering methods. The terms ON & OFF are used to represent the conduction and blocking mode of SCR respectively open circuited with the anode to cathode voltage made large enough .In conduction state the SCR behaves as an ordinary diode.

The anode to cathode voltage at which the SCR conducts is called BREAK OVER VOLTAGE or FORWARD BLOCKING VOLTAGE. It has great switching speed than other devices.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



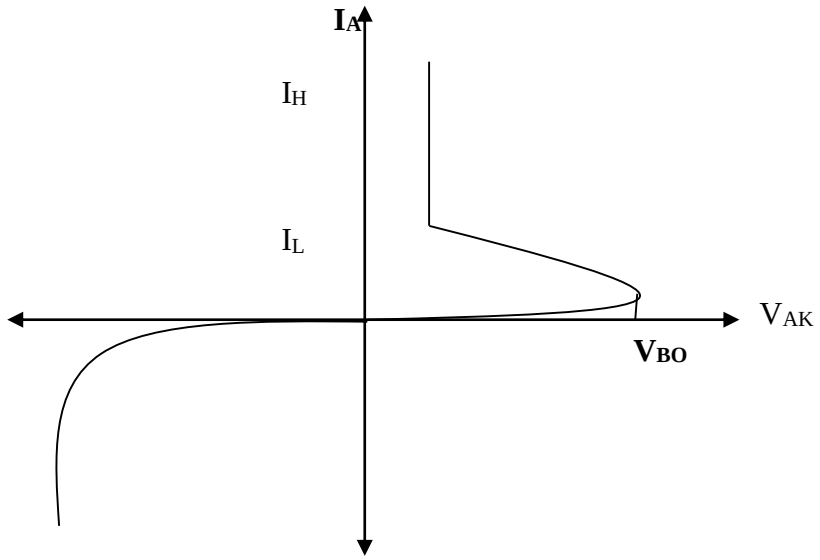
PROCEDURE:

1. All the connections are made as per the circuit diagram.
2. Keep the gate current (I_G) open i.e. $I_G = 0$ mA.
3. Vary the anode to cathode supply voltage and note down the readings of Voltage V_{AK} (V), and Current I_{AK} (µA).
4. Now Keep the gate current (I_G) at a standard value of 10 mA i.e. $I_G = 10$ mA.
5. Again vary the anode to cathode supply voltage and note down the corresponding readings of Voltage V_{AK} (V), and Current I_{AK} (mA).
6. Plot the graph by taking V_{AK} (V) on x-axis and Current I_{AK} (mA) on y-axis.
7. Measure the Break-over voltage (V_{BO}) and Holding current (I_H) of SCR from the graph.

TABULAR COLUMN:

S.No.	I_G=0mA		I_G = 10 mA	
	V_{AK} (V)	I_{AK} (µA)	V_{AK} (V)	I_{AK} (µA)

MODEL GRAPH:



Review Questions:

1. What is meant by Valley Point and Peak Point?
2. After triggering an SCR, the gate pulse is removed. What is the state (ON or OFF) of the device at this condition? Justify our answer
3. Why is Peak Reverse Voltage Important?
4. What is asymmetrical SCR?
5. What is the difference between SCR and TRIAC?

RESULT:

The V-I characteristics of SCR are drawn and the Break-over voltage (V_{BO}), Holding current (I_H) of SCR are found.

1. The Break-over voltage (V_{BO}) of SCR is _____.
2. The Holding current (I_H) of SCR is _____.

Ex.No:11.a

DESIGN OF CLIPPER AND CLAMPER

Preparatory Questions

1. What is clipper?
2. What is clamper?
3. Difference between clipper and clamper?
4. What are different types of clampers?
5. Positive base and negative base clippers means

AIM:

To construct and study the operation of clipper and clamper circuits.

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE/SPECIFICATION	QUANTITY
1.	Resistor	4.7KΩ,100KΩ	1each
2.	Capacitor	0.1µf	1
3.	Diode	IN4001	1
4.	AFG	1MHz	1
5.	CRO	30MHz	1
6.	Bread Board		1
7.	Regulated power supply	(0 – 30)V	1

THEORY:

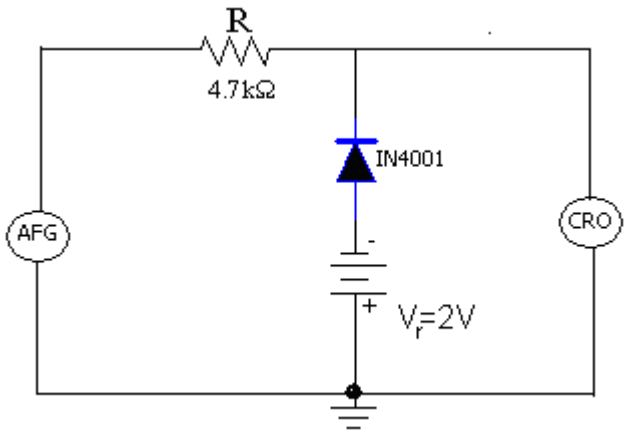
The basic action of a clipper circuit is to remove certain portions of the waveform, above or below certain levels as per the requirements. Thus the circuits which are used to clip off unwanted portion of the waveform, without distorting the remaining part of the waveform are called clipper circuits or Clippers. The half wave rectifier is the best and simplest type of clipper circuit which clips off the positive/negative portion of the input signal. The clipper circuits are also called limiters or slicers.

PROCEDURE

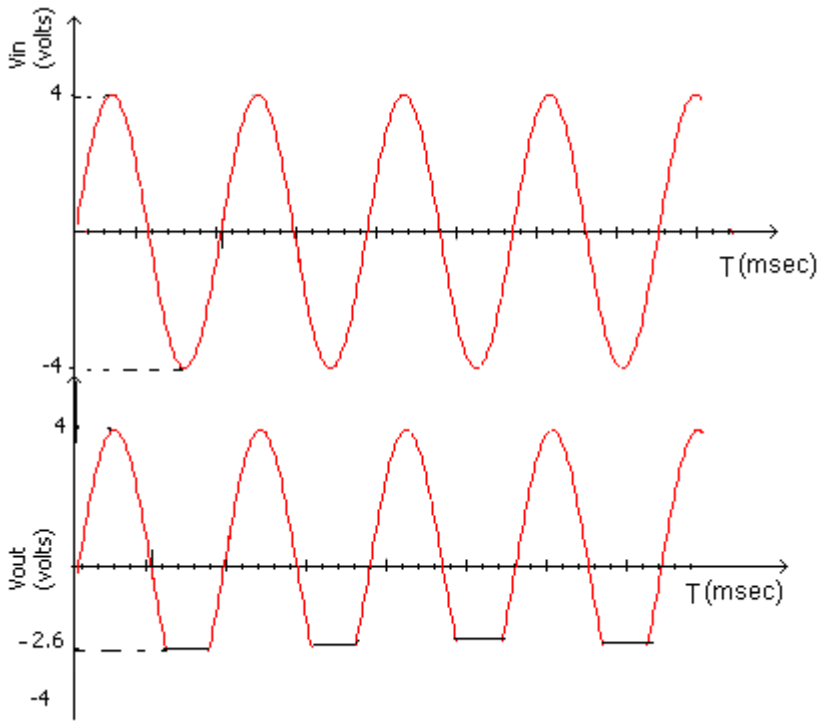
Clipper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1 kHz frequency and the reference voltage as 2V using RPS.
3. Observe the output across the diode using CRO.
4. Plot the input and output signal in a linear graph.

NEGATIVE PEAK CLIPPER



MODEL GRAPH



Theoretical calculations:

Vr=2v, Vγ=0.6v

When the diode is forward biased Vo =-(Vr+ Vγ) = -(2v+0.6v)= -2.6v

When the diode is reverse biased the Vo=Vi

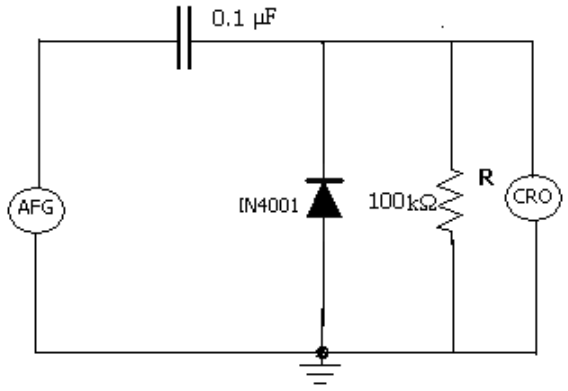
PROCEDURE

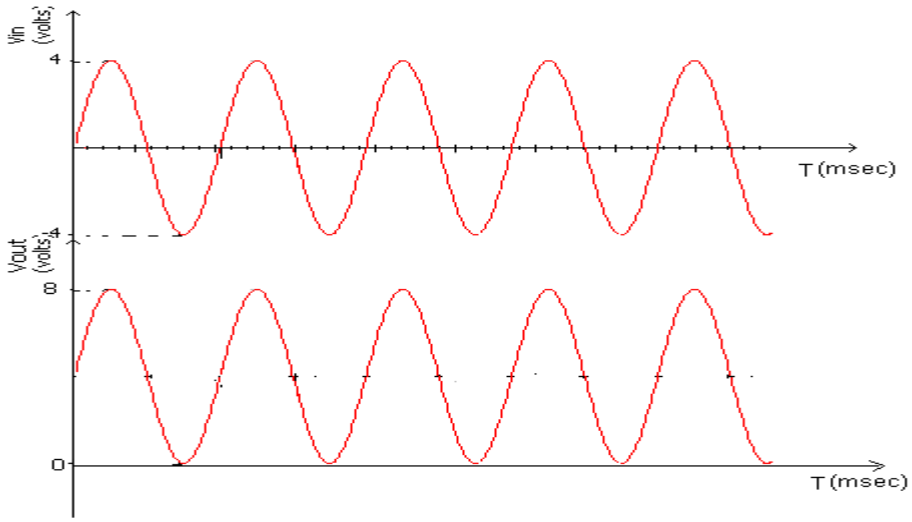
Clamper Circuit

1. Connect the components and apparatus as shown in the circuit diagram.
2. Set input, sinusoidal signal of 8Vp-p and 1kHz frequency
3. Observe the output across the load resistance using CRO.
4. Plot the input and output signal in a linear graph.

CIRCUIT DIAGRAM

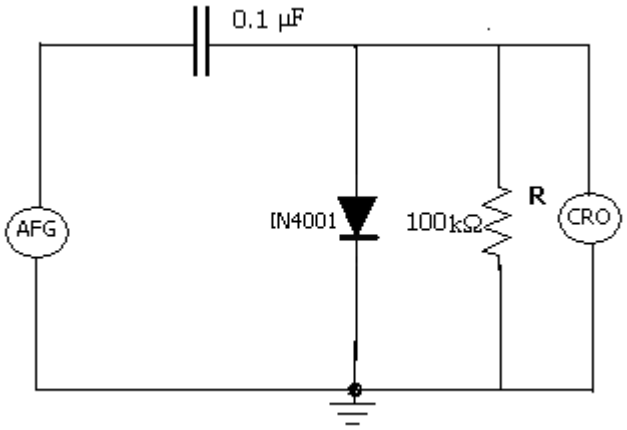
POSITIVE CLAMPER

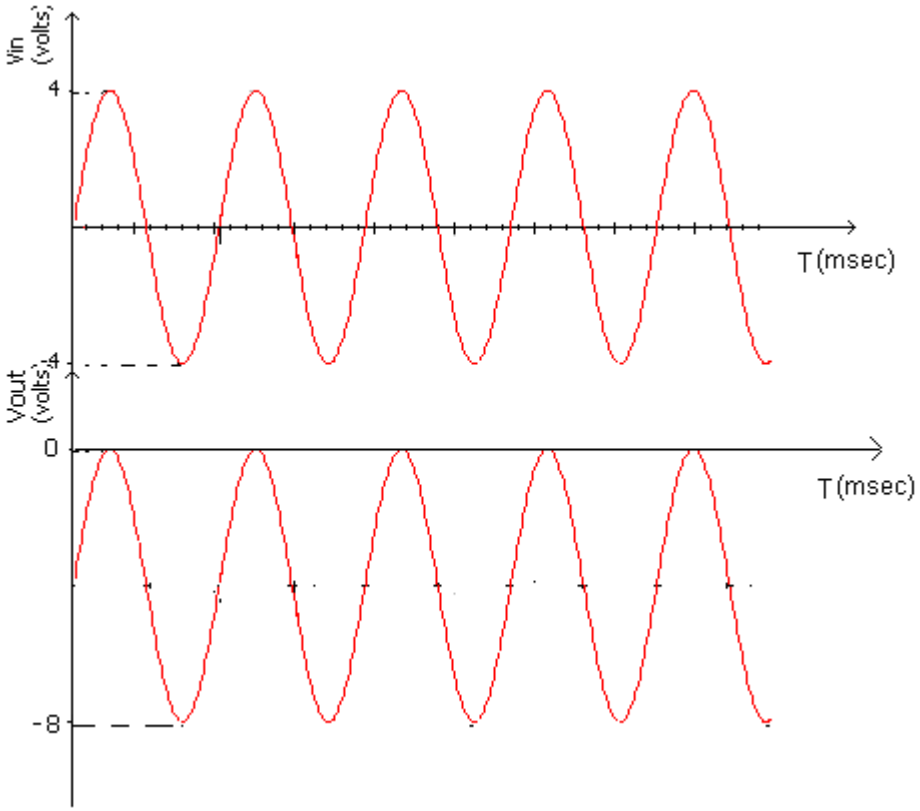




CIRCUIT DIAGRAM

NEGATIVECLAMPER





Review Questions:

1. How does a clamper circuit add a dc level to the output voltage?
2. What I do you mean by biased and combinational clipper?
3. What are the classifications of a clipper circuit?
4. Why capacitors are used in clampers?
5. What happens in the output waveform if the polarity of capacitor is changed in the clampers

RESULT:

Thus the clipper and clamper circuits are designed and the output waveforms are observed.

Ex.No:11.b

FULL WAVE RECTIFIER

Preparatory Questions

1. What is a Rectifier?
2. What are types and its difference?
3. What is ripple factor?
4. What is meant by regulation?
5. What is a filter?

AIM:

To construct full wave rectifier and to calculate ripple factor and regulation.

APPARATUS REQUIRED:

S,No	Name of the Component	Specification/Rating	Quantity(in number)
1.	Transformer	230 V / (9-0-9)	1
2.	Diode	IN4007	2
3.	Decade Resistance Box	(1KΩ-10 KΩ)	1
4.	Capacitor	100μF	1
5.	Voltmeter	(0-20V)MC	2
6	Multimeter	-	1
7.	Bread board , connecting wires	-	1,few

THEORY:

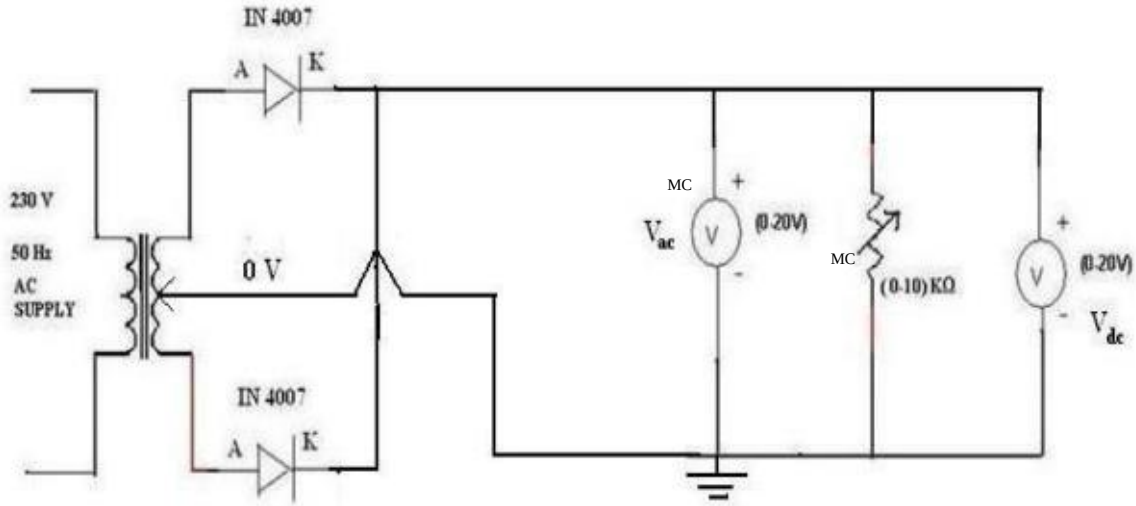
The full wave rectifier conducts for both the positive and negative half cycles of the input AC supply. In order to rectify both the half cycles of the AC input, two diodes are used in this circuit. The diodes feed a common load resistance with the help of a centre tapped transformer. The rectifier's DC output is obtained across the load. The DC load current for the full wave rectifier is twice that of the half wave rectifier. The efficiency of full wave rectification is twice that of half wave rectification. The ripple factor for the full wave rectifier is less compared to the half wave rectifier**.**

PROCEDURE:

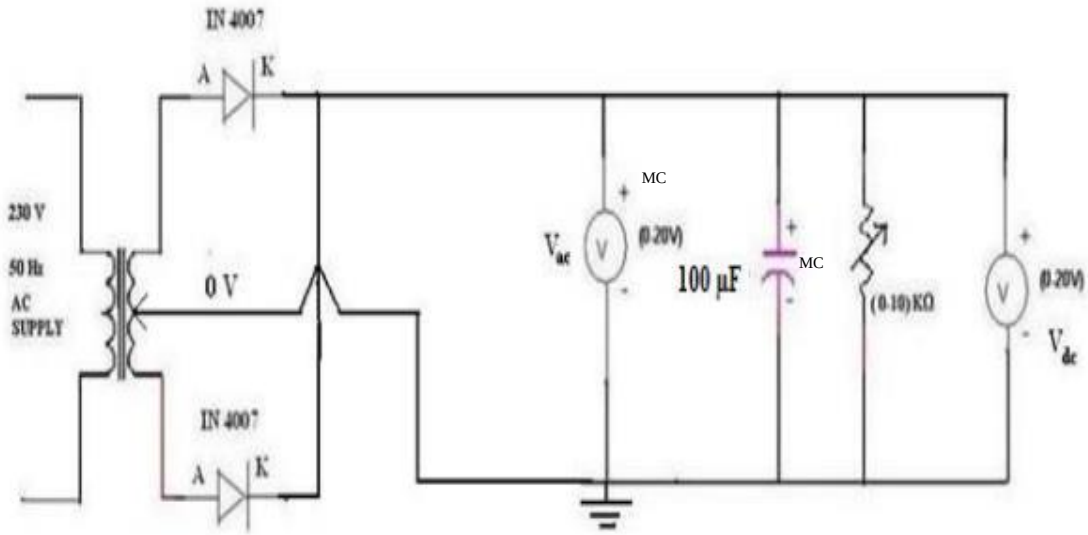
1. Connect the circuit as per the circuit diagram. For full wave rectifier without filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input
3. Switch on the supply.
4. Vary the DRB and note down the corresponding voltmeter and ammeter reading.
5. Calculate the ripple factor and regulation.
6. Repeat the above steps for full wave rectifier with filter.

CIRCUIT DIAGRAM:

FULLWAVE RECTIFIER WITHOUT FILTER:



FULLWAVE RECTIFIER WITH CAPACITIVE FILTER:



TABULATION:

FULL WAVE RECTIFIER WITHOUT FILTER

S.No.	V_{pp}	Time period	V_m	V_{ripple}	V_{dc}

FULL WAVE RECTIFIER WITH CAPACITIVE FILTER

S.No.	V_{pp}	Time period	V_m	V_{ripple}	V_{dc}

FORMULA USED:

Ripple Factor = $\frac{V_{ac}}{V_{dc}}$ and % Regulation = $\frac{V_{NL} - V_{FL}}{V_{NL}} * 100\%$

Review Questions:

1. What is a full wave rectifier?
2. What is the value of the ripple factor of a full wave rectifier?
3. What is the maximum efficiency that can be obtained in a full wave rectifier?
4. What is the advantage of full wave rectifier over half wave rectifier?
5. Define Transformer utilization factor.

RESULT:

Thus the full wave rectifier was constructed and the ripple factor and percentage regulation were calculated as,

Ripple factor: i) With filter = ii) Without filter =

% Regulation: i) With filter = ii) Without filter =

Ex.No:12

SIMULATION OF DIODE CHARACTERISTICS AND RECTIFIERS USING PSPICE

Preparatory Questions

1. What is meant by SPICE?
2. What is meant by simulation?
3. What is ORCAD
4. What is EDA tool?
5. List some EDA tools.

AIM:

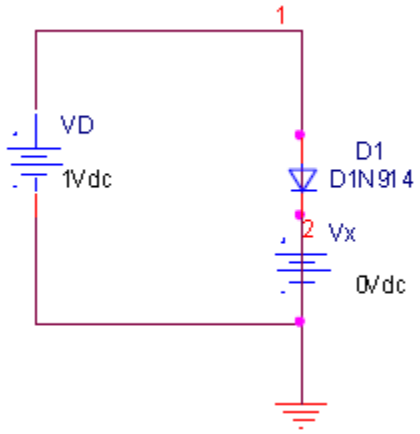
To Study and Simulate V-I characteristics of a Diode and Rectifiers using PSPICE windows.

APPARATUS REQUIRED:

PSPICE Tool

CIRCUIT DIAGRAM:

(i). DIODE:



PROGRAM:

vd 1 0 dc 1v

d1 1 2 d1n914;

vx 2 0 dc 0v;

.model D1N914 D(Is=168.1E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p

M=.3333 Vj=.75 Fc=.5 Isr=100p Nr=2 Bv=100 Ibv=100u Tt=11.54n)

.dc vd 0 1v 0.01v;

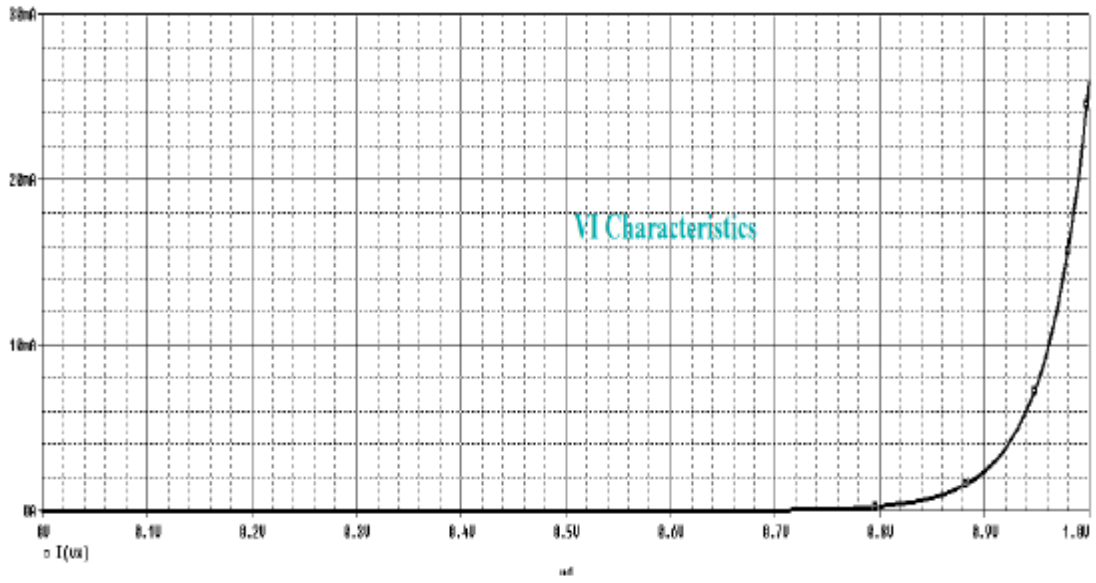
.plot dc I(vx);

.probe;

.tran 0us 100us;

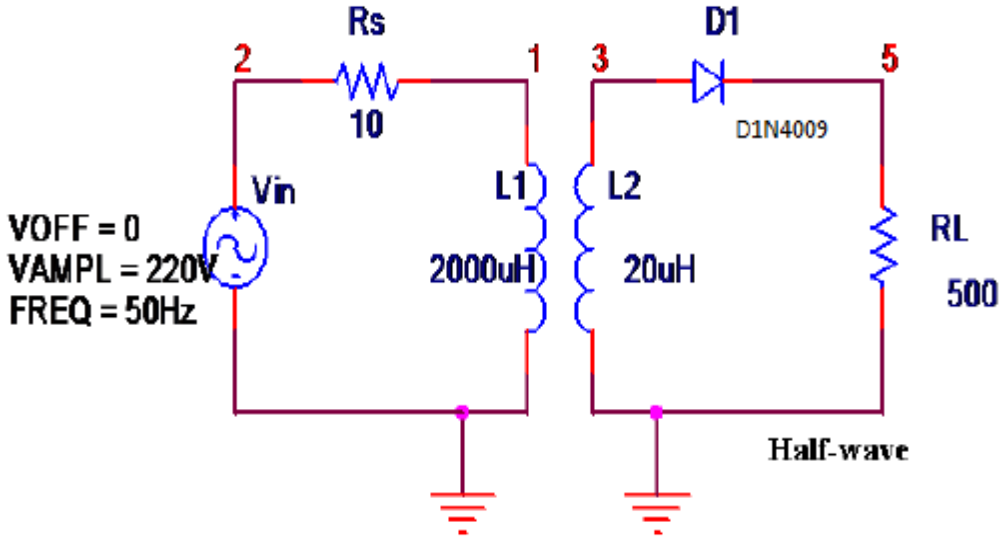
.end;

OUTPUT:



The forward biased silicon diode in an electronic system under dc condition has a drop of 0.7v across it in conduction state at any value of diode current.

(ii). HALF WAVE RECTIFIER :



PROGRAM:

VIN 2 0 sin(0 220V 50HZ)

RL 5 0 500

RS 2 1 10

L1 1 0 2000uH

L2 3 0 20uH

K1 L1 L2 0.99999

D1 3 5 D1N4009

.model D1N4009 D(Is=544.7E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p

M=.3333

+ Vj=.75 Fc=.5 Isr=30.77n Nr=2 Bv=25 Ibv=100u Tt=2.885n)

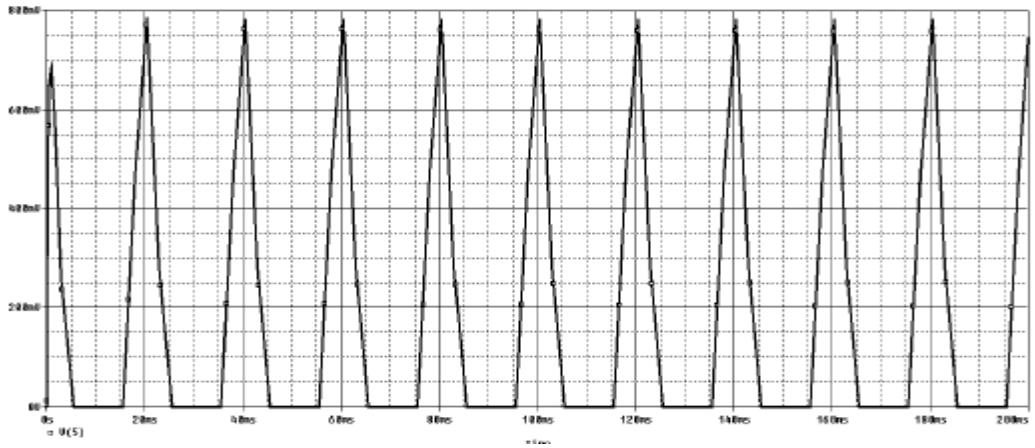
.tran 0.2m 200m

.plot tran v(3), v(5)

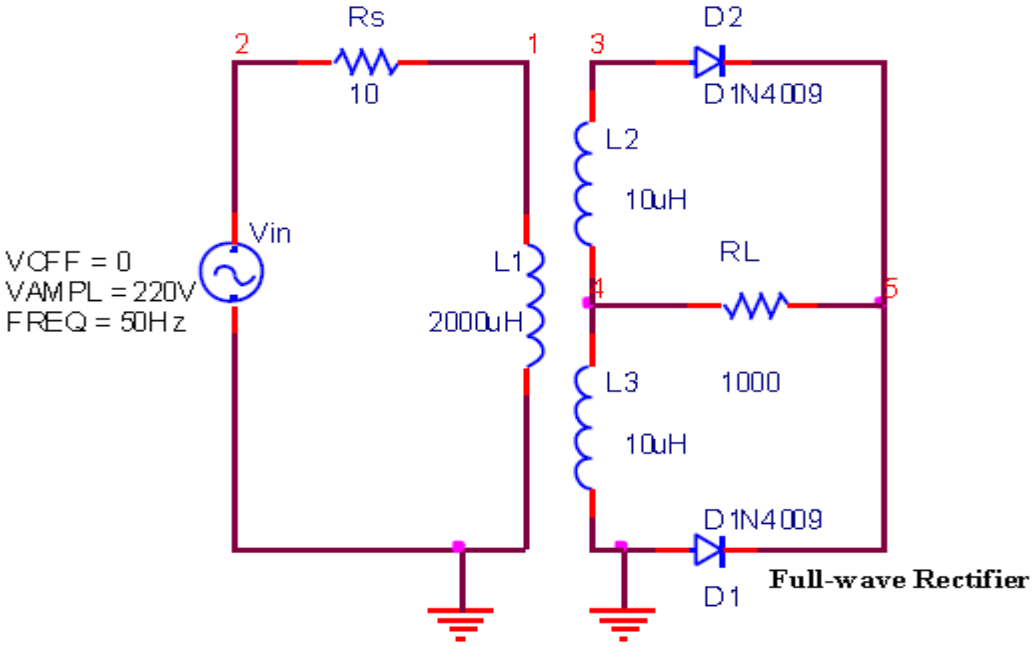
.probe

.end

OUTPUT:



(iii). FULL WAVE RECTIFIER :



PROGRAM:

Vin 2 0 sin(0 230V 50HZ)

RL 5 4 1000

RS 2 1 10

L1 1 0 2000

L2 3 4 10

L3 4 0 10

K1 L1 L2 L3 0.99

D1 0 5 D1N4009

D2 3 5 D1N4009

.model D1N4009

D(Is=544.7E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333

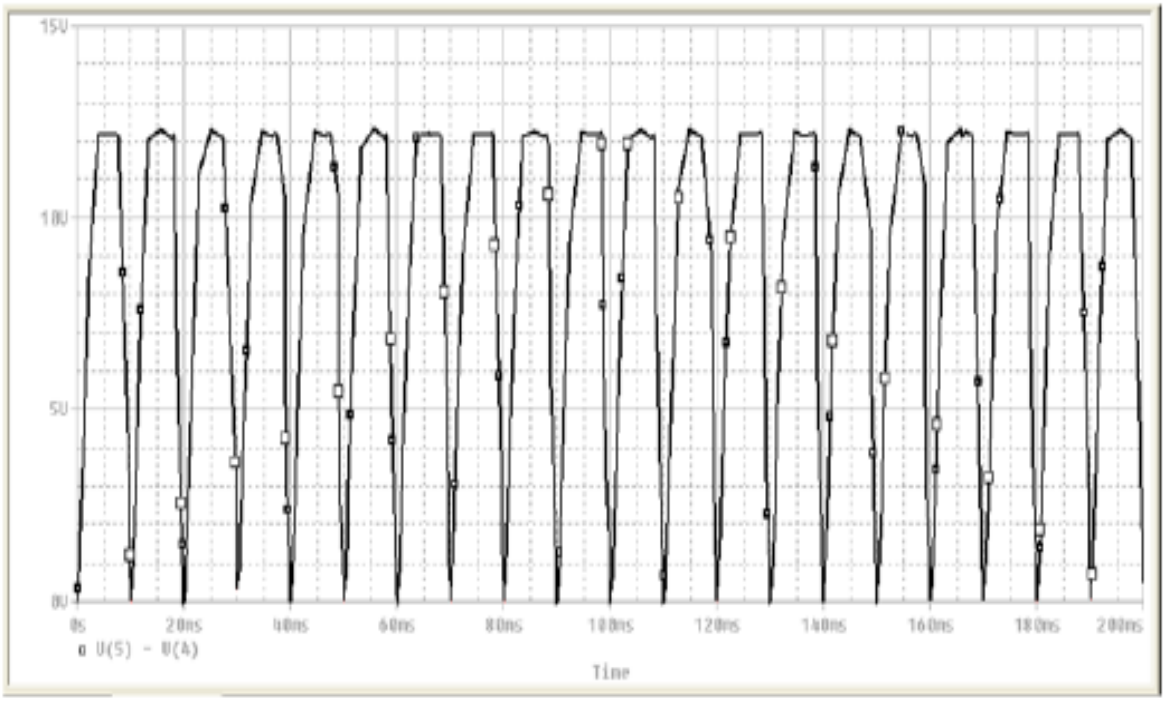
+ Vj=.75 Fc=.5 Isr=30.77n Nr=2 Bv=25 Ibv=100u Tt=2.885n)

.tran 0.2ms 200ms

.probe

.end

OUTPUT:



FULL WAVE RECTIFIER

Review Questions:

1. What is meant by AC and DC analysis?
2. What is meant by Transient Analysis?
3. What is use of Plot and Probe?
4. What are the uses of PSPICE?
5. List Advantages of PSPICE.

RESULT:

Thus the characteristics of Diode and Rectifier circuits are simulated using PSPICE

ADDITIONAL EXPERIMENTS

Ex.No:13

CHARACTERISTICS OF UNIJUNCTION TRANSISTOR

Preparatory Questions

1. What is UJT?
2. What is current controlled device?
3. What is voltage controlled device?
4. What are the charge carriers in UJT?
5. List the applications of UJT?

AIM:

To plot the characteristics of Uni-Junction transistor (UJT) & and to generate saw tooth waveform using UJT.

APPARATUS REQUIRED:

S,No	Name of the Component	Specification /Rating	Quantity(in number)
1.	Dual regulated power supply	(0 - 30V)	1
2.	Voltmeter	(0-30V)MC	2
3.	Ammeter	(0-30mA)MC	1
4.	Unijunction transistor	2N2646	1
5.	Resistors	560Ω,1KΩ	Each one
6.	Bread board, connecting wires.	-	1,few
7.	CRO	-	-

THEORY:

The UJT consists of a bar of lightly doped N type Si with a small piece of heavily doped p-type joined to one side of the base. The two terminals of the N-type bar are designated as Base 1 (B_1) and Base 2 (B_2) the P type region is termed as the emitter (E) .Since the Si bar is lightly doped, it exhibits high resistance which can be represented as two resistors (R_{B1} and R_{B2}). Let V_1 be the voltage across R_{B1} and V_2 be the voltage across R_{B1} where R_{B1} and R_{B2} are the base resistances. If the emitter is forward biased and the forward bias voltage is greater than V_2, the emitter current starts flowing. The voltage at which the device starts conducting is called the peak Voltage (V_p) .When the emitter voltage is increased beyond V_p, the charge carriers are injected into N region and the resistance starts decreasing .Now the device enters the negative resistance region .As the voltage decreases, the emitter current increases. When the current reaches a certain limit, the resistance is saturated and the voltage falls to a low value called valley voltage (V_V). The intrinsic standoff ratio is found with the values of V_p, V_v and V_{B1B2}If the voltage is increased further the emitter current increases rapidly, with slight increase in emitter voltage similar to a forward diode.

PROCEDURE:

CHARACTERISTICS OF UJT

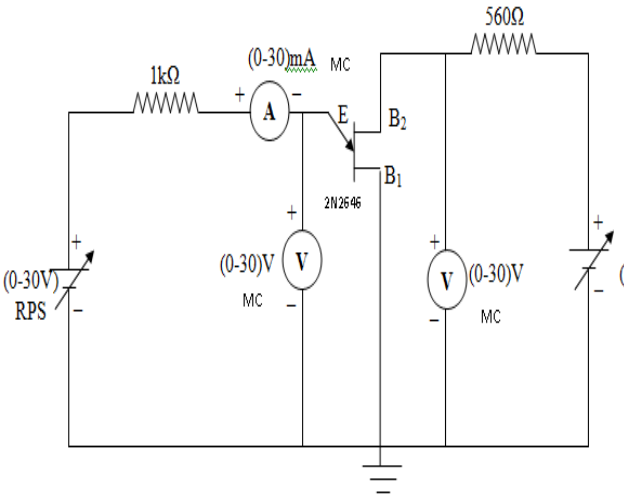
1. The connections are given as per the circuit diagram.
2. The power supply is switched ON.
3. The voltage across B_1 and B_2 ($V_{B1\,B2}$) is set to some desired value.
4. The emitter voltage (V_E) is slowly increased. At a certain voltage, the device starts conducting .The voltage at this point is called the peak voltage (V_P). With the supply voltage is increased further, the emitter voltage falls and the current increases and in each step, the readings are tabulated.
5. The experiment is repeated for different values of $V_{B1\,B2}$.
6. The characteristics are plotted between emitter current along X axis and emitter voltage along Y axis for different values of $V_{B1\,B2}$ .The peak and valley voltage are marked on the graph.

SAW TOOTH WAVEFORM GENERATION

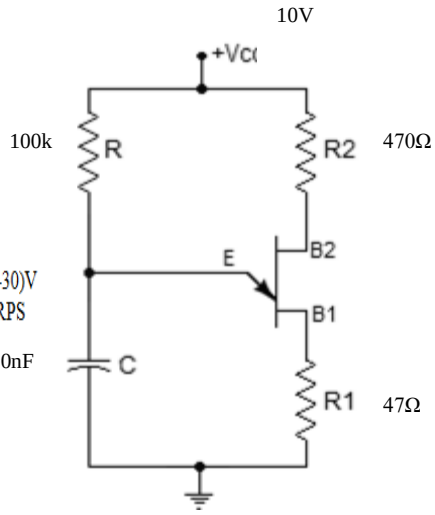
1. The connections are given as per the circuit diagram.
2. The power supply is switched ON.
3. The output saw tooth waveform is generated across the capacitor is seen in a CRO.
4. The frequency and amplitude of the waveform is noted and sketched.

CIRCUIT DIAGRAM:

CHARACTERISTICS OF UJT

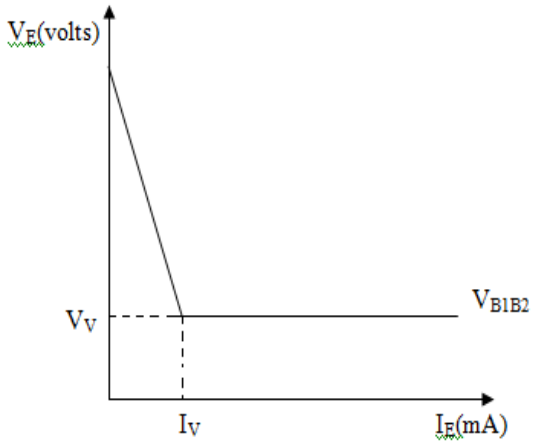


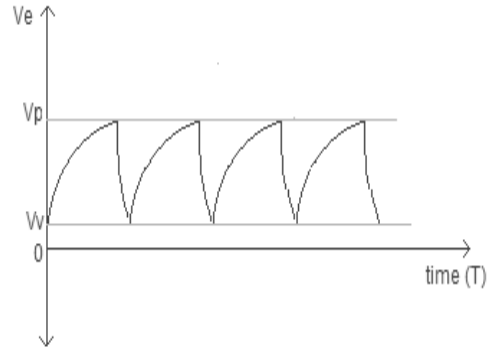
SAWTOOTH WAVEFORM GENERATION



MODEL GRAPH:

CHARACTERISTICS OF UJT **SAWTOOTH WAVEFORM**





Wave form across the capacitor in a UJT relaxation oscillator

TABULAR COLUMN:

S.No	V_{B1B2}=10V		V_{B1B2}=15V	
	V_E(V)	I_E(mA)	V_E(V)	I_E(mA)

CALCULATIONS:

Intrinsic standoff ratio $\eta = \dfrac{V_P - V_V}{V_{B1B2}}$

Review Questions:

1. What is the difference between UJT and BJT?
2. Define peak and valley voltage.
3. What is intrinsic standoff ratio of a UJT?
4. What are advantages of UJT?
5. How does UJT differ from a FET?

RESULT:

The characteristic of UJT is drawn and the saw tooth waveform is plotted.

Peak Voltage V_p =

Intrinsic standoff ratio (η) =

Ex.No:14

FREQUENCY RESPONSE OF SERIES AND PARALLEL RESONANCE CIRCUITS

Preparatory Questions

1. What is a parallel resonant circuit?
2. What is a series resonant circuit?
3. What are tuned circuits?
4. When the circuit is said to be in resonance?
5. What is resonant frequency?

AIM:

To plot the current vs frequency graph of series and parallel resonance circuits and hence measure the bandwidth, resonant frequency.

APPARATUS REQUIRED:

Sl.No	Name	Range	Qty
1.	Signal Generator	2MHz	1
2.	CRO	30MHz	1
3.	Connecting Wires		
4.	Resistors	1K, 470Ω,100Ω	1 each
5.	Capacitors	0.01uF, 0.1µf	2
6.	Inductors	99mH, 300mH	1
7.	Bread Board		1

Circuit Description ForRLC Series Circuit:

A circuit is said to be in resonance when applied voltage V and current I are in phase with each other. Thus at resonance condition, the equivalent complex impedance of the circuit consists of only resistance (R). So current is maximum. Since V and I are in phase, the power factor is unity.

When the frequency is equal to complex impedance

$V = R + j (X_L – X_C)$

Where

$X_L = \omega L$

$X_C = 1/\omega C$

Resonance Curve:

The curve between current and frequency is known as resonance curve. The shapes of such curve for of R as shown in fig (1). For smaller values of R, current Vs frequency wave is sharply peak, but for larger values of R, it is flat.

Bandwidth of a Resonance Circuit:

Bandwidth of a circuit is given by the band of frequencies which lies between two points on either side of resonance frequency, where current falls through 1/1.414 of the maximum value of resonance. Narrow is the bandwidth, higher the selectivity of the circuit. As shown in fig, the bandwidth AB is given by $F_2 - F_1$. F_1 is the lower cut off frequency and F_2 is the upper cut off frequency.

Q - Factor:

In the case of a RLC series circuit, it is defined as equal to the voltage magnification in the circuit at resonance. At resonance, current is maximum. $I_o = V/R$.

The applied voltage $V = I_oR$
Voltage magnification = $V_L/V = I_oX_L$

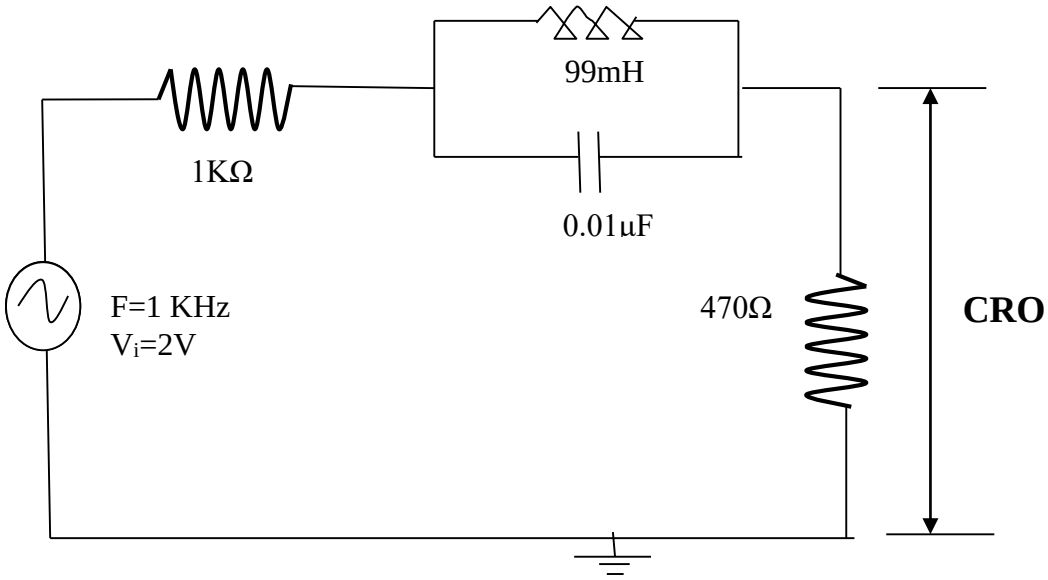
In the case of resonance, high Q factor means not only high voltage, but also higher sensitivity of tuning circuit. Q factor can be increased by having a coil of large inductance, not of smaller ohmic resistance.

$$Q = \omega L / R$$

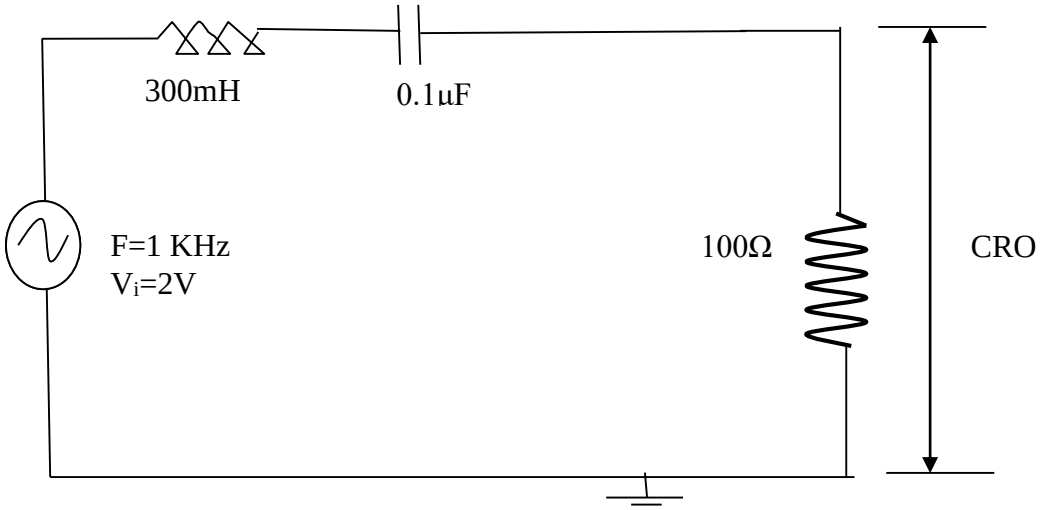
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. By varying the frequency and note down the corresponding meter reading.
3. Draw the current V_S frequency curve and measure the bandwidth, resonance frequency and Q factor.

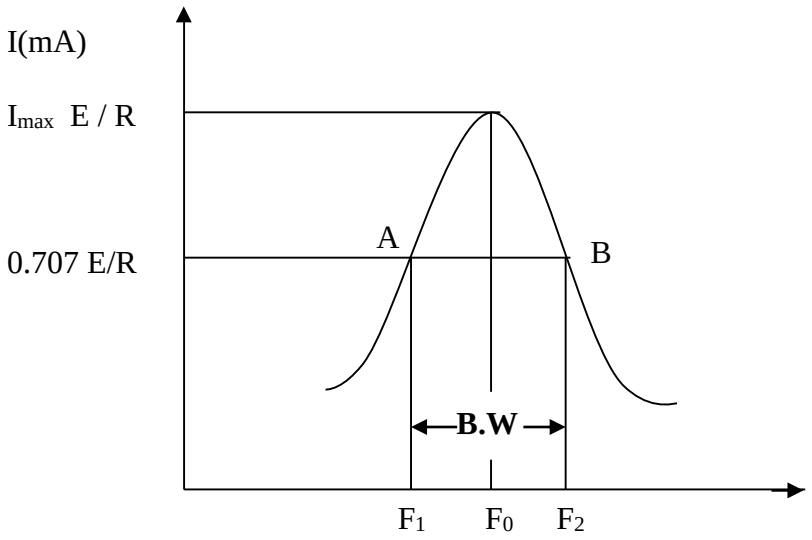
RLC Parallel Resonance Circuit:



RLC Series Resonance Circuit:

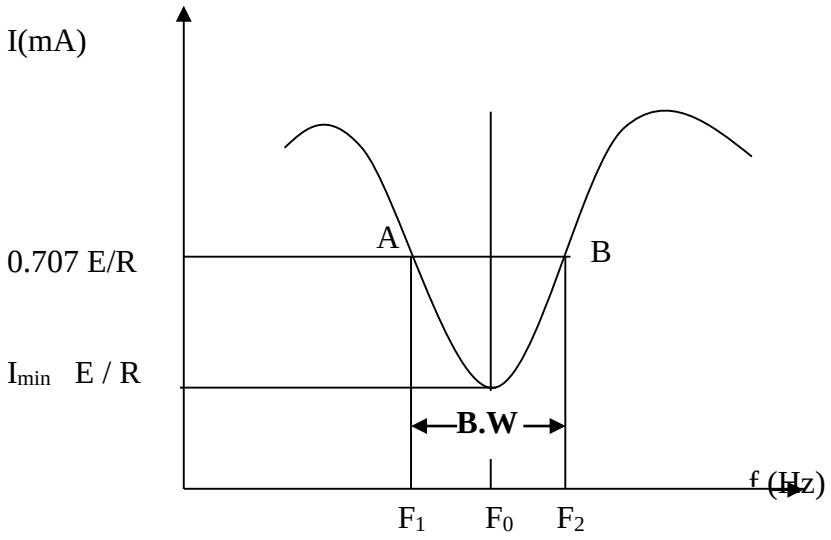


Series Resonance Curve:



Bandwidth B. W = $F_2 - F_1$
Resonant Frequency = F_0

Parallel Resonance Curve:



TABULATION:

Series circuit*:*

Input Voltage: V

S.No	Frequency (Hertz)	Output Voltage (V)	Current (mA)

Parallel circuit:

Input Voltage: V

S.No	Frequency (Hertz)	Output Voltage (V)	Current (mA)

Review Questions:

1. Explain series resonance.
2. Define Q factor.
3. What is coefficient of coupling?
4. What is transient response?
5. Briefly explain the series & parallel connection of independent source.

RESULT:

Thus the frequency curve of series and parallel circuits are drawn.