SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM NAGAR, KATTANKULATHUR – 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LABORATORY MANUAL

1906305 - ANALOG AND DIGITAL ELECTRONICS LABORATORY

Regulation - 2019

Semester/Branch	**:**	**III semester ECE**
Academic Year	**:**	**2022 -23 (ODD)**
Prepared By	**:**	**Mr. A. Anbarasan, A.P (O.G)**
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION OF THE INSTITUTE

Educate to excel in social transformation

MISSION OF THE INSTITUTE

• To contribute to the development of human resources in the form of professional engineers and managers of international excellence and competence with high motivation and dynamism, who besides serving as ideal citizen of our country will contribute substantially to the economic development and advancement in their chosen areas of specialization.
• To build the institution with international repute in education in several areas at several levels with specific emphasis to promote higher education and research through strong institute-industry interaction and consultancy.

VISION OF THE DEPARTMENT

To excel in the field of electronics and communication engineering and to develop highly competent technocrats with global intellectual qualities.

MISSION OF THE DEPARTMENT

M1: To educate the students with the state of art technologies to compete internationally, able to produce creative solutions to the society`s needs, conscious to the universal moral values, adherent to the professional ethical code
M2: To encourage the students for professional and software development career
M3: To equip the students with strong foundations to enable them for continuing education and research.

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PROGRAM OUTCOMES

1.Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2.Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3.Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4.Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5.Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6.The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7.Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8.Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9.Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10.Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11.Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12.Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOME(PSOs)

PSO1: Ability to apply the acquired knowledge of basic skills, mathematical foundations, principles of electronics, modelling and design of electronics based systems in solving engineering Problems.
PSO2: Ability to understand and analyze the interdisciplinary problems for developing innovative sustained solutions with environmental concerns.
PSO3: Ability to update knowledge continuously in the tools like MATLAB, NS2, XILINIX and technologies like VLSI, Embedded, Wireless Communications to meet the industry requirements.
PSO4: Ability to manage effectively as part of a team with professional behaviour and ethics.

SYLLABUS

1906305 - ANALOG AND DIGITAL ELECTRONICS LABORATORY **L T P C**
0 0 4 2

OBJECTIVES:

The student should be made to:

- ✓ Determine the Frequency response of CE, CB and CC Amplifier.
- ✓ Learn the frequency response of CS Amplifiers.
- ✓ Study the Transfer characteristics of differential amplifier.
- ✓ Perform experiment to obtain the bandwidth of single stage and multistage. Amplifiers.
- ✓ Do SPICE simulation of Electronic Circuits.

LIST OF ANALOG EXPERIMENTS:

1. Design of Regulated power supplies.
2. Frequency Response of CE, CB, CC and CS Amplifiers.
3. Darlington Amplifier.
4. Differential Amplifiers- Transfer characteristic, CMRR Measurement.
5. Cascode and Cascade amplifier.
6. Determination of bandwidth of single stage and multistage amplifiers.
7. Analysis of BJT with fixed bias and voltage divider bias using Spice.
8. Analysis of FET, MOSFET with fixed bias, self-bias and voltage divider bias using simulation software like Spice.
9. Analysis of Cascode and Cascade amplifiers using Spice.
10. Analysis of Frequency Response of BJT and FET using Spice.

LIST OF DIGITAL EXPERIMENTS

11. Design and implementation of code converters using logic gates (i) BCD to excess-3 code and vice versa (ii) Binary to gray and vice-versa.
12. Design and implementation of 4 bit binary Adder/ Sub tractor and BCD adder using IC 7483.
13. Design and implementation of Multiplexer and De-multiplexer using logic gates.
14. Design and implementation of encoder and decoder using logic gates.
15. Construction and verification of 4 bit ripple counter and Mod-10 / Mod-12 Ripple counters.
16. Design and implementation of 3-bit synchronous up/down counter.

TOTAL: 60 PERIODS

OUTCOMES:

On completion of this lab course, the student would be able to,

- ✓ Test rectifiers, filters and regulated power supplies.
- ✓ Understand BJT/JFET amplifiers.
- ✓ Design Cascode and cascade amplifiers.
- ✓ Analyze the limitation in bandwidth of single stage and multi stage amplifier.
- ✓ Simulate and analyze amplifier circuits using PSpice.

LIST OF EXPERIMENTS

CYCLE-I

ANALOG EXPERIMENTS

1. Design of Regulated power supplies.
2. Frequency Response of CE, CB, CC and CS Amplifiers
3. Darlington Amplifier
4. Differential Amplifiers- Transfer characteristic, CMRR Measurement
5. Cascode and Cascade amplifier
6. Determination of bandwidth of single stage and multistage amplifiers
7. Analysis of BJT with fixed bias and voltage divider bias using Spice
8. Analysis of FET, MOSFET with fixed bias, self-bias and voltage divider bias using simulation software like Spice
9. Analysis of Cascode and Cascade amplifiers using Spice
10. Analysis of Frequency Response of BJT and FET using Spice

CYCLE-II

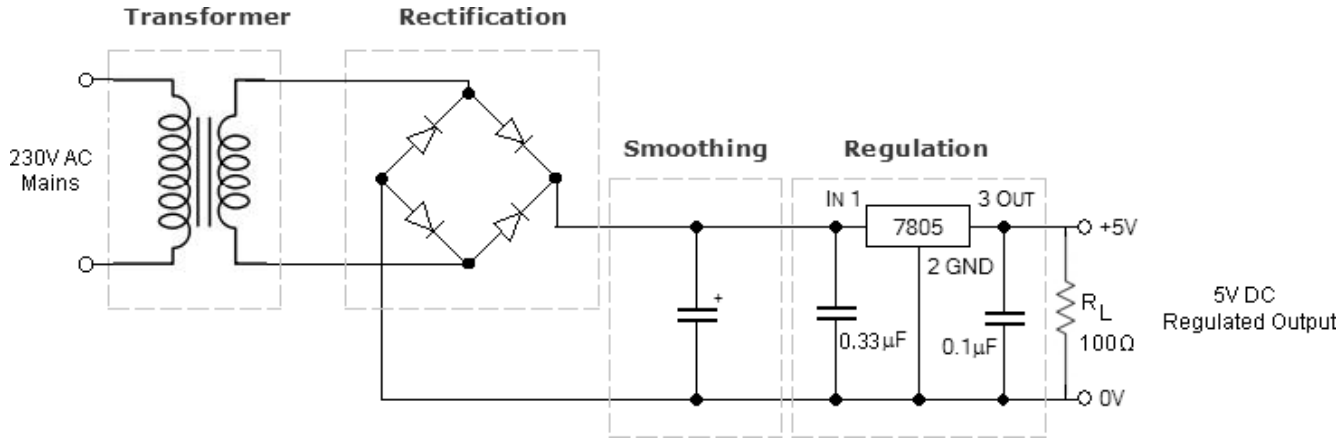
DIGITAL EXPERIMENTS

11. Study of Logic Gates and Flip Flops
12. Design and implementation of code converters using logic gates (i) BCD to excess-3 code and vice versa (ii) Binary to gray and vice-versa
13. Design and implementation of 4 bit binary Adder/ Subtractor and BCD adder using IC 7483
14. Design and implementation of Multiplexer and De-multiplexer using logic gates
15. Design and implementation of encoder and decoder using logic gates
16. Construction and verification of 4 bit ripple counter and Mod-10 / Mod-12 Ripple counters
17. Design and implementation of 3-bit synchronous up/down counter

ADDITIONAL EXPERIMENTS

18. Design and implementation of 2 Bit Magnitude Comparator

CIRCUIT DIAGRAM



EXPT. NO: 1 DESIGN OF REGULATED POWER SUPPLY

DATE:

AIM:

To design a +5 V DC regulated power supply delivering up to 1A of current to the load. Also to determine the load regulation and efficiency of the regulated power supply.

COMPONENTS REQUIRED:

S.NO	Name of the Component	Specification/Range	Quantity
1.	Diode	1N4007	04
2.	IC	IC7805	01
3.	Step down transformer	230 V/ 9 V, 1A	01
4.	Resistor	100Ω	01
5.	Capacitor	0.33μF, 0.1μF	Each 1
6.	Electrolytic Capacitor	1000μF/25V	01
7.	Function Generator	3 MHz	01
8.	RPS	(0-30)V	01
9.	CRO	30 MHz	01
10.	Bread Board		01
11.	Connecting Wires	Single stand	few

PRE-LAB EXERCISE

1. Design and create a SPICE model of a bridge-type, full-wave rectified, dc power supply using a filter capacitor.
2. Analyze the circuit for different values of filter capacitors. Observe the change in ripple content and comment on your observation.
3. Analyze the circuit for different load conditions. Observe the change in ripple content and comment on your observation.
4. From the IC 7805 datasheet, write down the minimum, typical and maximum values of the output voltage V0.
5. Determine the smallest value of the input voltage VI for which IC7805 can still work as a voltage regulator.

THEORY:

Every electronic circuit is designed to operate off of supply voltage, which is usually constant. A regulated power supply provides this constant DC output voltage and continuously holds the output voltage at the design value regardless of changes in load current or input voltage.

The power supply contains a rectifier, filter, and regulator. The rectifier changes the AC input voltage to pulsating DC voltage. The filter section removes the ripple component and provides an unregulated DC voltage to the regulator section. The regulator is designed to deliver a constant voltage to the load under varying circuit conditions. The two factors that can cause the voltage across the load to vary are fluctuations in input voltage and changes in load current requirements.

Load regulation is a measurement of power supply, showing its capacity to maintain a constant voltage across the load with changes in load current. Line regulation is a measurement of power supply, showing its capacity to maintain a constant output voltage with changes in input voltage.

DESIGN

Design a 5 V DC regulated power supply to deliver up to 1A of current to the load with 5% ripple. The input supply is 50Hz at 230 V AC.

Selection of Voltage regulator IC:

Fixed voltage linear IC regulators are available in a variation of voltages ranging from -24V to +24V. The current handling capacity of these ICs ranges from 0.1A to 3A. Positive fixed voltage regulator ICs have the part number as 78XX. The design requires 5V fixed DC voltage, so 7805 regulator IC rated for 1A of output current is selected.

Selection of Bypass Capacitors:

The data sheet on the 7805 series of regulators states that for best stability, the input bypass capacitor should be 0.33µF. The input bypass capacitor is needed even if the filter capacitor is used. The large electrolytic capacitor will have high internal inductance and will not function as a high frequency bypass; therefore, a small capacitor with good high frequency response is required. The output bypass capacitor improves the transient response of the regulator and the data sheet recommends a value of 0.1µF.

Dropout voltage:

The dropout voltage for any regulator states the minimum allowable difference between output and input voltages if the output is to be maintained at the correct level. For 7805, the dropout voltage at the input of the regulator IC is Vo +2.5 V.

$$V_{dropout} = 5+2.5 = 7.5V$$

Selection of Filter Capacitor:

The filter section should have a voltage of at least 7.5V as input to regulator IC.

That is Vdc = 7.5 V

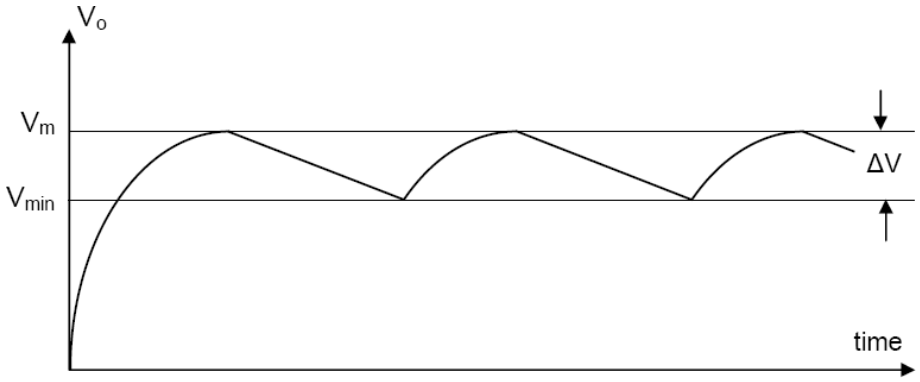


Figure 2: Output wave shape from a full-wave filtered rectifier

Ripple voltage = ΔV = Vr

Two figures of merit for power supplies are the ripple voltage, Vr, and the ripple factor, RF.

RF = Vr(rms) / Vdc $\qquad v_{r\,(rms)} = \frac{v_m - v_{min}}{2\sqrt{3}} = \frac{v_r}{2\sqrt{3}}$

V_{dc} = 2Vm/π = 0.636 Vm

$$v_{dc} = v_m - \frac{v_r}{2} = \frac{v_m + v_{min}}{2}$$

Vr = IL x Toff/C can be solved for the value of C.
The ripple frequency of the full-wave ripple is 100 Hz. The off-time of the diodes for 100 Hz ripple is assumed to be 85%. Toff = 8.5mS.
C = IL x Toff / Vr

Selection of Diodes:

1N4007 diodes are used as it is capable of withstanding a higher reverse voltage, PIV of 1000V whereas 1N4001 has PIV of 50V.

Selection of Transformer:

Maximum unregulated voltage, Vunreg(max) = Vdropout + Vr =
Two diodes conduct in the full-wave bridge rectifier, therefore peak of the secondary voltage must be two diode drops higher than the peak of the unregulated DC.

Vsec(peak) = Vunreg(max) + 1.4V =

Vsec(rms) = 0.707 x Vsec(peak) =

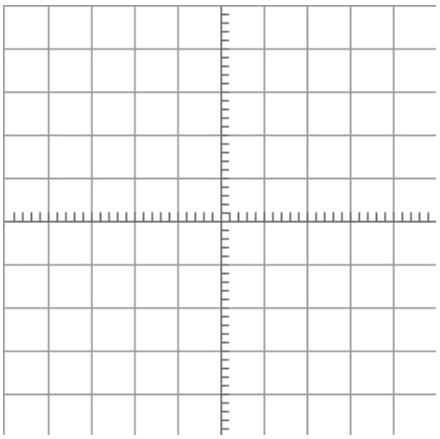
The power supply is designed to deliver 1A of load current, so the secondary winding of the transformer needs to be rated for 1A.

PROCEDURE:

1. Power Supply

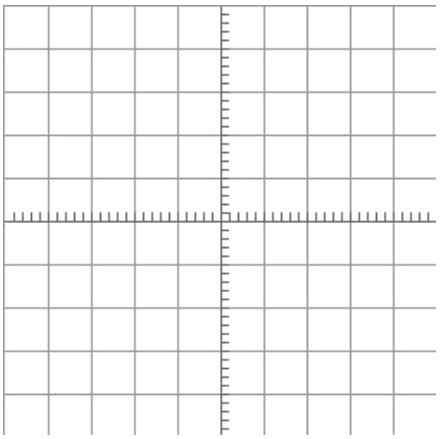
1. Connect the circuit as shown in Figure 1 .
2. Apply 230V AC from the mains supply.
3. Observe the following waveforms using oscilloscope
   (i) Waveform at the secondary of the transformer
   (ii) Waveform after rectification
   (iii) Waveform after filter capacitor
   (iv) Regulated DC output

Volt/div = Time/div =



Graph 1: Waveform at the secondary of the transformer

Volt/div = Time/div =



Graph 2: Waveform after rectification

Volt/div = Time/div=

2. Load Regulation

1. Observe the No load voltage and Full load voltage
2. Calculate the load regulation.

Load Regulation = ((VNL – VFL)/VFL) x 100 %

Theoretical efficiency of linear voltage regulator =

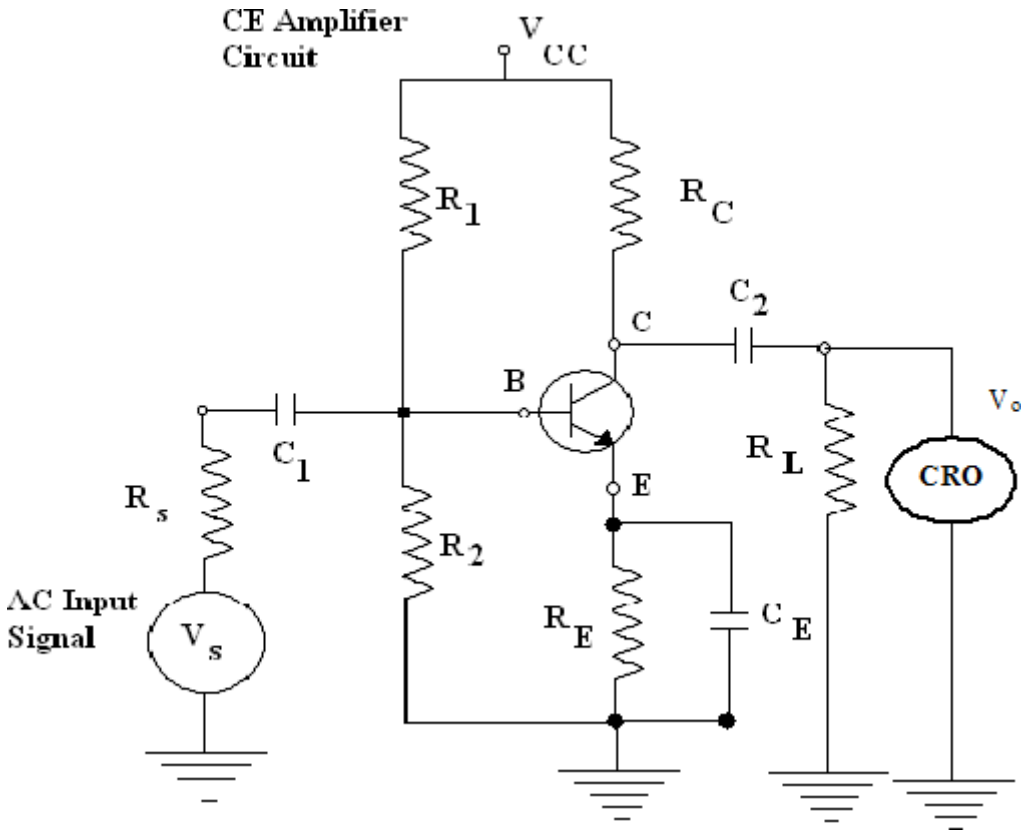
POST-LAB EXERCISE

1. Why is the ripple voltage larger at full load?
2. Under full load conditions, what is the power dissipated by the regulator IC?
3. Comment on the efficiency of the circuit for a minimum output voltage and a maximum output voltage.
4. Identify the short-circuit current of 7805 from data sheets.
5. What modification needs to be done to obtain a variable output voltage?

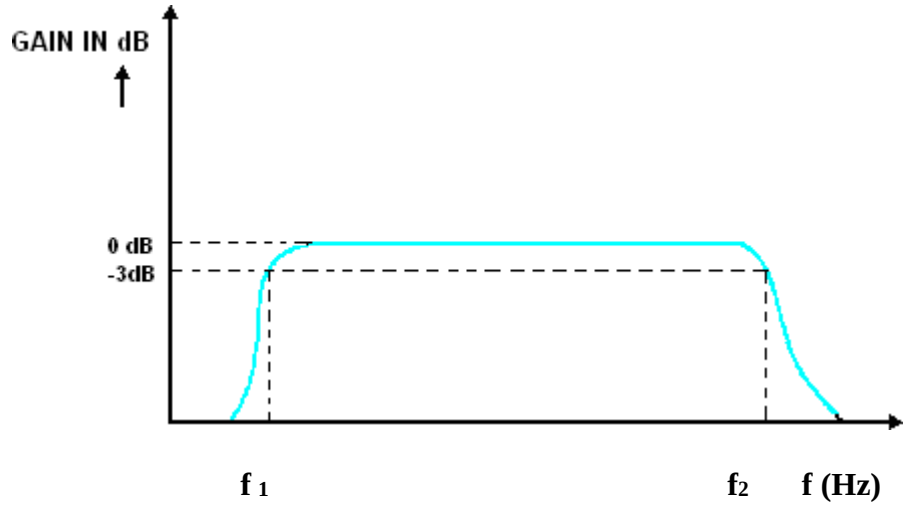
RESULT:

Thus the +5 V DC regulated power supply was designed and also the load regulation and efficiency of the regulated power supply was determined.

CIRCUIT DIAGRAM:



MODEL GRAPH: FREQUENCY RESPONSE CURVE



EXPT. NO: 2 FREQUENCY RESPONSE OF CE / CB / CC AMPLIFIER

DATE:

EXPT. NO: 2A FREQUENCY RESPONSE OF CE AMPLIFIER

AIM:

To design a BJT Common Emitter (CE) Amplifier using voltage divider bias (self-bias) bypassed emitter resistor to

- Measurement of gain
- Plot the frequency response & Determination of Gain Bandwidth Product.

COMPONENTS REQUIRED:

S.NO	Name of the Component	Specification/Range	Quantity
1.	Transistor	(BC547)	01
2.	Resister	180KΩ, 39KΩ, 1KΩ, 3.9KΩ, 120Ω, 470 Ω, 2.2 KΩ, DRB	Each 1
3.	Capacitor	4.7μF, 10 μF	01,02
4.	Function Generator	2MHz	01
5.	RPS	(0-30)V	01
6.	CRO	30MHz	01
7.	Bread Board		01
8.	Connecting Wires	Single stand	few

PRE-LAB EXERCISE

1. What are the types of bias compensation techniques?
2. What type of biasing used in this amplifier?
3. What are the advantages & disadvantages of RC coupled or CE amplifier?
4. Compare RC Coupled amplifier with Transformer coupled amplifier and Direct coupled amplifier.
5. Define Bandwidth.

THEORY:

In CE amplifier, the input is applied between Base & Emitter and the output is taken between Collector & Emitter. As Emitter is common to both input & output, hence the name Common Emitter amplifier.

When V_{in} goes +ve, V_b increases. This increases I_b and hence I_c. This increases the voltage drop at Rc & Vc decreases. Thus whenever there is a +ve swing at the input, there is a –ve swing at the Collector. Similarly, whenever there is a -ve swing at the input, there is a +ve swing at the Collector. Or, there is 180 degree phase difference between input & output voltages. A small change at the input gives a large change at the output resulting in amplification.

In RC coupled CE amplifier, Resistances R_1, R_2 and R_E set the proper operating point for the CE amplifier. Input Capacitor C1

– Couples the signal to the base of the transistor

- Blocks DC and allows only AC Signal for Amplification & thereby ensures Constant biasing conditions.

DESIGN

Given A_V=10, h_{fe}=300, V_{CC}=10, I_{CQ}=2mA and f=200Hz

Step 1

$V_{CEQ}=V_{CC}$ /2= 10 /2 =5V

Step 2

$V_E=I_ER_E=V$ /10 =1V

Step 3

$R_E=V_E/I_E$= 1/ ($2*10^{-3}$) =0.5KΩ ≈470Ω

Step4

V_B =V_E+0.7 =1+0.7 =1.7V

Let R_1=180KΩ

Step5

$V_B=R_2(V_{CC}/(R_1+R_2))$

1.7 =R_2 (10/(180K +R_2))

306K+1.7R_2 =10R_2

306KΩ =8.3R_2

R_2=306K/8.3=36.8KΩ ≈39KΩ

Step6

$V_{CC}=I_CR_C+V_{CE}+I_ER_E$

$R_C=(V_{CC}-V_{CE}-I_ER_E)/ I_C$ =(10-5-1)/($2*10^{-3}$)=2KΩ ≈2.2KΩ

Step7

r_e'=25mV/ I_E=$25*10^{-3}/2*10^{-3}$=12.5Ω

Step8

A_V =($R_C||R_L$) / r_e'

10 =($R_C||R_L$) /12.5

($R_C||R_L$)=125Ω

On solving, R_L=132.5Ω ≈120Ω

Step9

($R_1||R_2$) =R_B=32054.7Ω

X_{C1}= ($h_{ie}||R_B||h_{fe}R_E$)/10=($h_{ie}||R_B$)/10=(1K||32054.7)/10=96.97Ω

C_1 = 1/2∏f X_{C1} = 1/2π*200*96.97=8.2μF ≈10μF

Step10

X_{C2}= (R_C+R_L)/10 =232Ω

C_2 = 1 /2πf X_{C2}=1 /2π*200*232=3.4μF ≈4.7μF

Step11

$X_{E/10}$= R_E/10= 470=47Ω

C_E = 1/2πf X_E=1/ 2π*200*47=16.9μF ≈10μF

DESIGN VALUES

Given A_V=10,h_{fe}=300, V_{CC}=10V,I_{CQ}=2mA and f=200Hz

R_1=180KΩ, R_2=39KΩ, R_E=470Ω, R_C=2.2KΩ, R_L=120Ω, R_S=0Ω, C_1=10µF, C_2=4.7µF, C_E=10µF.Use BC547

Emitter Bypass Capacitor, C_E

- Provides a Low reactance path to the amplified AC signal
- If it is absent, the amplified signal passing through RE will cause a voltage drop across it & hence output voltage and Gain of the Amplifier will reduce

Output Coupling Capacitor, C_2

- Couples the output signal to the Load or to the next stage of the Amplifier
- Blocks DC and allows only the amplified AC Signal

RC coupling scheme finds application in Audio small signal amplifiers which are used in Record players, Tape recorders, Public address system, Radio & TV receivers etc.,

PROCEDURE:

Measurement of gain and plotting of frequency response curve

1. The circuit connection is made as per the circuit diagram using Bread board with Rs being a Decade Resistance Box (DRB). Set Rs=0.
2. The RPS is adjusted to the value of Vcc needed.
3. The voltage level of AO is adjusted to be suitable value V_s. This level was maintained constant through out the experiment.
4. The frequency of the oscillator was varied over its working range in suitable steps. For each frequency setting, the corresponding value of output voltage Vo is noted.
5. The voltage gain Av in dB is given by 20 log (Vo/Vi) is computed for each frequency setting.
6. The frequency response curve is plotted on semi log graph sheet. The bandwidth is calculated from the graph by drawing the 3dB line.

   $BW = f_2 - f_1$ Hz

   Where BW is the bandwidth

   f_1 is the lower cutoff frequency.

   f_2 is the lower and upper cutoff frequency

Determination of gain band width product

1. Find the mid band gain or maximum gain (Av) from the table.
2. Find the band width BW= f2-f1
3. Gain bandwidth product =|Av|BW

TABULATION 1:

Input VOLTAGE (V_s) = _____ mV

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= ($20\log V_0/V_s$) dB

POST-LAB EXERCISE

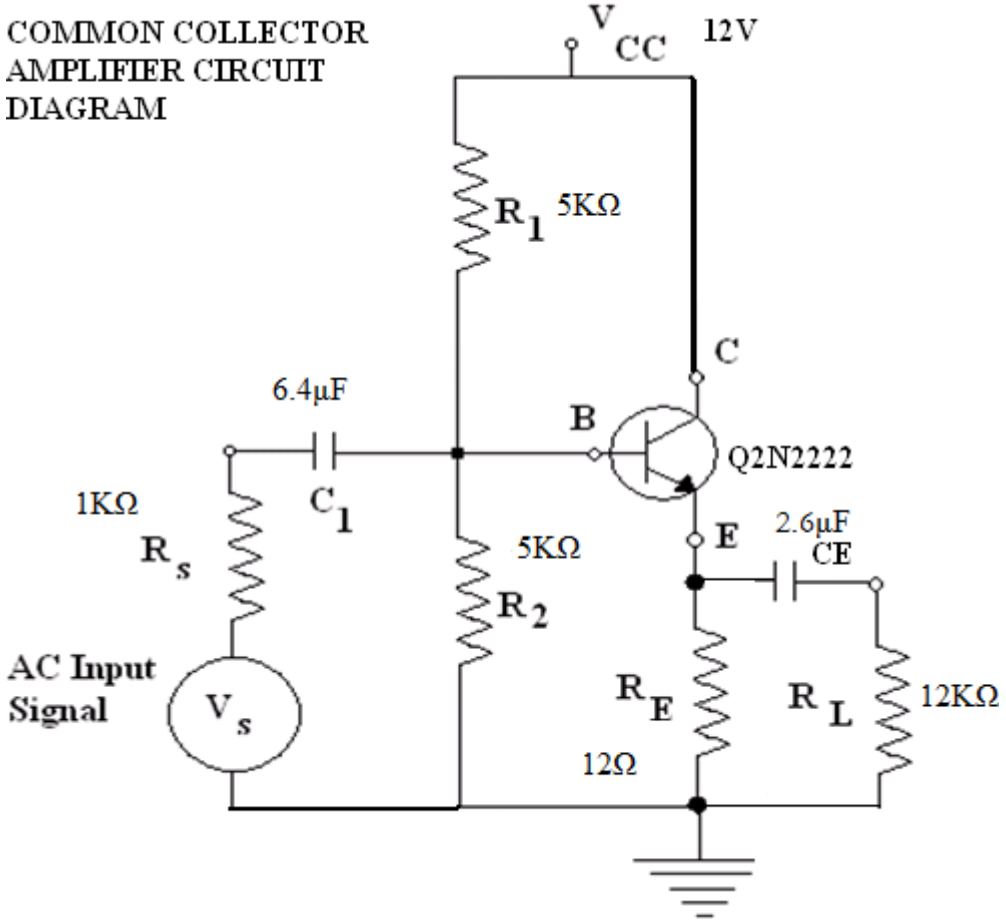
1. Why bandwidth is measured at 3 dB points?
2. What is Stability factor?
3. What is the expression of Stability factor S, S' & S'' of Self biased BJT circuit?
4. Why is Voltage divider bias frequently used?
5. Based on operating point, Is Voltage divider bias circuit, a class A or class B or class AB amplifier?

RESULT:

The BJT Common Emitter Amplifier using voltage divider bias (self-bias) with bypassed emitter resistor is designed & constructed and the frequency response of the amplifier is plotted.

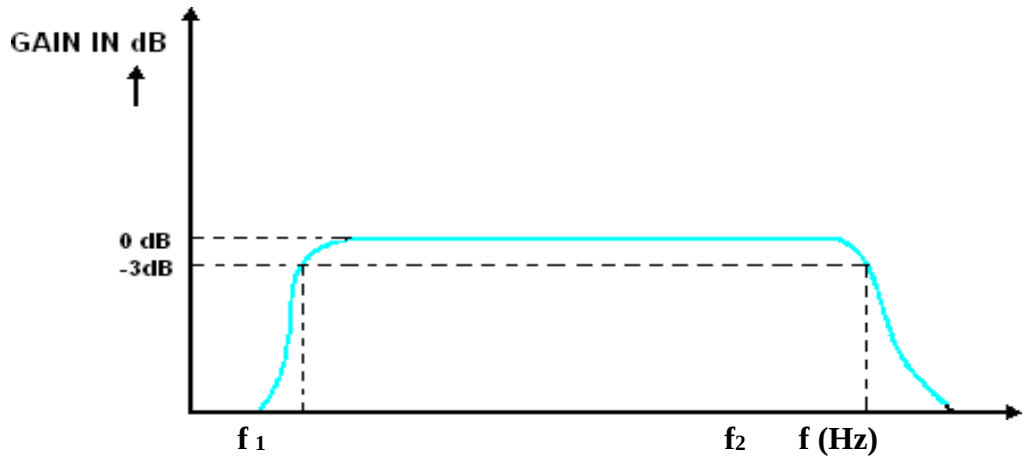
- Bandwidth of the bypassed CE amplifier = f_2-f_1= _____
- Mid band gain of bypassed CE amplifier=_____
- Gain bandwidth product bypassed CE amplifier =_____

CIRCUIT DIAGRAM:



MODEL GRAPH:

FREQUENCY RESPONSE CURVE



EXPT. NO: 2B FREQUENCY RESPONSE OF CC AMPLIFIER

AIM:

To Design a BJT Common Collector Amplifier (CC or Emitter follower) using voltage divider bias (self-bias) and to

- Measurement of gain
- Plot the frequency response & Determination of Gain Bandwidth Product

COMPONENTS REQUIRED:

S.NO	Name of the Component	Range	Quantity
1.	Transistor (Q2N2222 or BC107)		01
2.	Resister	5KΩ, 1KΩ, 12Ω,12KΩ	02 Each 01
3.	Capacitor	6.4μF,2.6μF	Each 01
4.	Function Generator		01
5.	RPS	(0-30) V	01
6.	CRO		01
7.	Bread Board		01
8.	Connecting Wires		

PRE-LAB EXERCISE

1. Why the common collector amplifier is also called as an emitter follower?
2. What is the need for coupling capacitors?
3. What will be the input &output impedance of common collector amplifier?
4. Write some applications of common collector amplifier?
5. What is the current amplification factor of common collector amplifier?

THEORY:

The common collector configuration has the base as the input terminal and the emitter as the output terminal with collector as the common terminal. It is otherwise called as the emitter follower as the output follows the input.

The voltage gain is lesser than one and the current gain $\gamma=1+\beta$ is very larger. Hence this amplifier can be used only for the current amplification and cannot be used as the voltage amplifier.

It is the only configuration where the input is reverse biased and the output is forward biased. Hence the input impedance which finds application in the impedance matching. Impedance matching is used to connect the circuit with the higher output impedance to the circuit with the lower input impedance.

DESIGN

Given $A_V=1$, $I_E=1mA$, $V_{CC}=12v$, $R_L=12K\ \Omega$, $\beta=h_{fe}=120$ & $f=200Hz$

Step 1

$V_{CEQ} = V_{CC}/2=12/2=6V$

Step 2

$V_{CC} = V_{CE} + V_E$

$V_E = V_{CC}-V_{CE}$

Therefore $V_E=6V$

DESIGN VALUES

Given A_V=10,h_{fe}=300, V_{CC}=10V,I_{CQ}=2mA and f=200Hz

R_1=180KΩ, R_2=39KΩ, R_E=470Ω, R_C=2.2KΩ, R_L=120Ω, R_S=0Ω, C_1=10µF, C_2= 4.7µF, C_E=10µF.Use BC547

Determination of gain band width product

1. Find the mid band gain or maximum gain (Av) from the table
2. Find the band width BW= f2-f1
3. Gain bandwidth product =|Av|BW

TABULATION:

Input Voltage (V_s or Vin) =_____V

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= 20log(V_0/V_s) dB

Step 3

$R_B = R_{B1} || R_{B2} = (R_1 || R_2)$

Choose $R_1 = R_2 = 10K\ \Omega$ Therefore $R_b = 10K\ \Omega$

Step4

Since $R_E = R_L \Rightarrow R_E = 12K\ \Omega$

Then $R_{eff} = R_E || R_L = 12K\ \Omega$

Step5

$(R_1 || R_2) = R_B = 32054.7\Omega$

$X_{C1} = (h_{ie} || R_B || h_{fe} R_E)/10 = (h_{ie} || R_B) = (1K || 32054.7)/10 = 96.97\Omega$

$C_1 = 1/2\pi f X_{C1} = 1/2\pi * 200 * 96.97 = 8.2\mu F \approx 10\mu F$ or $6.4\ \mu F$(available)

Step6

$X_E = R_E/10 = 470/10 = 47\Omega$

$C_E = 1/2\pi f X_E = 12\pi * 200 * 47 = 2.65\mu F$

PROCEDURE:

Measurement of gain and plotting of frequency response curve

1. The circuit connection is made as per the circuit diagram using Bread board with Rs being a Decade Resistance Box(DRB) . Set Rs=0.
2. The RPS is adjusted to the value of Vcc needed.
3. The voltage level of AO is adjusted to be suitable value V_s. This level was maintained constant throughout the experiment.
4. The frequency of the oscillator was varied over its working range in suitable steps. For each frequency setting, the corresponding value of output voltage Vo is noted.
5. The voltage gain Av in dB is given by 20 log (Vo/Vi) is computed for each frequency setting.
6. The frequency response curve is plotted on semi log graph sheet. The bandwidth is calculated from the graph by drawing the 3dB line.
   Bandwidth= BW= f_2-f_1, where f_1 & $f_2$is the lower & upper cutoff frequency.

POST-LAB EXERCISE

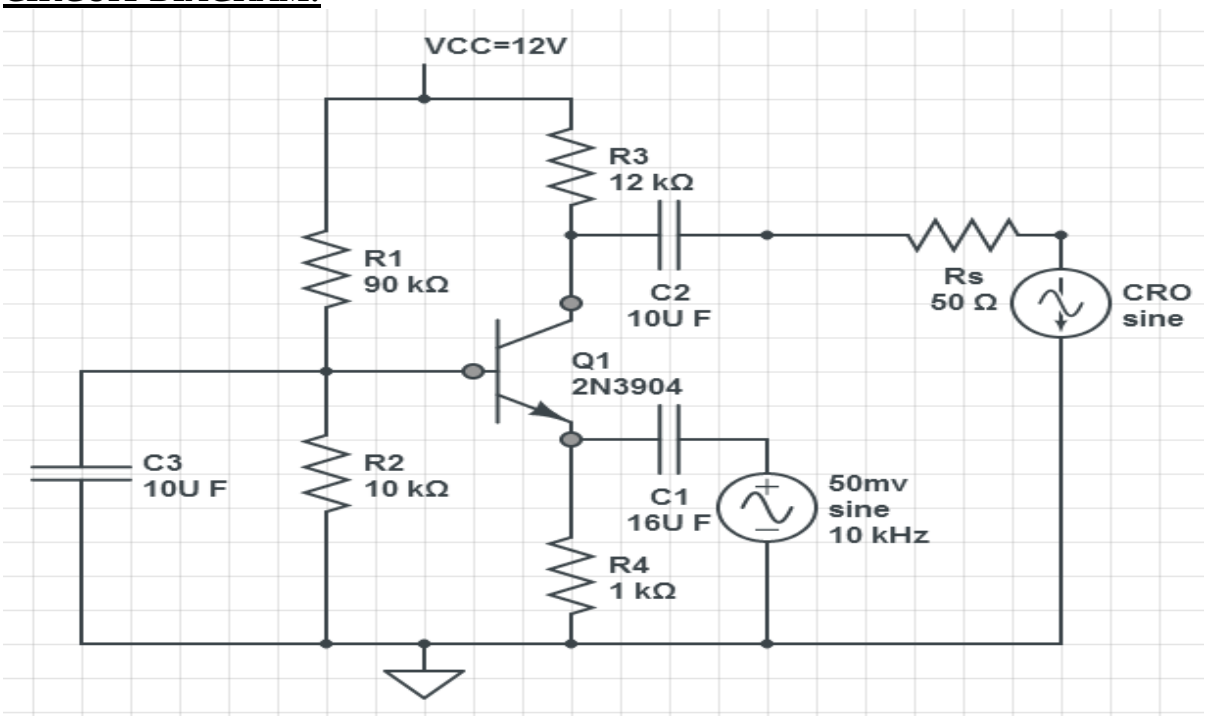
1. What do you mean by 'volt equivalent of temperature'?
2. What is the voltage gain of the CC amplifier?
3. Why the circuit is referred to an 'emitter follower'?
4. Give one application for emitter follower.
5. What are the three most important characteristics of an emitter follower?

RESULT:

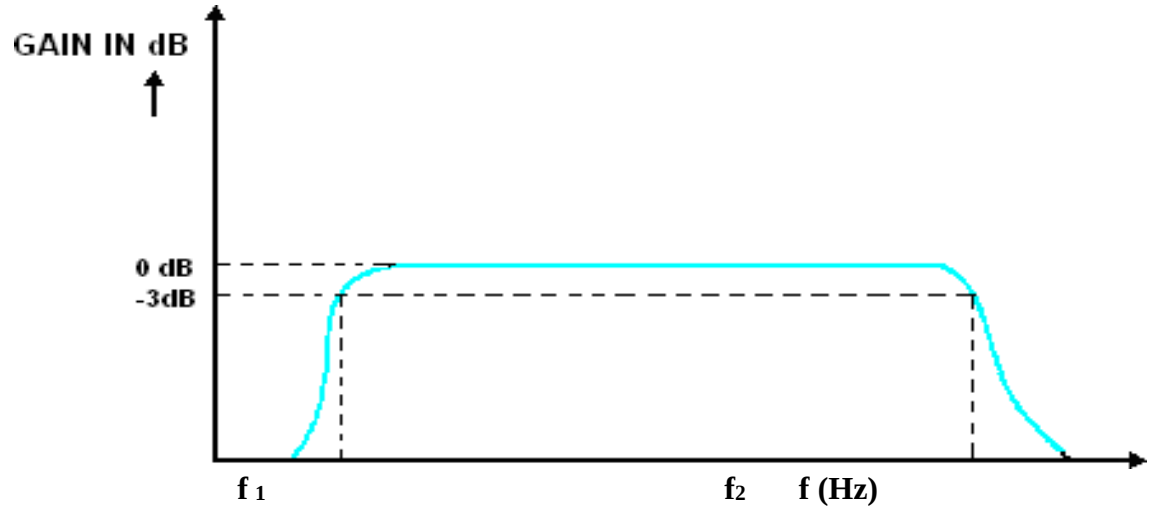
The BJT Common Collector Amplifier (Emitter follower) using voltage divider bias (self bias) designed & constructed and the frequency response of the amplifier is plotted.

- Bandwidth of the amplifier BW= f_2-f_1= _____
- Mid band gain A_v=_____
- Gain bandwidth product=_____

CIRCUIT DIAGRAM:



MODEL GRAPH:



EXPT. NO: 2C FREQUENCY RESPONSE OF CB AMPLIFIER

AIM:

To design a CB amplifier using voltage divider bias and to study the frequency response characteristics of the amplifier.

COMPONENTS REQUIRED:

S.No	Item Name	Range	Quantity
1	BJT	BC547 or BC107	1
2	Resistors	90k,10k,12k,1k,50	1 (each)
3	Capacitors	10µF, 16µF	1(each)
4	Function Generator/AFO	(0-3)MHz	1
5	CRO	(0-20)MHz	1
6	RPS (Regulated Power Supply)	(0-30)V	1
7	Bread Board and Connecting Wires		

Pre-Lab Exercise

1. What do you mean by 'volt equivalent of temperature'?
2. What is the voltage gain of the CB amplifier?
3. Give the technical specifications of BC107.
4. Write the hybrid parameters of CB amplifier.
5. Define miller effect.

THEORY:

A common Base amplifier is also known as an emitter follower or voltage follower. In this circuit the emitter terminal of the transistor serves as the input, the collector as the output and the base is common to both. The common base amplifier has large bandwidth for voltage gain. The Circuit has large voltage gain and low input impedance. typically used as a current buffer or voltage amplifier This arrangement is not very common in low-frequency circuits, where it is usually employed for amplifiers that require an unusually low input impedance, for example to act as preamplifier for moving-coil microphones. However, it is popular in high-frequency amplifiers, for example for VHF and UHF, because its input capacitance does not suffer from the Miller effect, which degrades the bandwidth of the common emitter configuration, and because of the relatively high isolation between the input and output. This high isolation means that there is little feedback from the output back to the input, leading to high stability.

DESIGN:

V_{cc} = 12V, Vin= 10mV@ 10KHz, R_S = 50Ω,Ie=0.51mA, R_{in} = 50 Ω

$$I_E = \frac{V_T}{R_{in}} = \frac{0.026V}{50\Omega} = 0.52mA, I_B = 5.1\mu A, I_c = .51mA$$

$$Let\ emitter\ voltage\ drop\ V_{RE} = 0.5V, and\ I_E = 0.52mA, R_E \approx 1000\Omega$$

$$V_{ceq} = 6V, R_c = \frac{V_{cc} - V_{ceq}}{I_c} = \frac{12 - 6}{0.5mA} = 12k\Omega$$

$$V_{BB} = V_E + V_{be} = 0.5V + 0.7V = 1.2V$$

$$R_{BB} = 0.1 * (1 + 100) * 1000 = 10.1k\Omega$$

$$R_{BB} = R_1 \parallel R_2$$

$$V_B = V_{cc}\left(\frac{R_2}{R_1 + R_2}\right)$$

R_2=0.1*h_{FE}*R_E=10kΩ.

R_1=$V_{CC}R_2$-

V_BR_2/V_B=90KΩ

Design of coupling capacitor:

$$R_{in} = 50\Omega$$

$$\tau_{cc1} = (R_s + R_{in}) * C_{c1} = (50 + 50) * 10\mu F = 1mSec$$

$$Freq_{cc1} = \frac{1}{2\pi\tau_{cc1}} = 100Hz \qquad C_{c1} = \frac{1}{2\pi(R_s + R_{in})Freq_{cc1}} = 16\mu F$$

TABULATION :

Input Voltage (V_s or Vin) =_____V

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= 20log(V_0/V_s) dB

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The regulated power supply is turned on and its voltage level is adjusted to the value of V_{CC}
3. Switch on the AFO and adjust the voltage to V_i.
4. The frequency of the oscillator was varied over its working range in suitable steps.
5. Note down the value of V_o from CRO for each frequency setting.
6. Calculate the voltage gain.
7. Plot the frequency response curve and calculate Bandwidth from graph.

Post-Lab Exercise

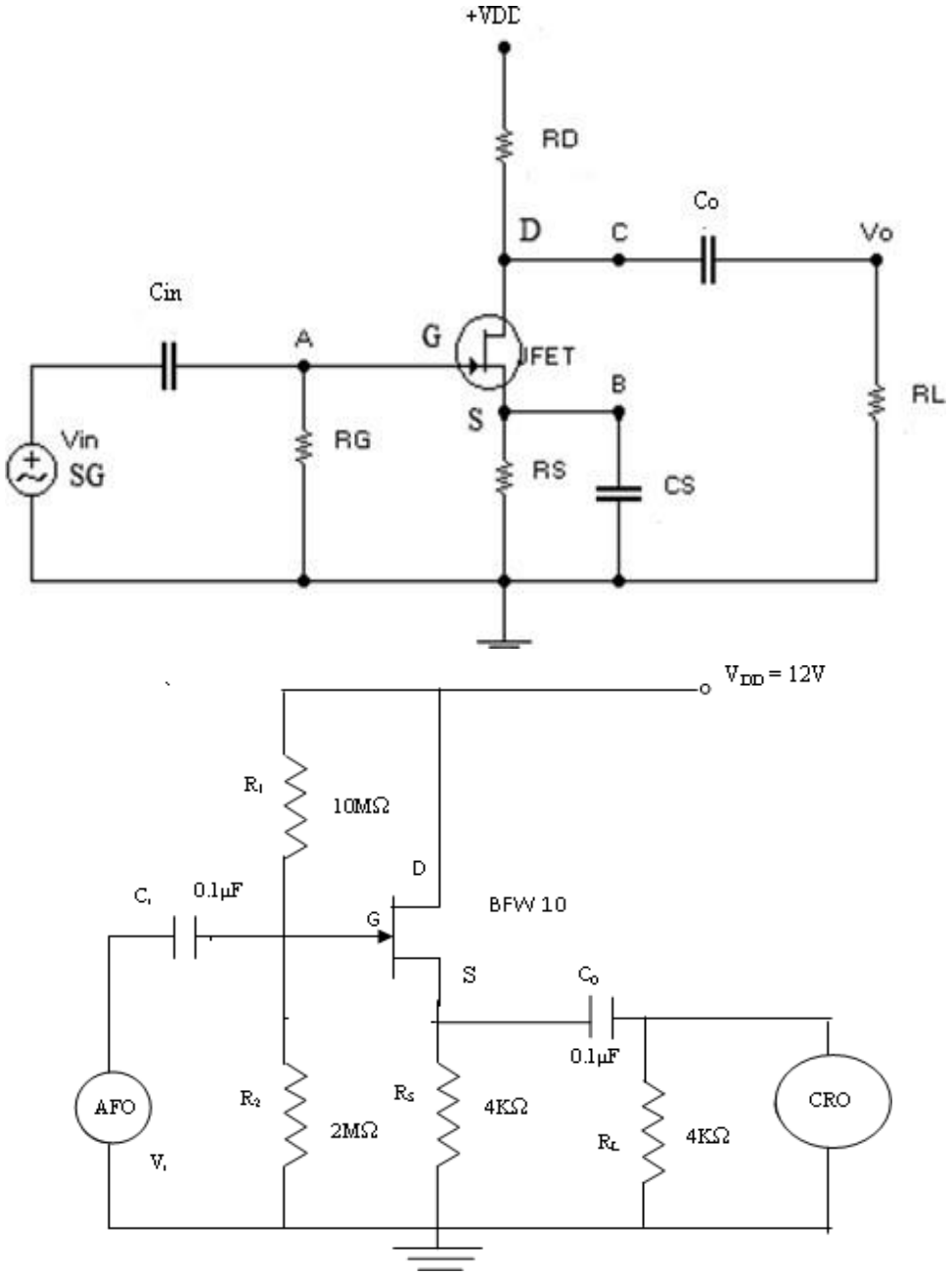
1. Give one application for CB amplifier.
2. What are the three most important characteristics of a Common Base amplifier?
3. List the advantages of CB amplifier.
4. List the disadvantages of CB amplifier.
5. Define base width modulation.

RESULT:

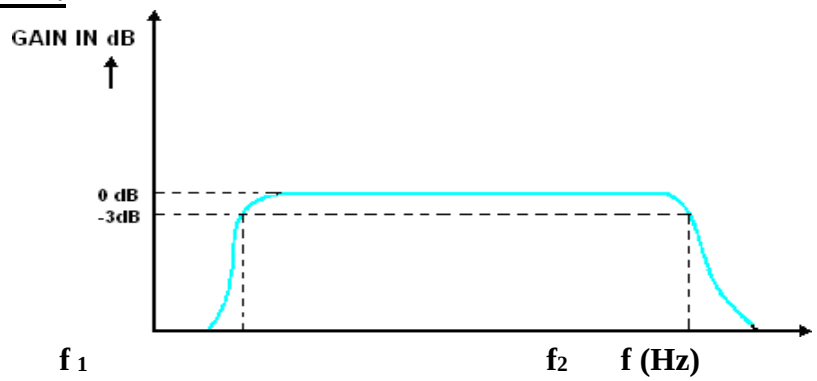
The BJT Common Base Amplifier (CB) using voltage divider bias designed & constructed and the frequency response of the amplifier is plotted.

- Bandwidth of the amplifier BW= f_2-f_1= _____
- Mid band gain A_v=_____
- Gain bandwidth product=_____

CIRCUIT DIAGRAM:



MODEL GRAPH:



EXPT. NO: 2D FREQUENCY RESPONSE OF CS AMPLIFIER

AIM:

To construct a Common Source (CS) Amplifier and to determine its frequency response curve and to obtain its band width.

COMPONENTS REQUIRED:

S.No	Item Name	Range/ Specification	Quantity
1	FET	BFW10	1
2	Resistors	10MΩ,1MΩ,2MΩ 4KΩ	1(each) 2
3	Capacitors	0.1µF	3
4	Function Generator/AFO	(0-3)MHz	1
5	CRO	(0-20)MHz	1
6	RPS (Regulated Power Supply)	(0-30)V	1
7	Bread Board and Connecting Wires		

Pre-Lab Exercise

1. What is common source amplifier?
2. What are the applications of common source amplifier?
3. What is the other name of source follower?
4. What do you say about the input and output impedance of source follower?
5. What are the advantages of bootstrapping?

THEORY:

There are three basic types of FET amplifier or FET transistor namely common source amplifier, common gate amplifier and source follower amplifier.

The common-source (CS) amplifier may be viewed as a transconductance amplifier or as a voltage amplifier.

i) As a transconductance amplifier, the input voltage is seen as modulating the current going to the load.

ii) As a voltage amplifier, input voltage modulates the amount of current flowing through the FET, changing the voltage across the output resistance according to Ohm's law.

However, the FET device's output resistance typically is not high enough for a reasonable transconductance amplifier (ideally infinite), nor low enough for a decent voltage amplifier (ideally zero). Another major drawback is the amplifier's limited high-frequency response. Therefore, in practice the output often is routed through either a voltage follower (common-drain or CD stage), or a current follower (common-gate or CG stage), to obtain more favorable output and frequency characteristics.

DESIGN:

Assume A_V=0.9622, I_{DSS}=1mA,V_P=-4V,V_{DD}=30V,f_L=300Hz

Step1

$I_D=I_{DSS}/2= 10/2 =5mA$

Step2

$I_D=I_{DSS}\ \{ 1-(V_{GS}/V_P)\}^2$

$5 =10(1+ (V_{GS}/4))^2$

On solving, $V_{GS}= -1.17V$

Step3

$g_m = g_{m0} (1-(V_{GS}/V_P))$

$g_{m0}=2I_{DSS}/|V_P|=2*(10*10^{-3})/4=5*10^{-3}\Omega^{-1}$

Hence $g_m=5*10^{-3}(1-(1.17/4)) =3.537*10^{-3}\Omega^{-1}$

Step4

$A_v= ((g_m R_S)/(1+g_m R_S))$

Substituting the values of A_v and g_m and solving for R_S in the above equation, we get,

$R_S=7.02K\Omega \approx 7.2K\Omega$

Step5

Let $R_1=1M\Omega$ and $R_2=1M\Omega$

Step6

$X_{Ci}= (R_1||R_2) /10 = (1M||1M)/10 =50K\Omega$

$C_i=1/ \ 2\pi f X_{Ci} =1/2\pi*300*50K\Omega \ =0.01\mu F$

Step7

$X_{Co}= R_E/10 \ =7.2K/10=0.72K\Omega$

$C_o= 1 /2\pi f X_{Co}=1/2\pi*300*0.72K=0.73\mu F \approx 1\mu F$

TABULATION :

Input Voltage (V_s or Vin) = _____ V

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= 20log(V_o/V_s) dB

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The regulated power supply is turned on and its voltage level is adjusted to the value of V_{CC} needed.
3. The AFO was switched on and voltage level adjusted to be a suitable value V_S. This level was maintained constant throughout the Experiments.
4. The frequency of the oscillator was varied over its working range in suitable steps.
5. For each frequency setting, the corresponding value of output voltage V_O is noted.
6. The voltage gain A_V,given by 20 log (Vo / Vi) is computed for each frequency setting.

The frequency response curve is plotted in a semi log graph sheet and BW is calculated

Post-Lab Exercise

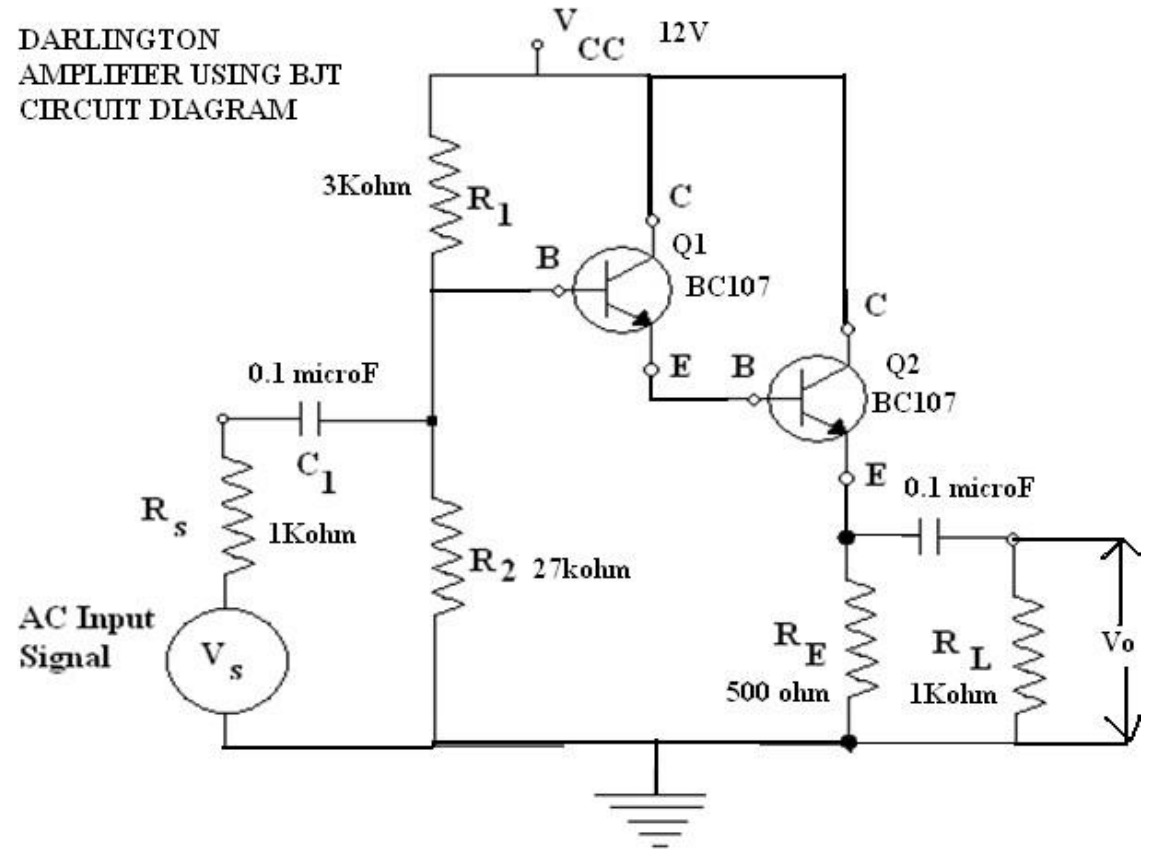
1. What are the techniques of improving Input Impedance
2. Give the expression for Input Impedance of Bootstrapped source follower
3. How the above bootstrapped circuits provide a good impedance matching?
4. What is the difference between source follower & emitter follower?
5. Define transconductance.

RESULT:

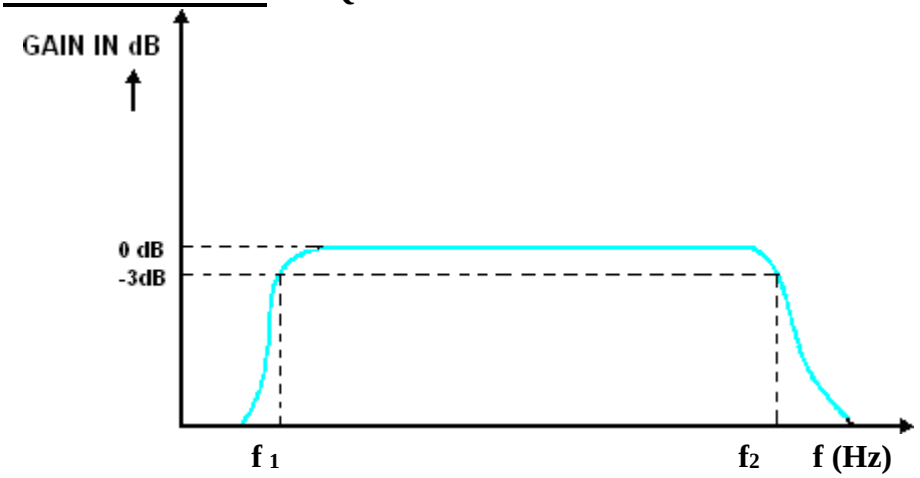
Thus the common source (CS) amplifier circuit is constructed & frequency response is plotted.

- Bandwidth of the amplifier BW= f2-f1= _____
- Mid band gain A_v =_____
- Gain bandwidth product=_____

CIRCUIT DIAGRAM:



MODEL GRAPH: FREQUENCY RESPONSE CURVE



EXPT.NO: 3 **DARLINGTON AMPLIFIER**
Date:
AIM:

To construct a Darlington current amplifier circuit using BJT and to
1. Measurement of gain and input resistance.
2. Comparison with calculated values.
3. Plot the frequency response & Determination of Gain Bandwidth Product

COMPONENTS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC 107	1
2.	Resistor	1kΩ,3kΩ,27KΩ,560Ω	2,1,1,1
3.	Capacitor	0.1μF	2
4.	Function Generator	(0-3)MHz	1
5.	CRO	30MHz	1
6.	Regulated power supply	(0-30)V	1
7.	Bread Board		1

Pre-Lab Exercise

1. What is meant by Darlington pair?
2. How many transistors are used to construct a Darlington amplifier circuit?
3. What is the advantage of Darlington amplifier circuit?
4. Write some applications of Darlington amplifier?
5. What is the voltage gain of Darlington amplifier?

THEORY:

In Darlington connection of transistors, emitter of the first transistor is directly connected to the base of the second transistor .Because of direct coupling dc output current of the first stage is $(1+h_{fe})I_{b1}$.If Darlington connection for n transitor is considered, then due to direct coupling the dc output current foe last stage is $(1+h_{fe})^{n}$ times I_{b1} .Due to very large amplification factor even two stage Darlington connection has large output current and output stage may have to be a power stage. As the power amplifiers are not used in the amplifier circuits it is not possible to use more than two transistors in the Darlington connection.

In Darlington transistor connection, the leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high, which is not desired.

TABULATION :

Input Voltage (V_s or Vin) =_____V

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= $20\log(V_0/V_s)$ dB

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Set Vi =50 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 Hz to 1M Hz in regular steps and note down the corresponding output voltage.
4. Plot the graph; Gain (dB) vs Frequency(Hz).
5. Calculate the bandwidth & Gain Bandwidth Product from the graph.

Post-Lab Exercise

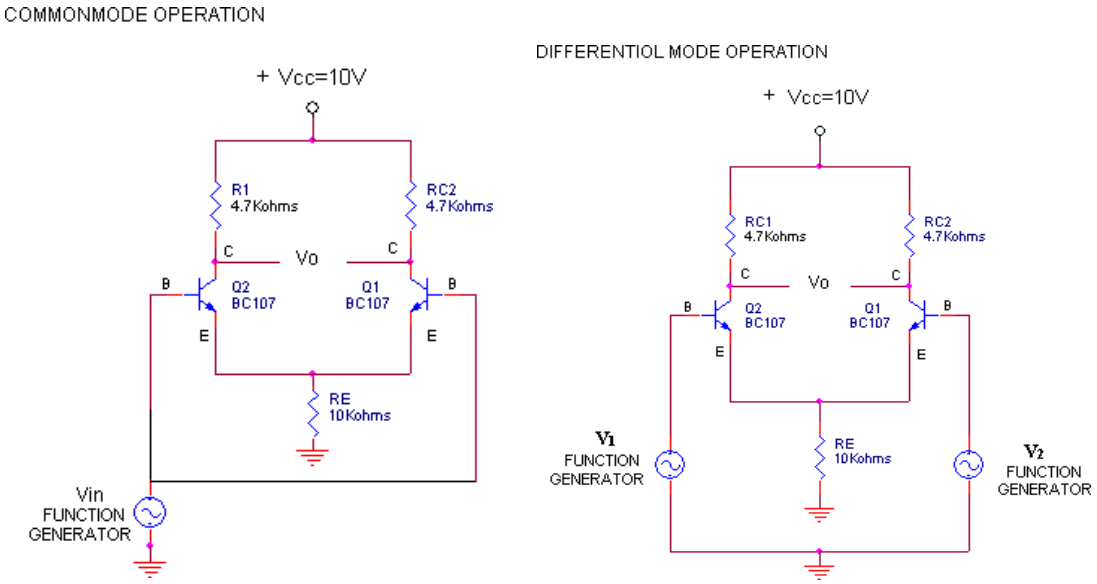
1. Why the input impedance is higher than that of emitter follower?
2. Define stabilization factor.
3. How do you determine the lower and upper cutoff frequencies of the amplifier?
4. What is cascade amplifier?
5. What are the advantages of Darlington amplifier?

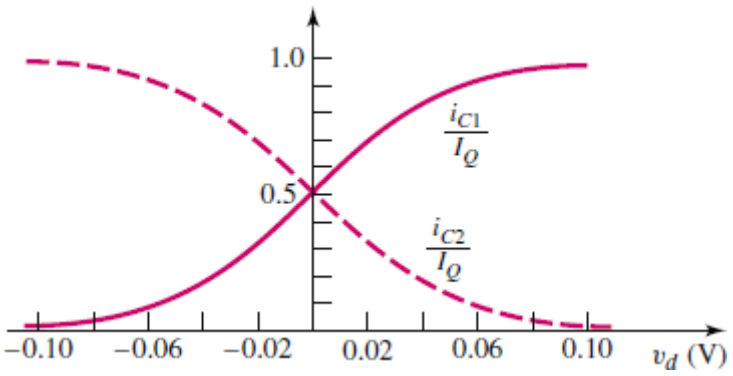
RESULT:

The Darlington current amplifier circuit using BJT constructed and the frequency response of the amplifier is plotted.

- Bandwidth of the amplifier BW= f2-f1= _____
- Mid band gain A_v =_____
- Gain bandwidth product=_____

CIRCUIT DIAGRAM:





Normalized dc transfer characteristics for BJT differential amplifier

EXPT.NO: 4A DIFFERENTIAL AMPLIFIERS - TRANSFER CHARACTERISTIC

AIM:

To construct a differential amplifier and to determine Transfer Characteristics.

COMPONENTS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC 107	2
2.	Resistor	4.7kΩ,10kΩ,	2,1
3.	Function Generator	(0-3)MHz	2
4.	CRO	30MHz	1
5.	Regulated power supply	(0-30)V	1
6.	Bread Board		1

Post-Lab Exercise

1. What is a differential amplifier?
2. What is common mode and differential mode inputs in a differential amplifier?
3. What are the assumptions made while designing a differential amplifier?
4. What is meant by balanced output differential amplifier?
5. List some applications of differential amplifier.

THEORY:

A differential amplifier multiplies the difference between two inputs by a constant factor called differential gain. A differential amplifier rejects noise common to both inputs. This circuit has a unique topology: two inputs and two outputs. Differential amps finds use in control of motors or servos, Signal amplification, in operational amplifiers, as Phase inverter.

The differential amplifier is a basic stage of an integrated operational amplifier. It is used to amplify the difference between 2 signals. It has excellent stability, high versatility and immunity to noise. In a practical differential amplifier, the output depends not only upon the difference of the 2 signals but also depends upon the common mode signal.

Transistor Q1 and Q2 have matched characteristics. The values of R_{C1} and R_{C2} are equal. R_{e1} and R_{e2} are also equal and this differential amplifier is called emitter coupled differential amplifier. The output is taken between the two output terminals.

For the differential mode operation the input is taken from two different sources and the common mode operation the applied signals are taken from the same source .

We can perform a general analysis of the differential-pair configuration by using the exponential relationship between collector current and B–E voltage. To begin, we know that

$$i_{C1} = I_S e^{v_{BE1}/V_T}$$

and

$$i_{C2} = I_S e^{v_{BE2}/V_T}$$

TABULATION:

Common Mode				
S.No	Input Voltage		Output Voltage	
	V1	V2	Theoretical Value	Practical Value

Difference Mode				
S.No	Input Voltage		Output Voltage	
	V1	V2	Theoretical Value	Practical Value

We assume $Q1$ and $Q2$ are matched and are operating at the same temperature, so the coefficient I_S is the same in each expression.
Neglecting base currents and assuming IQ is an ideal constant-current source, we have

$$I_Q = i_{C1} + i_{C2}$$

where i_{C1} and i_{C2} are the total instantaneous currents, which may include the signal currents. We then have

$$I_Q = I_S[e^{v_{BE1}/V_T} + e^{v_{BE2}/V_T}]$$

Taking the ratios of i_{C1} to I_Q and i_{C2} to I_Q, we obtain

$$\frac{i_{C1}}{I_Q} = \frac{1}{1 + e^{(v_{BE2} - v_{BE1})/V_T}}$$

and

$$\frac{i_{C2}}{I_Q} = \frac{1}{1 + e^{-(v_{BE2} - v_{BE1})/V_T}}$$

The above equations describe the basic current–voltage characteristics of the differential amplifier. If the differential-mode input voltage is zero, then the current IQ splits evenly between i_{C1} and I_{C2}, as we discussed. However, when a differential-mode signal v_d is applied, a difference occurs between i_{C1} and i_{C2} which in turn causes a change in the collector terminal voltage. This is the fundamental operation of the diff-amp. If a common-mode signal $v_{CM} = v_{B1} = v_{B2}$ is applied, the bias current I_Q still splits evenly between the two transistors.

The figure shows the normalized plot of the dc transfer characteristics for the differential amplifier. We can make two basic observations. First, the gain of the differential amplifier is proportional to the slopes of the transfer curves about the point $v_d = 0$. In order to maintain a linear amplifier, the excursion of v_d about zero must be kept small. Second, as the magnitude of

v_d becomes sufficiently large, essentially all of current I_Q goes to one transistor, and the second transistor effectively turns off.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. To determine the Transfer Characteristics, we set differentinput signal values.
3. Then measure output current across the collector terminals.

Post-Lab Exercise

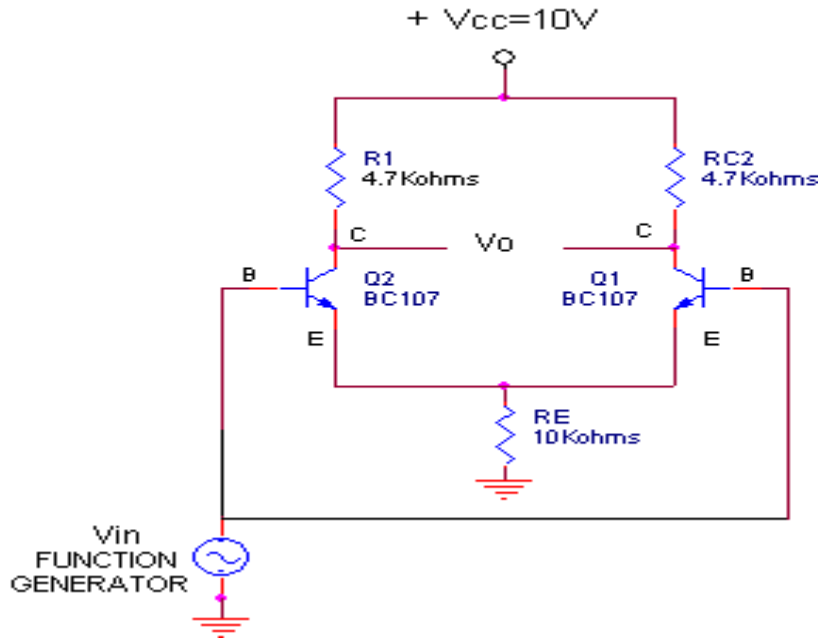
1. Define common mode & differential mode gain.
2. What is ideal value of A_c, A_d?
3. What is transconductance in differential amplifier?
4. Compare common mode gain and differential mode gain.
5. What is common mode rejection ratio?

RESULT:

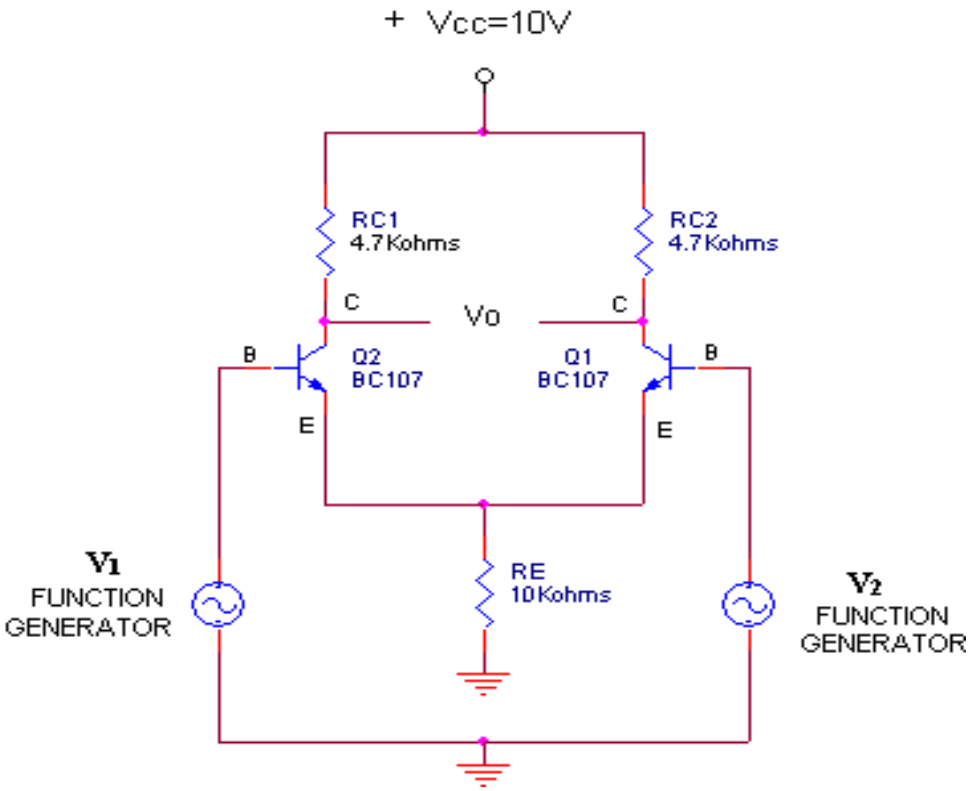
Thus the differential amplifier using BJT is constructed and its transfer characteristic is obtained.

CIRCUIT DIAGRAM:

COMMONMODE OPERATION



DIFFERENTIOL MODE OPERATION



EXPT.NO: 4B DIFFERENTIAL AMPLIFIERS-CMRR MEASUREMENT

AIM:

To construct a differential amplifier and to determine Common Mode Rejection Ratio (CMRR).

COMPONENTS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC 107	2
2.	Resistor	4.7kΩ,10kΩ,	2,1
3.	Function Generator	(0-3)MHz	2
4.	CRO	30MHz	1
5.	Regulated power supply	(0-30)V	1
6.	Bread Board		1

Pre-Lab Exercise

1. What is a differential amplifier?
2. Why CMRR should be very high or low? Justify.
3. For a given value of differential gain, does a higher CMRR result in higher or lower common mode gain?
4. How do you express CMRR in dB?
5. What are the assumptions made while designing a differential amplifier?

THEORY:

A differential amplifier multiplies the difference between two inputs by a constant factor called differential gain. A differential amplifier rejects noise common to both inputs. This circuit has a unique topology: two inputs and two outputs. Differential amps finds use in control of motors or servos, Signal amplification, in operational amplifiers, as Phase inverter.

The differential amplifier is a basic stage of an integrated operational amplifier. It is used to amplify the difference between 2 signals. It has excellent stability, high versatility and immunity to noise. In a practical differential amplifier, the output depends not only upon the difference of the 2 signals but also depends upon the common mode signal.

Transistor Q1 and Q2 have matched characteristics. The values of R_{C1} and R_{C2} are equal. R_{e1} and R_{e2} are also equal and this differential amplifier is called emitter coupled differential amplifier. The output is taken between the two output terminals.

For the differential mode operation the input is taken from two different sources and the common mode operation the applied signals are taken from the same source .

Common Mode Rejection Ratio (CMRR) is an important parameter of the differential amplifier. CMRR is defined as the ratio of the differential mode gain, A_d to the common mode gain, A_c.

$$CMRR = A_d / A_c$$

In ideal cases, the value of CMRR is very high.

FORMULA:

Common mode Gain $(A_c) = V_0 / V_{IN}$

Differential mode Gain $(A_d) = V_0 / V_{IN}$ Where $V_{IN} = V_1 - V_2$

Common Mode Rejection Ratio (CMRR) = A_d/A_c

TABULATION:

Common Mode

V_1 Volts	V_2 Volts	V_0 Volts	Gain $A_c = V_0 / V_1 = V_0 / V_2$

Differential Mode

V_1 Volts	V_2 Volts	V_0 Volts	Gain $A_d = V_0 / V_{in}$ $V_{in} (V_1 - V_2)$

CALCULATION: CMRR = A_d / A_C

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. To determine the common mode gain, we set input signal with voltage V_{in}=2Vand determine V_o at the collector terminals. Calculate common mode gain, $A_c=V_o/V_{in}$.
3. To determine the differential mode gain, we set input signals with voltages V_1 and V_2. Compute $V_{in}=V_1-V_2$ and find V_o at the collector terminals. Calculate differential mode gain, $A_d=V_o/V_{in}$.
4. Calculate the CMRR=A_d/A_c.
5. Measure the dc collector current for the individual transistors.

Post-Lab Exercise

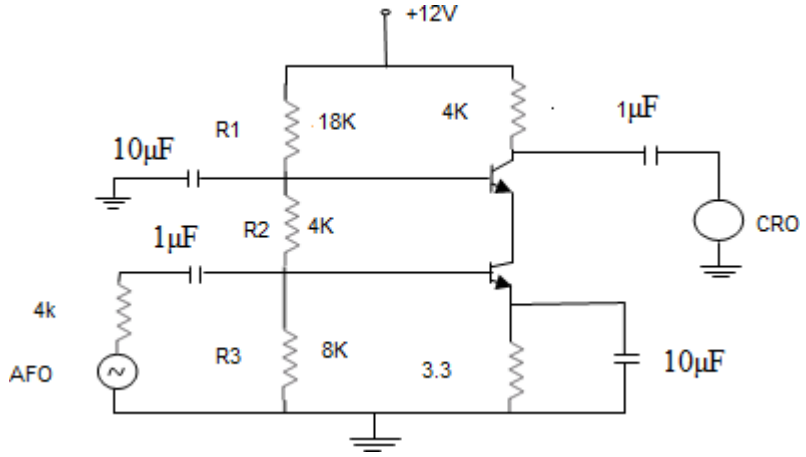
1. What is meant by balanced output differential amplifier?
2. How to improve CMRR?
3. What is CMRR interms of 'h' parameters?
4. What is ideal value of A_c, A_d & CMRR?
5. What is transconductance in differential amplifier?

RESULT:

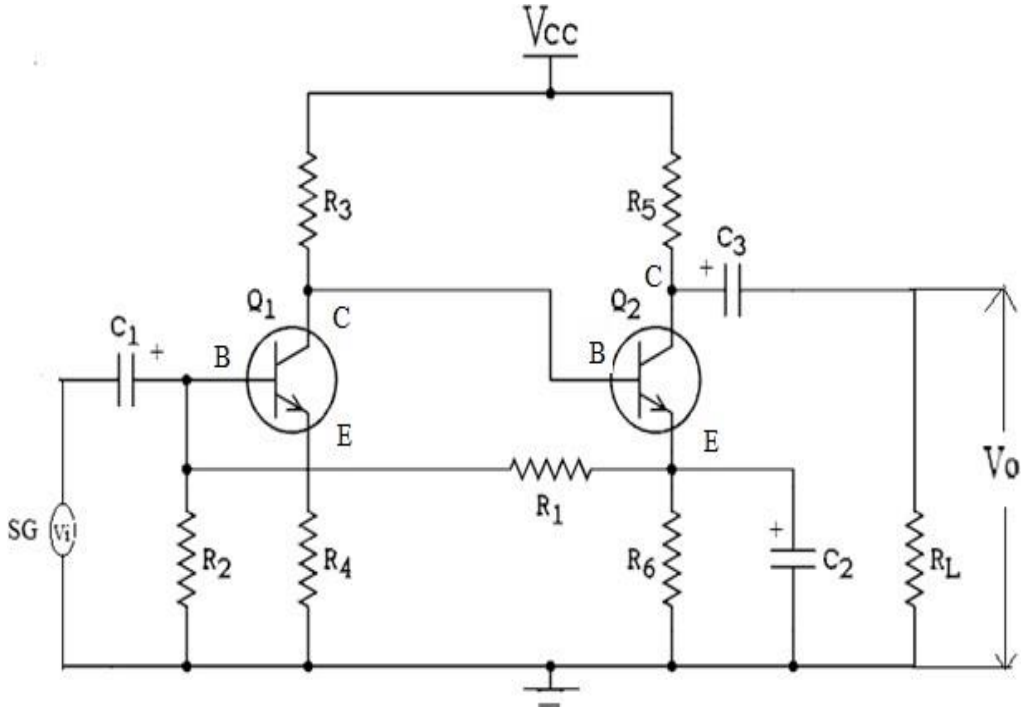
Thus the differential amplifier using BJT is constructed and its CMRR is calculated.
The CMRR calculated value is_____

CIRCUIT DIAGRAM: Cascode Amplifier

Let $C_i = 1\mu F$ *and* $C_0 = 3\mu F$



CIRCUIT DIAGRAM: Cascade Amplifier



EXPT.NO:5 CASCODE / CASCADE AMPLIFIER

AIM:

To construct and verify the performance of two stage Cascode/ Cascade amplifier and to determine the frequency response and Bandwidth.

COMPONENTS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC-547	2
2.	Capacitors (designed values)	1µF, 10µF	2
3.	Resistors (designed values)	18 KΩ, 8KΩ, 3.3KΩ 2KΩ, 4 KΩ(3No)	Each 1
4.	Function Generator	0 -1MHZ	1
5.	Cathode Ray Oscilloscope	20MHZ	1
6.	Regulated Power Supply	0-30V,1Amp	1

Pre-Lab Exercise

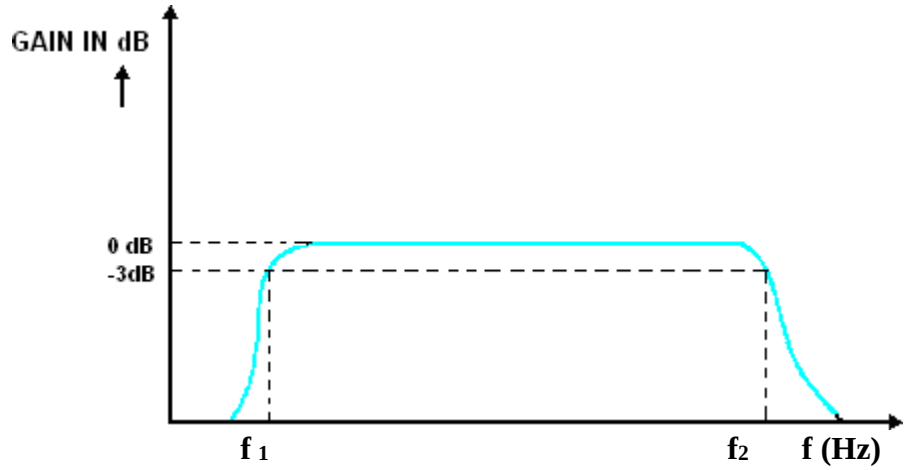
1. What is Cascode amplifier?
2. What is Cascade amplifier?
3. What is the difference between cascade and cascade amplifier?
4. What is FET and MOSFET?
5. Compare BJT and FET.

THEORY:

Cascode amplifier is a two-stage circuit consisting of a transconductance amplifier followed by a buffer amplifier. The word "cascode" was originated from the phrase "cascade to cathode". This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate etc. The reason behind the increase in bandwidth is the reduction of Miller effect. Cascode amplifier is generally constructed using FET (field effect transistor) or BJT (bipolar junction transistor). One stage will be usually wired in common source/common emitter mode and the other stage will be wired in common base/ common emitter mode.

A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker.

MODEL GRAPH:



TABULATION:

Input Voltage (V_s or Vin) = _____V

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= 20log(V_0/V_{in}) dB

PROCEDURE:

1. The circuit connections are made as per the circuit diagram.
2. The regulated power supply is turned on and its voltage level is adjusted to the value of V_{CC} needed.
3. The A/O was switched on and voltage level adjusted to be a suitable value V_S. This level was maintained constant throughout the Experiments.
4. The frequency of the oscillator was varied over its working range in suitable steps.
5. For each frequency setting, the corresponding value of output voltage V_O is noted.
6. The voltage gain A_V, given by 20 log (Vo / Vi) is computed for each frequency setting.
7. The frequency response curve is plotted in a semi log graph sheet and BW is calculated.

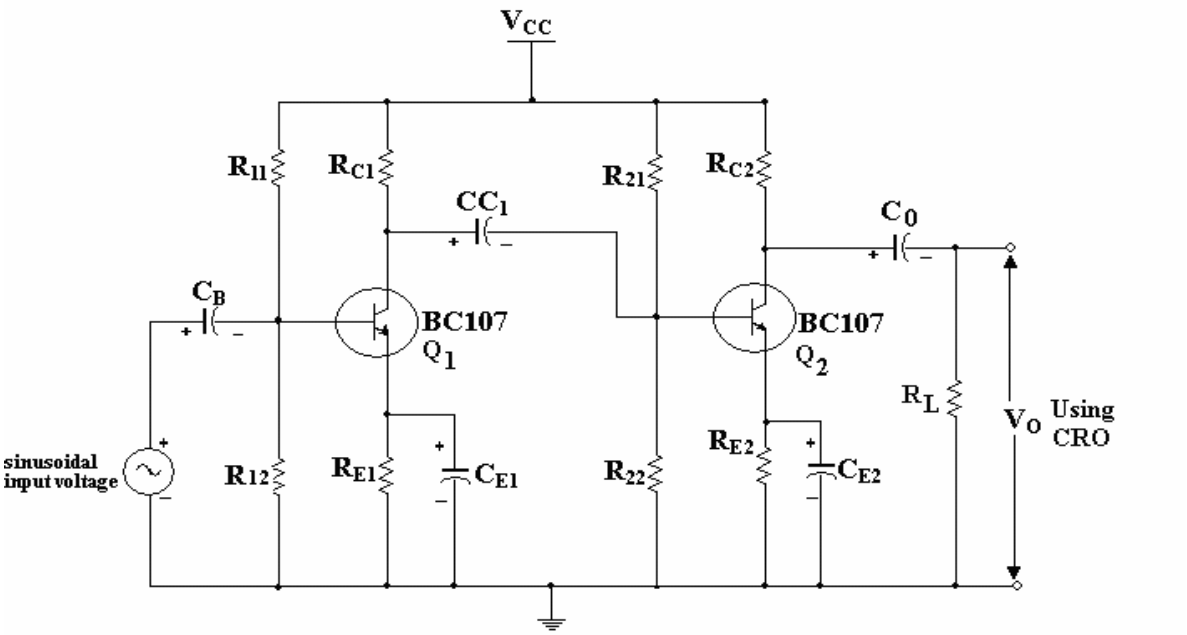
Post-Lab Exercise

1. Give an application Cascode amplifier.
2. What are the applications Cascade amplifiers?
3. What will be the effect on band width of cascade amplifier?
4. How do you determine the lower and upper cutoff frequencies of the cascode amplifier?
5. List the advantages and disadvantages of cascade amplifier.

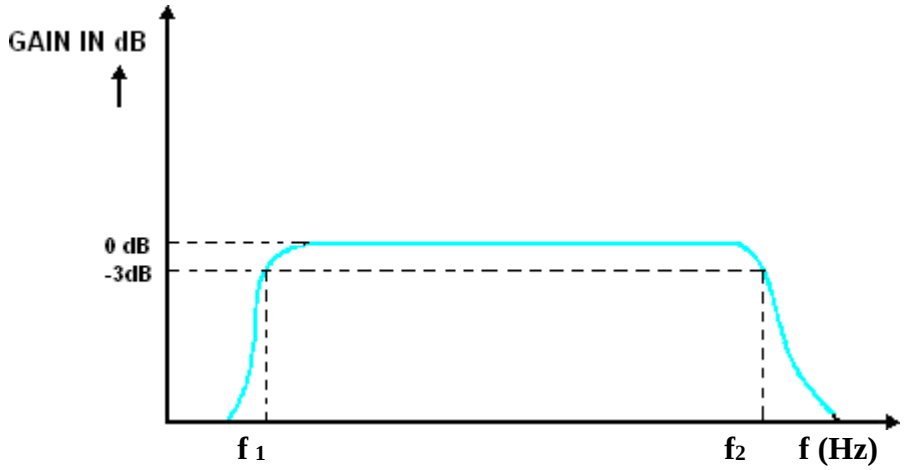
RESULT:

Thus, the frequency response of the Cascode amplifier using BJT is constructed and the Bandwidth is determined.

CIRCUIT DIAGRAM:



MODEL GRAPH:



EXPT.NO:6 DETERMINATION OF BANDWIDTH OF SINGLE STAGE AND MULTISTAGE AMPLIFIERS

AIM:

To design, construct and verify the performance of two stage RC Coupled (Cascaded) multistage amplifier and to determine the frequency response and Bandwidth.

COMPONENTS REQUIRED:

S.No.	Name	Range	Quantity
1.	Transistor	BC-107	2
2.	Capacitors(designed values)	0.1µF, 0.01µF, 1µF, 10µF	5
3.	Resistors (designed values)	56 K, 9.8 K, 1.2 K, 4.8 K	9
4.	Function Generator	0 -1MHZ	1
5.	Cathode Ray Oscilloscope	20MHZ	1
6.	Regulated Power Supply	0-30V,1Amp	1

Pre-Lab Exercise

1. Why RC coupled amplifiers widely used as voltage amplifiers?
2. What is multistage amplifier?
3. What are the advantages of multistage amplifier?
4. What are the different types of coupling?
5. What is cascade amplifier?

THEORY:

When two amplifiers are connected, in such a way that the output signal of first serves as the input signal of second, the amplifiers are said to be connected in cascade. Cascading is done to increase the gain of the amplifier. Each stage of the cascade amplifier should be biased at its designed level. It is possible to design a multistage cascade in which each stage is separately biased and coupled to the adjacent stage using blocking or coupling capacitors. In this circuit each of the two capacitors c1 & c2 isolate the separate bias network by acting as open circuits to dc and allow only signals of sufficient high frequency to pass through cascade.

DESIGN:

Given Data: hfe1 = hfe2= 200, RL =10Ω, IE1 = IE2 =1mA, s1 = s2 =8, f=100HZ, VCC=12v

1) For fixing the optimum operating point Q, mark the middle of the d.c load line and the corresponding VCE (Q) and ICQ values are determined.

   VCE (Q) = VCC/2 = 12/2 = 6

2) By choosing drop across RE as 0.1

   VCC VE = VCC/10 = 12/10 = 1.2V

3) In transistor since base current is very small, so IE is approximately equal to IC (IE = IC) , IERE = 1.2V ; ICRE =1.2V

   RE = VE ⁄ IE =1.2⁄1mA =1.2KΩ

4) Applying Kirchoff's voltage law to the collector circuit in the

diagram $RC = (VCC - VCE - VE) / IC = (12 - 6 - 1.2)/1mA = 4.8K\Omega$

5) The voltage across R2 is

$VBB = VCC * R2 / (R1 + R2)$ --------- (1)

$VBB = VBE + IERE = 0.6 + (10^{-3})(10^{3} * 1.2) \backslash = 1.8V$ ----------(2)

Substitute (2) in (1)

$1.8 = 12R2/(R1+R2) R2 = 0.1761R1$---------- (a)

6) $S=1+ R1R2/ (R1+R2) RE$

$8 = 1+ R1R2/(R1+R2) 1.2*10^{3}$ ---------- (b)

By solving (a) and (b) we get

$R1 = 56K\Omega$ $R2 = 9.8K\Omega$

TABULATION:

Input Voltage (V_s or Vin) =_____V

S.No	Frequency f(Hz)	Output voltage V_o(Volt)	Gain in dB= $20\log(V_0/V_{in})$ dB

Capacitor calculations:

To provide low reactance's almost short circuit at the operating frequency
f=100HZ. X cE = 0.1RE , Xci =0.1 Zi, Xco =0.001 Z_0

7) X cE << RE,
X cE =RE/10 =1.2K/10=120
=> CE= 0.132µF
8) XCi=Zi/10 Where Zi=hie//RE = 8.18KΩ
=> Ci =1.96µF
9) XCo= ZO/1000
Z_O=RL//RC = 827Ω
=> C_O = 19.2µF

Standard values
R11= R21= R1=56 KΩ, R22 = R12 =R2 = 9.8 KΩ, RE1 =RE2 =RE =1.2 KΩ,
RC1 =RC2 =RC=4.8 KΩ, RL=10Ω, Ci=0.1µF,CC= 0.01µF,CE = 1µF C0= 10µF.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Apply supply voltage, Vcc= 12V.
3. Make sure that the transistor is operating in active region by keeping Vce half of Vcc.
4. Now feed an ac signal of 20mV at the input of the amplifier with different frequencies ranging from 100Hz to 1MHz and measure the amplifier output voltage, Vo
5. Now calculate the gain in db at various input signal frequencies.
6. Draw a graph with frequencies on X- axis and gain in db on Y- axis.

Post-Lab Exercise

1. Why the voltage gain of RC coupled amplifier falls in low frequency range?
2. Why the voltage gain of RC coupled amplifier falls at high frequency range?
3. Write the applications of multistage amplifier.
4. What is the difference between single stage & multistage amplifier?
5. Why RC coupling is better than direct & transformer coupling?

RESULT:

Thus the two stage RC Coupled (Cascaded) multistage amplifier was designed, constructed and verified the performance of and determined the frequency response and Bandwidth.

PSPICE TUTORIAL

I. Opening PSpice

• Find PSpice on the C-Drive. Open Schematics or you can go to PSpice A_D and then click on the schematic icon  .

• You will see the window as shown in Figure 1.

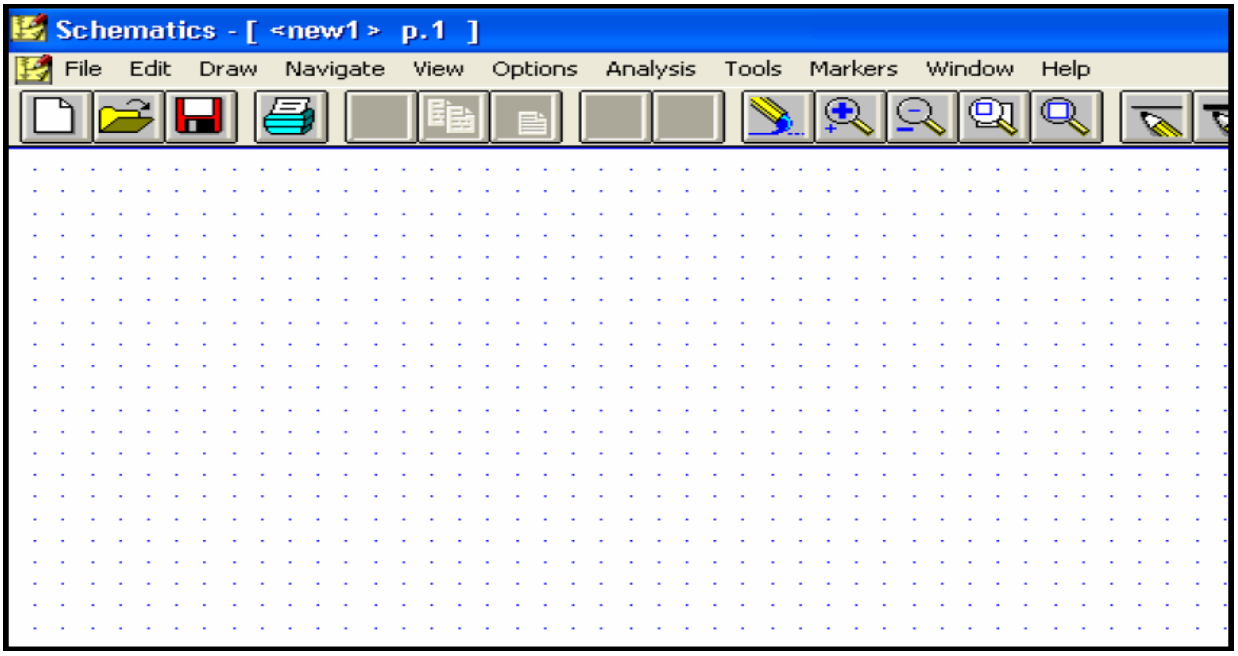


Figure 1

II. Drawing the circuit

A. Getting the Parts

- The first thing that you have to do is get some or all of the parts you need.
- This can be done by
    - Clicking on the 'get new parts' button  , or
    - Pressing "Control+G", or
    - Going to "Draw" and selecting "Get New Part..."
- Once this box is open, select a part that you want in your circuit. This can be done by typing in the name (part name) or scrolling down the list until you find it.

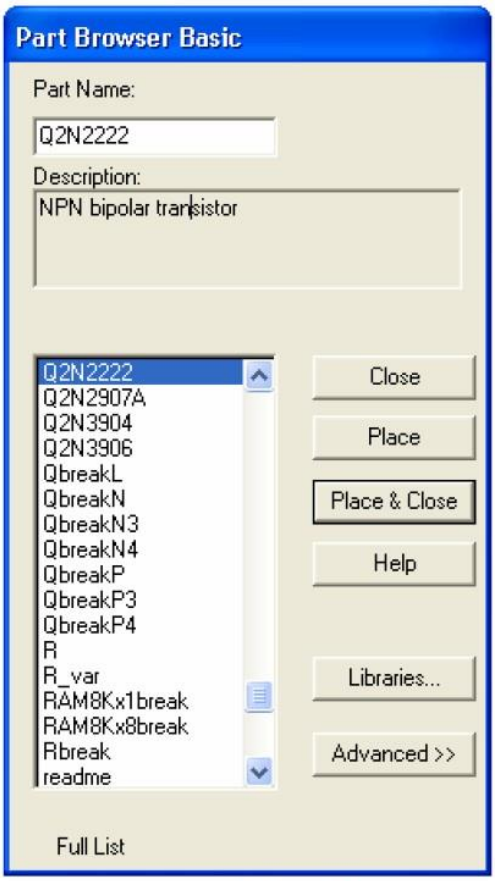


Figure 2

- An important prerequisite to building a schematic is the availability of the necessary parts (in the form of symbols) for assembly. *Schematics* have an extensive symbol libraries and a fully integrated symbol editor for creating your own symbols or modifying existing symbols. For the labs you will be using the existing symbols.
- Some common parts are:
  - r - resistor
  - C - capacitor
  - L - inductor
  - d - diode
  - GND_ANALOG or GND_EARTH -- this is very important, you MUST have a ground in your circuit
  - VAC and VDC
  - Q2N – bipolar transistor
  - VSIN –Transient sine voltage source

- Upon selecting your part (you will also see description of the part below part name and you can see the symbol of that part when you click on ***advanced*** in the above figure), click on the place button (you will see the part attached to the

mouse pointer) then click where you want it placed (somewhere on the white page with the blue dots), if you need multiple instances of this part click again, once you have selected that part right click your mouse the part will not be attached to the mouse pointer. Don't worry about putting it in exactly the right place, it can always be moved later.

- If you want to take a part and close then you just select the part and click on ***place& close***.
- Once you have all the parts you think you need, close that box. You can always open it again later if you need more or different parts. (The parts you have selected will be listed on the menu bar for quick access)

B. Placing the Parts

- You should have most of the parts that you need at this point.
- Now, all you do is put them in the places that make the most sense (usually a rectangle works well for simple circuits). Just select the part (It will become Red) and drag it where you want it.
- To rotate parts so that they will fit in you circuit nicely, click on the part and press "Ctrl+R" (or Edit "Rotate"). To flip them, press "Ctrl+F" (or Edit "Flip").
- If you have any parts left over, just select them and press "Delete".

C. Connecting the Circuit

- Now that your parts are arranged well, you'll have to attach them with wires.
- Go up to the tool bar and
    - select "Draw Wire"  or
    - "Ctrl+W" or
    - go to "Draw" and select "Wire".

- With the pencil looking pointer, click on one end of a part, when you move your mouse around, you should see dotted lines appear. Attach the other end of your wire to the next part in the circuit.
- Repeat this until your circuit is completely wired.
- If you want to make a node (to make a wire go more then one place), click somewhere on the wire and then click to the part (or the other wire). Or you can go from the part to the wire.
- To get rid of the pencil, right click.
- If you end up with extra dots near your parts, you probably have an extra wire, select this short wire (it will turn red), then press "Delete".

- If the wire doesn't go the way you want (it doesn't look the way you want), you can make extra bends in it by clicking in different places on the way (each click will form a corner).

D. Changing the Name of the Part

- You probably don't want to keep the names C1, C2 etc., especially if you didn't put the parts in the most logical order. To change the name, double click on the present name (C1, or R1 or whatever your part is), and then a box will pop up (Edit Reference Designator) see Figure 3. In the top window, you can type in the name you want the part to have.

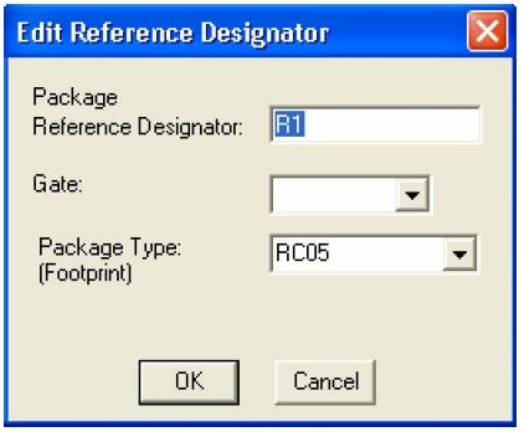


Figure 3

- Note that if you double click on the part or its value, a different box will appear.

E. Changing the Value of the Part

- If you only want to change the value of the part (if you don't want all your resistors to be 1K ohms), you can double click on the present value and a box called "Set Attribute Value" will appear see Figure 4. Type in the new value and press OK. Use u for micro as in uF = microFarad.

Figure 4

F. Making Sure You Have a GND

- This is very important. You cannot do any simulation on the circuit if you don't have a ground. If you aren't sure where to put it, place it near the negative side of your voltage source.

G. Voltage and Current Bubbles

- These are important if you want to measure the voltage at a point or the current going through that point.
- To add voltage or current bubbles, go to the right side of the top tool bar and select "Voltage/Level Marker" (Ctrl+M)  or "Current Marker"  . To get either of these, go to "Markers" and either "Voltage/Level Marker" or "Current Marker".

III. Voltage Sources

A. VDC

- This is your basic direct current voltage source that simulates a simple battery and allows you to specify the voltage value.

B. VAC

- A few things to note about the alternating current source, first PSpice takes it to be a sine source, so if you want to simulate a cosine wave you need to add (or subtract) a 90° phase shift. There are three values which PSpice will allow you to alter, these being:
  - **ACMAG** which is the RMS value of the voltage.
  - **DC** which is the DC offset voltage
  - **ACPHASE** which is the phase angle of the voltage
- Note that the phase angle if left unspecified will be set by default to 0°

C. VSIN

- The SIN type of source is actually a damped sine with time delay, phase shift and a DC offset (see Figure 5). If you want to run a transient analysis you need to use the VSIN see how AC will effect your circuit over time. Do not use this type of source for a phasor or frequency sweep analysis, VAC would be appropriate for that.

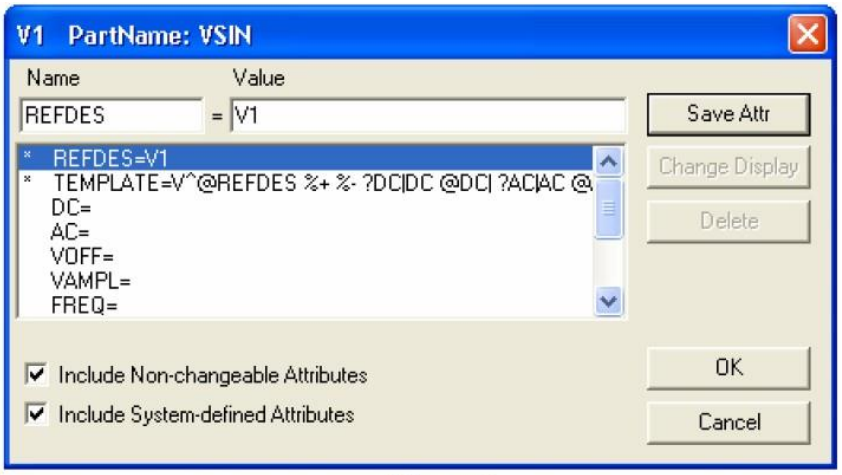


Figure 5

- **DC** the DC component of the sine wave
- **AC** the AC value of the sine wave
- **VOFF** is the DC offset value. It should be set to zero if you need a pure sinusoid.
- **Vamplitude** is the undamped amplitude of the sinusoid; i.e., the peak value measured from zero if there were no DC offset value.
- **FREQ** is the frequency in Hz of the sinusoid.
- **TD** is the time delay in seconds. Set this to zero for the normal sinusoid.
- **DF** is the damping factor. Also set this to zero for the normal sinusoid.
- **PHASE** is the phase advance in degrees. Set this to 90 if you need a cosine wave form.

- Note that the normal usage of this source type is to set **VOFF**, **TD** and **DF** to zero as this will give you a 'nice' sine wave.

D. VPULSE

- The VPULSE is often used for a transient simulation of a circuit where we want to make it act like a square wave source. It should never be used in a frequency response study because PSpice assumes it is in the time domain, and therefore your probe plot will give you inaccurate results. Details of VPULSE are (see Figure 6):
  - **DC** the DC component of the wave.
  - **AC** the AC component of the wave.
  - **V1** is the value when the pulse is not "on." So for a square wave, the value when the wave is 'low'. This can be zero or negative as required. For a pulsed current source, the units would be "amps" instead of "volts."
  - **V2** is the value when the pulse is fully turned 'on'. This can also be zero or negative. (Obviously, V1 and V2 should not be equal.) Again, the units would be "amps" if this were a current pulse.
  - **TD** is the time delay. The default units are seconds. The time delay may be zero, but not negative.

- **TR** is the rise time of the pulse. PSpice allows this value to be zero, but zero rise time may cause convergence problems in some transient analysis simulations. The default units are seconds.
- **TF** is the fall time in seconds of the pulse.
- **TW** is the pulse width. This is the time in seconds that the pulse is fully on.
- **PER** is the period and is the total time in seconds of the pulse.

- This is a very important source for us because we do a lot of work on with the square wave on the wave generator to see how various components and circuits respond to it.

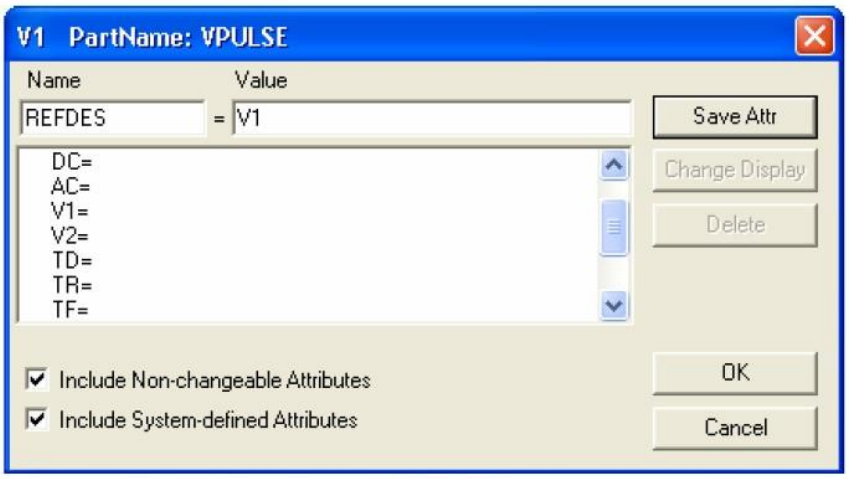


Figure 6

IV. Analysis Menu

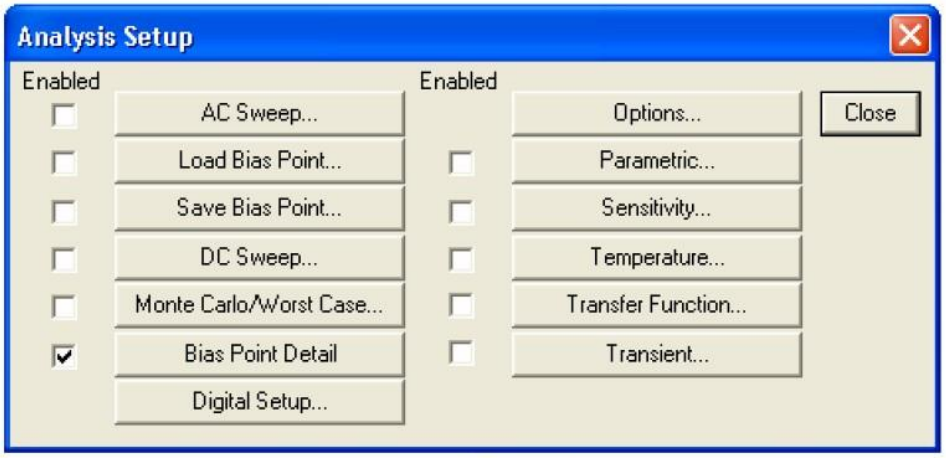


Figure 7

To open the analysis menu click on the  button.

A. DC Sweep

- The DC sweep allows you to do various different sweeps of your circuit to see how it responds to various conditions.
- For all the possible sweeps,
  - voltage,
  - current,
  - temperature, and
  - parameter and global

- You need to specify a start value, an end value, and the number of points you wish to calculate.
- For example you can sweep your circuit over a voltage range from 0 to 12 volts. The main two sweeps that will be most important to us at this stage are the voltage sweep and the current sweep. For these two, you need to indicate to PSpice what component you wish to sweep, for example V1 or V2.
- Another excellent feature of the DC sweep in PSpice, is the ability to do a nested sweep.
- A nested sweep allows you to run two simultaneous sweeps to see how changes in two different DC sources will affect your circuit.
- Once you've filled in the main sweep menu, click on the nested sweep button and choose the second type of source to sweep and name it, also specifying the start and end values. (Note: In some versions of PSpice you need to click on **enable nested sweep**). Again you can choose Linear, Octave or Decade, but also you can indicate your own list of values, example: 1V 10V 20V. **DO NOT** separate the values with commas.

B. Bias Point Detail

- This is a simple, but incredibly useful sweep. It will not launch Probe and so give you nothing to plot. But by clicking on **enable bias current display** or **enable bias voltage display**, this will indicate the voltage and current at certain points within the circuit.

C. Transient

The transient analysis is probably the most important analysis you can run in PSpice, and it computes various values of your circuit over time

- Choose **Analysis…Setup** from the menu bar, or click on the Setup Analysis button  in the toolbar. The Analysis Setup dialog box opens.

- Click on the **Transient** button in the Analysis Setup dialog box. The Transient dialog box opens.
- Two very important parameters in the transient analysis are (see Figure8):
    - **print step**
    - **final time**.

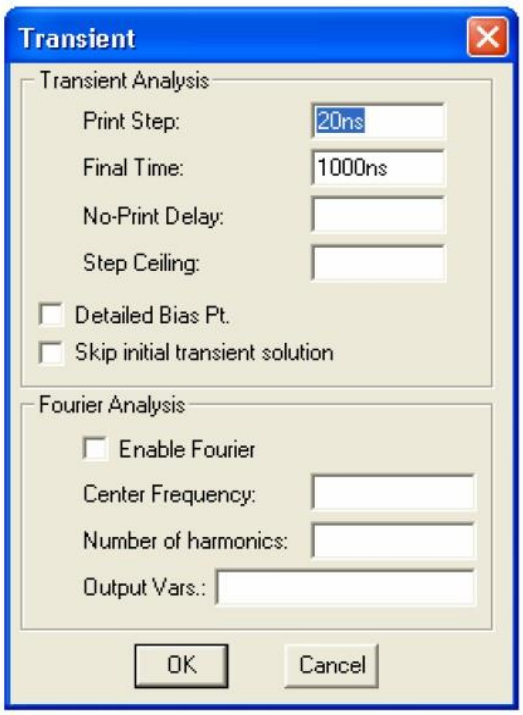


Figure 8

- The ratio of **final time: print step** (Keep print step atleast $1/100^{th}$ of the final time) determines how many calculations PSpice must make to plot a wave form. PSpice always defaults the start time to zero seconds and going until it reaches the user defined final time. It is incredibly important that you think about what print step you should use before running the simulation, if you make the print step too small the probe screen will be cluttered with unnecessary points making it hard to read, and taking extreme amounts of time for PSpice to calculate. However, at the opposite side of that coin is the problem that if you set the print step too high you might miss important phenomenon that are occurring over very short periods of time in the circuit. Therefore play with step time to see what works best for your circuit.

- You can set a step ceiling which will limit the size of each interval, thus increasing calculation speed. Another handy feature is the Fourier analysis, which allows you to specify your fundamental frequency and the number of harmonics you wish to see on the plot. PSpice defaults to the 9th harmonic unless you

specify otherwise, but this still will allow you to decompose a square wave to see it's components with sufficient detail.

V. Probe

A. Before you do the Probe

- You have to have your circuit properly drawn and saved.
- There must not be any floating parts on your page (i.e. unattached devices).
- You should make sure that all parts have the values that you want.
- There are no extra wires.
- It is very important that you have a ground on your circuit.
- Make sure that you have done the Analysis Setup and that only the things you want are enabled.

B. To Start the Probe:

- Click on the Simulate button on the tool bar  (or Analysis, Simulate, or F11).
- It will check to make sure you don't have any errors. If you do have errors, correct them.
- Then a new window will pop up. Here is where you can do your graphs.

C. Graphing:

- If you don't have any errors, you should get a window with a black background to pop up.
- If you did have errors, in the bottom, left hand side, it will say what your errors were (these may be difficult to understand, so go To "View - Output File").

D. Adding/Deleting Traces:

- PSpice will automatically put some traces in. You will probably want to change them.
- Go to Trace - Add Trace or  on the toolbar. Then select all the traces you want.
- To delete traces, select them on the bottom of the graph and push Delete.

E. Finding Points:

- There are Cursor buttons that allow you to find the maximum or minimum or just a point on the line. These are located on the toolbar (to the right).

- Select which curve you want to look at and then select "Toggle Cursor"  .
- Then you can find the max, min, the slope, or the relative max or min ( is find relative max).

VI. Measuring DC Analysis

- If you want to measure DC levels you can use two parts to view these levels. These parts are placed on the schematic drawing the same way any other part is placed. VIEWPOINT is a voltage viewing point, which will show the value after the circuit is simulated. You place VIEWPOINT on a node. IPROBE is a current probe, which will show the value after the circuit is simulated. You need to put this part between two parts, so that current flowing in that branch can be measured. If you have measurements that are time-varying (i.e. a sinusoid) then you need to run *Probe*.

EXPT.NO: 7 ANALYSIS OF BJT WITH FIXED BIAS AND VOLTAGE DIVIDER BIAS USING SPICE

AIM:

To design and simulate using Spice the BJT with fixed bias and voltage divider bias**.**

PRE-LAB EXERCISE:

1. What is Biasing?
2. Types of Biasing in BJT?
3. Explain fixed Bias?
4. Describe voltage divider bias?
5. Illustrate different configurations of BJT?

COMPONENTS REQUIRED:

Pc with PSPICE software.

THEORY:

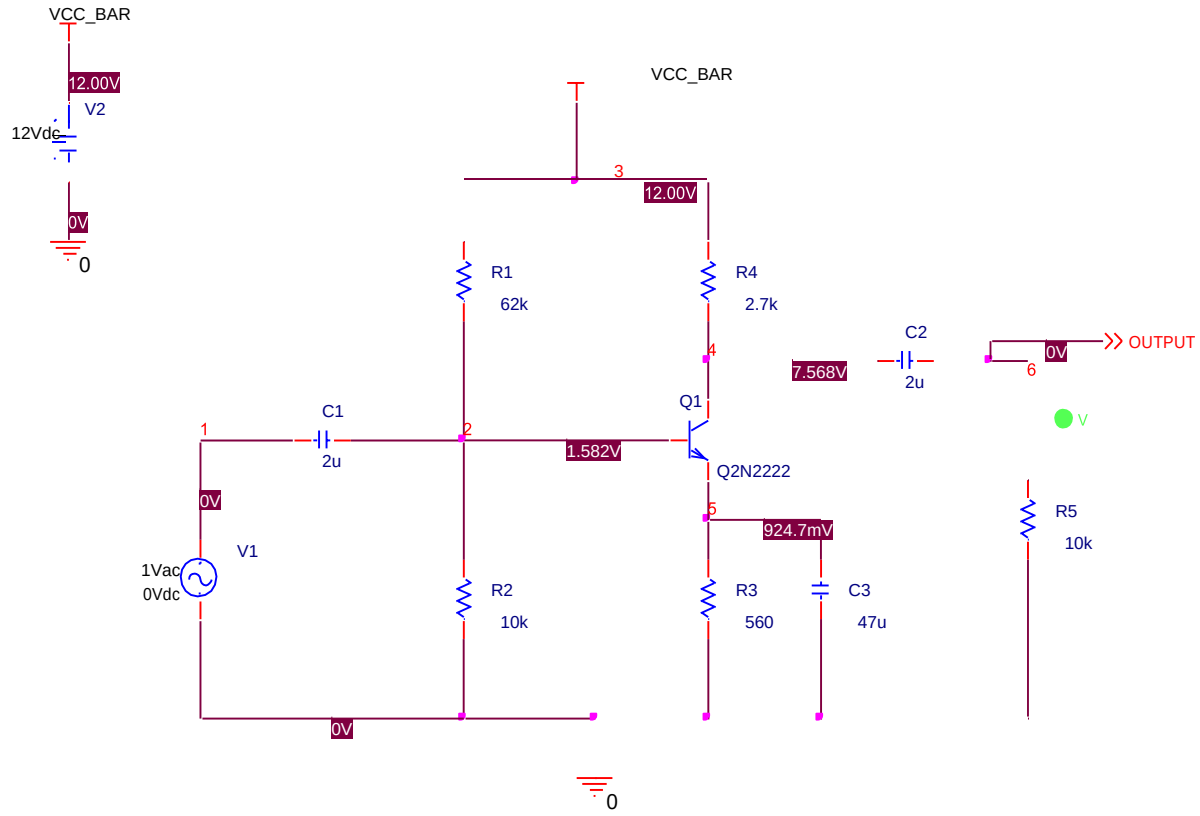
In common emitter configuration input is connected between base and the emitter while the output is taken between collector and emitter. Thus emitter is common to input and output circuits. In this configuration, the bias voltages are applied between collector and emitter and base and emitter. Emitter base junction is forward biased and the base is made more positive than the emitter by V_{BE}, collector-emitter junction is reverse-biased and the collector is made more positive than emitter by $V_{CE.}$ The value of V_{CE} must be greater than that of $V_{BE.}$ The base current I_B flows in the input circuit and collector current I_C flows in the output circuit. The current gain between the input and output sides is obtained; and since the input resistance is again less than the output resistance (though difference is not as much as in case of common base arrangement) there will be high voltage and power gains like those in equivalent vacuum tube circuits. The common emitter produces a reversal between input and output signals. Common emitter (CE) is commonly used because it's current, voltage and power gains are quite high and output impedance ratio is moderate.

The ratio of change in collector current (output current) and change in base current (input current) is called the base current amplification factor β*.

$$\text{i.e. } \beta = \Delta I_C / \Delta I_B$$

In CE configuration, a small collector current flows even when base current is zero (i.e. base lead is open). This is the collector cut-off current and denoted by I_{CEO}

CIRCUIT DIAGRAM:

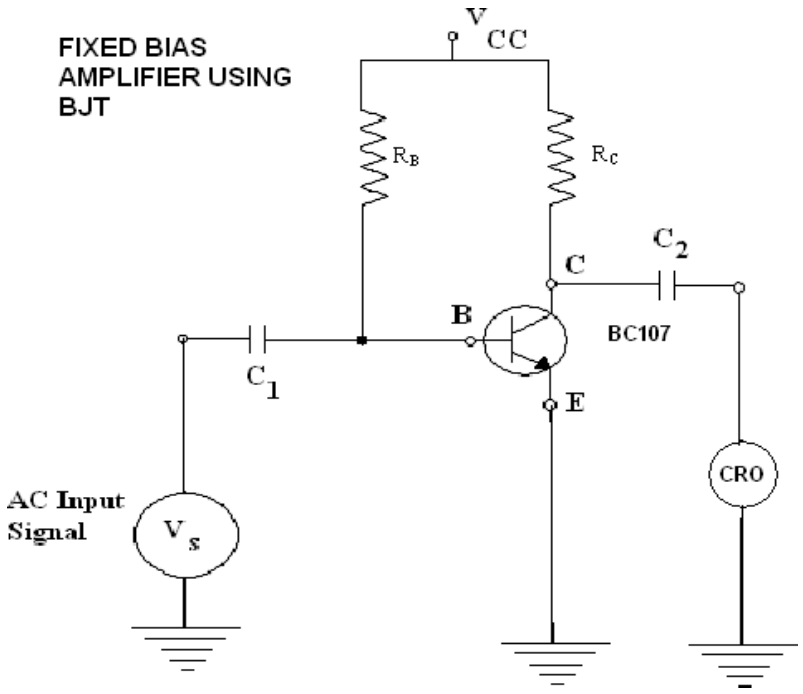


PROGRAM:

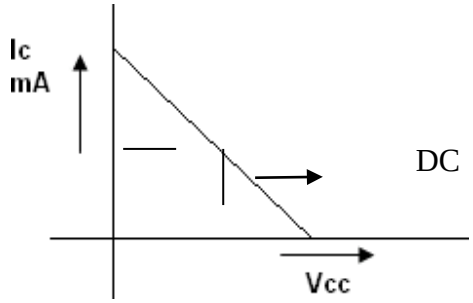
```
R_R1        2 VCC_BAR 62k
R_R2        0 2  10k
R_R3        0 5  560
R_R4        4 VCC_BAR 2.7k
R_R5        0 OUTPUT  10k
C_C1        1 2  2u
C_C2        4 OUTPUT  2u
C_C3        0 5  47u
V_V1        1 0 DC 0Vdc AC 1Vac
V_V2        VCC_BAR 0 12Vdc
Q_Q1        4 2 5 Q2N2222

.model Q2N2222 NPN(Is=14.34f Xti=3 Eg=1.11 Vaf=74.03 Bf=255.9 Ne=1.307
+                  Ise=14.34f Ikf=.2847 Xtb=1.5 Br=6.092 Nc=2 Isc=0 Ikr=0 Rc=1
+                  Cjc=7.306p Mjc=.3416 Vjc=.75 Fc=.5 Cje=22.01p Mje=.377 Vje=.75
+                  Tr=46.91n Tf=411.1p Itf=.6 Vtf=1.7 Xtf=3 Rb=10)
*                  National         pid=19          case=TO18
*                  88-09-07 bam creation
.AC DEC 101 10 10meg
.PROBE V(*) I(*) W(*) D(*) NOISE(*)
.END
```

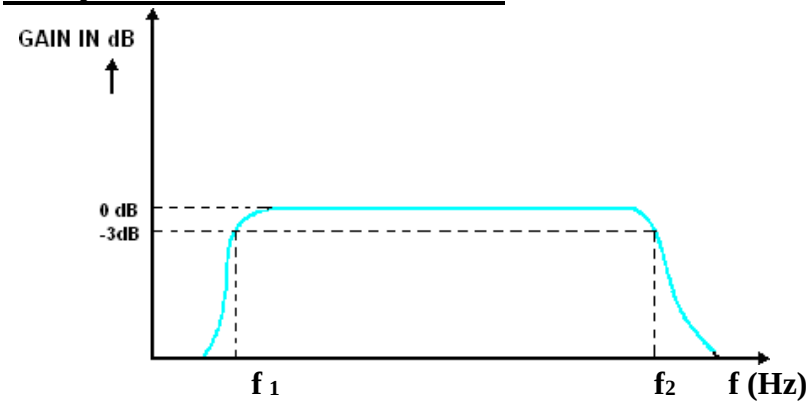
CIRCUIT DIAGRAM:



MODEL GRAPH: To locate Q point:



FREQUENCY RESPONSE CURVE



PROCEDURE:

1. Open Pspice software.
2. Goto Pspice AD/Lite in the software
3. Open the file Menu and create a new project
4. Type the program and save the file with extension .cir.
5. Simulate and Run the program and view the output frequency graph.

POST-LAB EXERCISE:

1. Explain about Spice?
2. Important tabs in spice?
3. Difference between fixed Bias and voltage divider bias?
4. Describe Rb and Rc?
5. Illustrate base current amplification factor?

RESULT:

Thus the BJT with fixed bias and voltage divider bias amplifier was simulated using Spice and frequency response was plotted.

EXPT.NO: 8 ANALYSIS OF FET, MOSFET WITH FIXED BIAS, SELF BIAS AND VOLTAGE DIVIDER BIAS USING SPICE

AIM:

To design and simulate using Spice the FET, MOSFET With Fixed Bias, Self-Bias And Voltage Divider Bias.

PRE-LAB EXERCISE:

1. Explain self-bias?
2. Importance of biasing?
3. Difference between fixed Bias and self-bias?
4. Describe various biasing technique of FET?
5. Illustrate various biasing technique of MOSFET?

COMPONENTS REQUIRED:

Pc with PSPICE software.

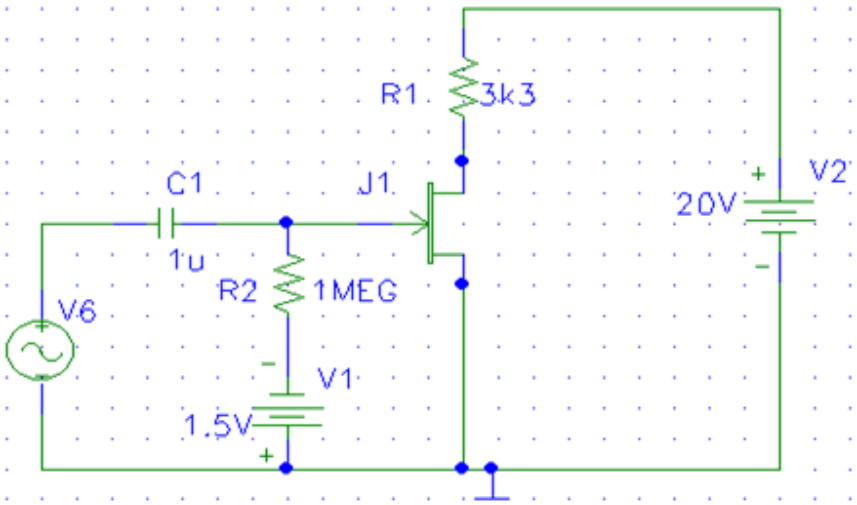
THEORY:

JFETs and **MOSFET**s are quite similar in their operating principles and in their electrical characteristics. However, they differ in some aspects, as detailed below :

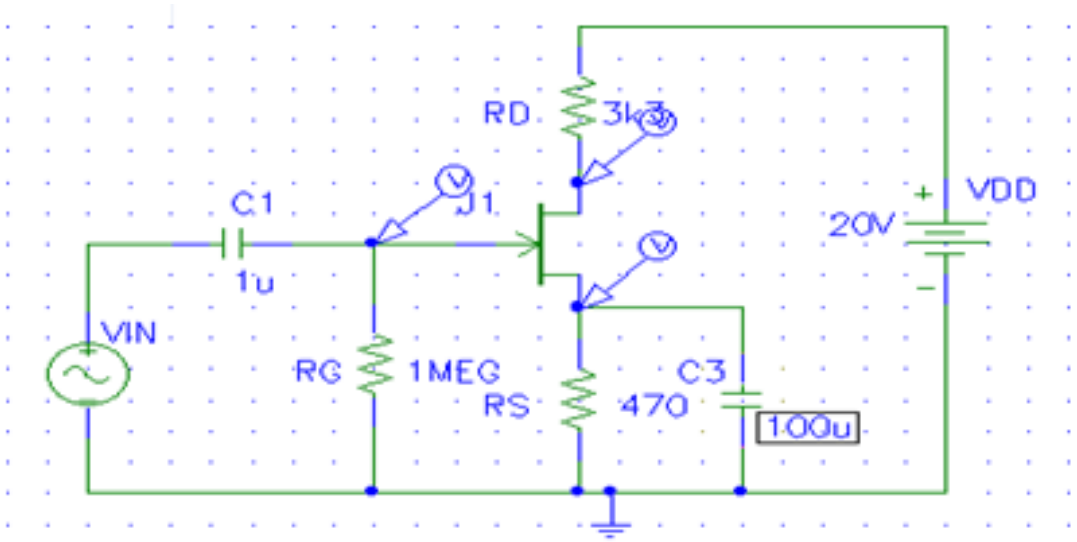
1. JFETs can only be operated in the **depletion mode** whereas MOSFETs can be operated in either depletion or in **enhancement mode**. In a JFET, if the gate is forward biased, excess- carrier injunction occurs and the gate current is substantial. Thus channel conductance is enhanced to some degree due to excess carriers but the device is never operated with gate forward biased because gate current is undesirable.
2. MOSFETs have input impedance much higher than that of JFETs. This is due to negligibly small leakage current.
3. JFETs have characteristic curves more flat than those of MOSFETs indicating a higher drain resistance.
4. When JFET is operated with a reverse bias on the junction, the gate current IG is larger than it would be in a comparable MOSFET. The current caused by minority carrier extraction across a reverse-biased junction is greater, per unit area, than the leakage current that is supported by the oxide layer in a MOSFET. Thus MOSFET devices are more useful in electrometer applications than are the JFETs.

For the above reasons, and also because MOSFETs are somewhat easier to manufacture, they are more widely used than are the JFETs

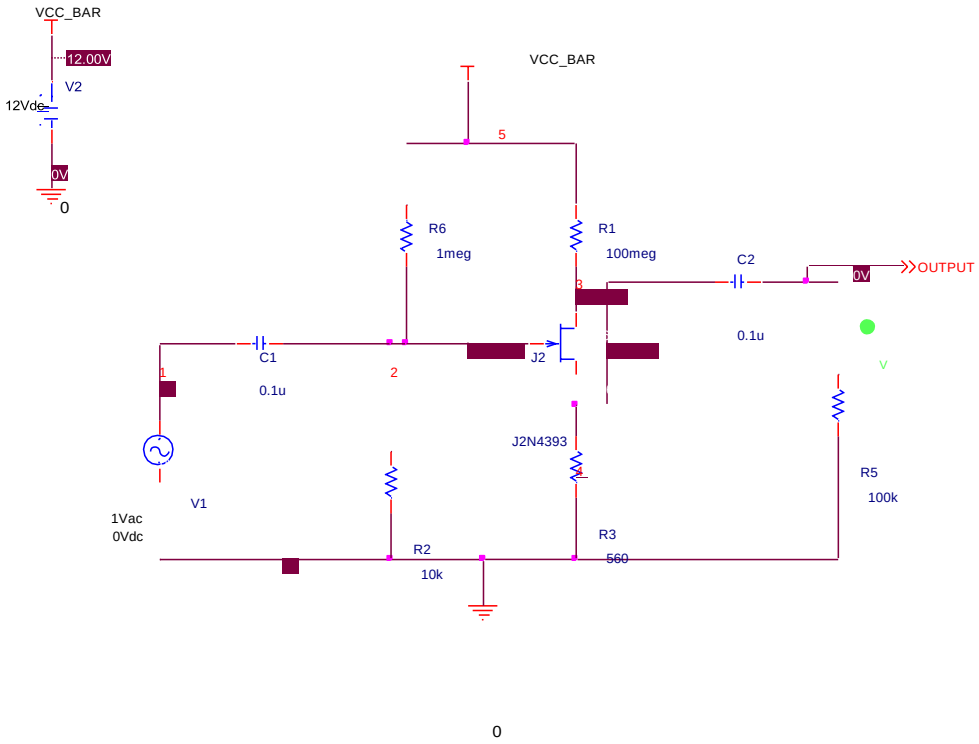
CIRCUIT DIAGRAM:
FET-FIXED BIAS



FET-SELF BIAS



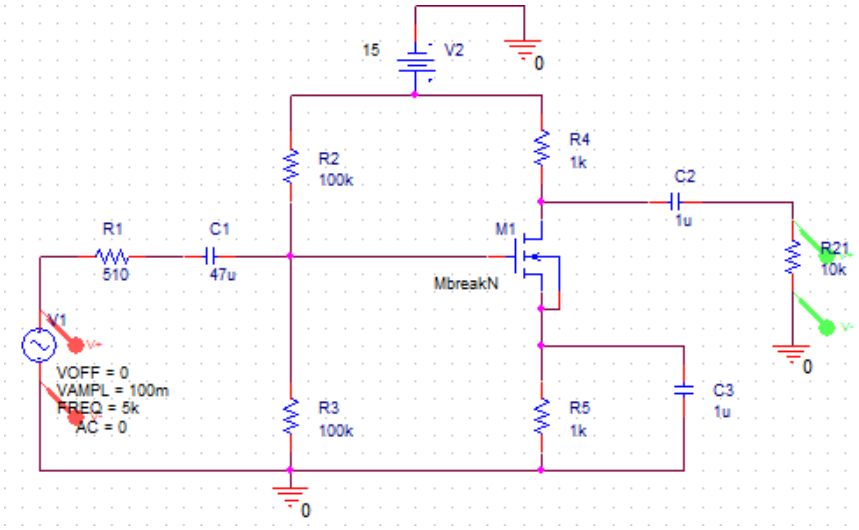
FET-VOLTAGE DIVIDER BIAS



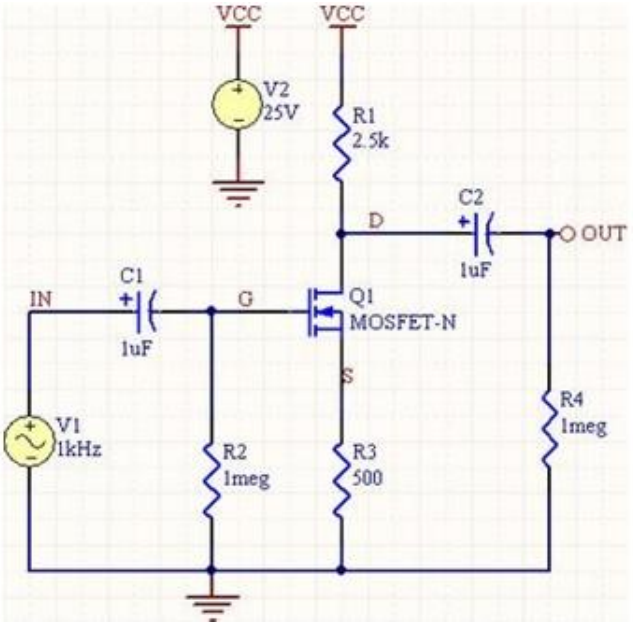
PROGRAM:

```
* source COMMON
R_R1        3VCC_BAR 100meg
R_R2        0 2  10k
R_R6        VCC_BAR 2 1meg
R_R3        0 4  560
J_J2        3 2 4 J2N4393
.model J2N4393          NJF(Beta=9.109m Betatce=-.5 Rd=1 Rs=1 Lambda=6m Vto=-1.422
+                   Vtotc=-2.5m Is=205.2f Isr=1.988p N=1 Nr=2 Xti=3 Alpha=20.98u
+                   Vk=123.7 Cgd=4.57p M=.4069 Pb=1 Fc=.5 Cgs=4.06p Kf=123E-18
+                   Af=1)
*                   National        pid=51          case=TO18
*                   88-07-13 bam BVmin=40
R_R5        0 OUTPUT  100k
C_C1        1 2  0.1u
C_C2        4 OUTPUT 0.1u
V_V1        1 0 DC 0Vdc AC 1Vac
V_V2        VCC_BAR 0 12Vdc
*Analysis directives:
.AC DEC 101 1meg 100000meg
.PROBE V(*) I(*) W(*) D(*) NOISE(*)
.END
```

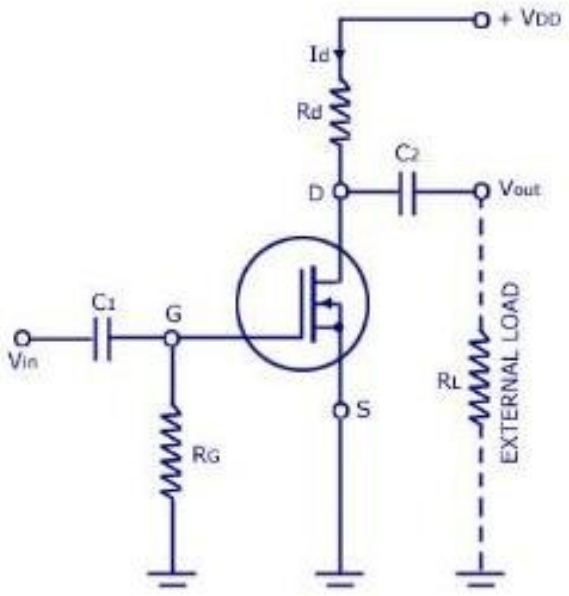
CIRCUIT DIAGRAM:
MOSFET-VOLTAGE DIVIDER BIAS



MOSFET-SELF BIAS



MOSFET- FIXED BIAS



PROCEDURE:

1. Open Pspice software.
2. Goto Pspice AD/Lite in the software
3. Open the file Menu and create a new project
4. Type the program and save the file with extension .cir.
5. Simulate and Run the program and view the output frequency graph.

POST-LAB EXERCISE:

1. Explain about drain current?
2. Elaborate modes of FET?
3. Difference between JFET and MOSFET?
4. Describe Rg and Rd?
5. Illustrate current amplification factor?

RESULT:

Thus the analysis of FET, MOSFET with fixed bias, self bias and voltage divider bias was simulated using Spice.

EXPT.NO: 9 ANALYSIS OF CASCODE AND CASCADE USING SPICE

AIM:

To design and simulate using Spice the cascade and cascade amplifier.

PRE-LAB EXERCISE:

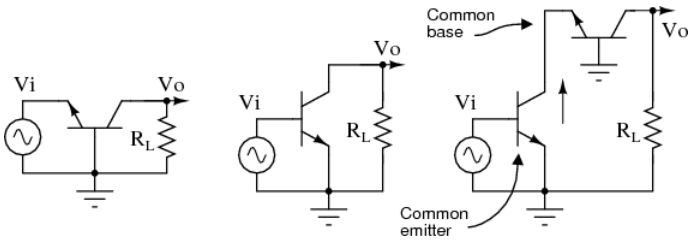
1. Explain cascade amplifier?
2. Importance of cascading?
3. Difference between cascode and cascade?
4. Describe miller effect?
5. Illustrate coupling circuits?

COMPONENTS REQUIRED:

Pc with PSPICE software.

THEORY:

While the C-B (common-base) amplifier is known for wider bandwidth than the C-E (common-emitter) configuration, the low input impedance (10s of Ω) of C-B is a limitation for many applications. The solution is to precede the C-B stage by a low gain C-E stage which has moderately high input impedance (kΩs). See Figure below. The stages are in a cascode configuration, stacked in series, as opposed to cascaded for a standard amplifier chain. See "Capacitor coupled three stage common-emitter amplifier" Capacitor coupled for a cascade example. The cascode amplifier configuration has both wide bandwidth and a moderately high input impedance.



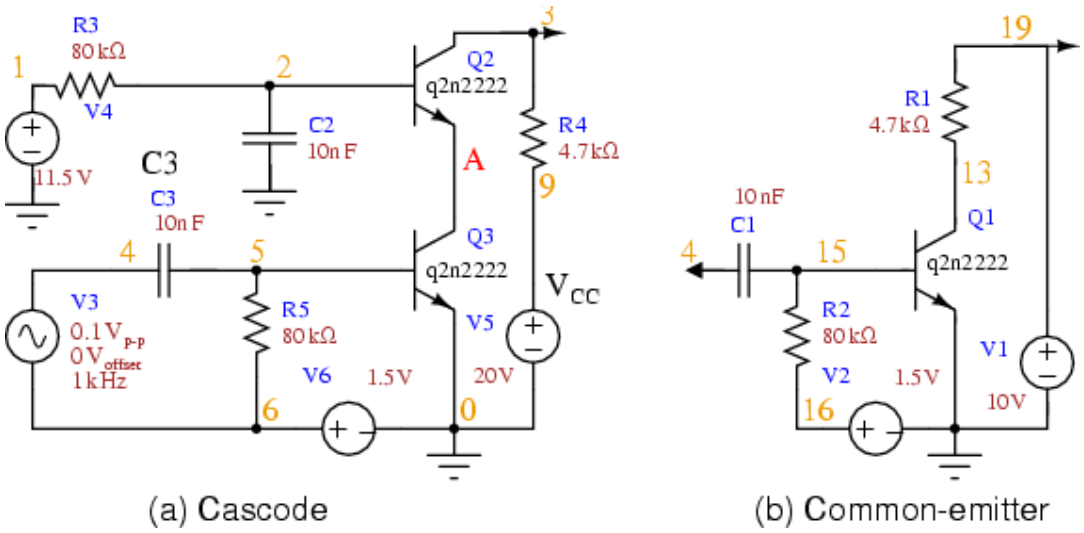
Common-base Common-emitter Cascode

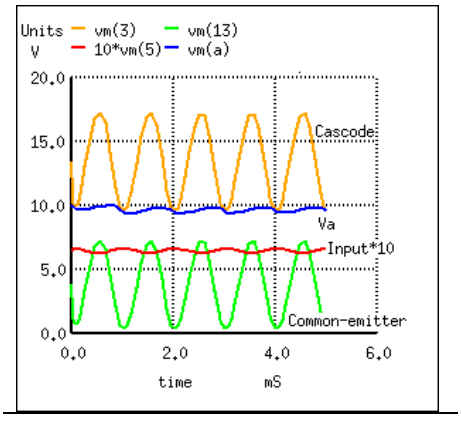
The cascode amplifier is combined common-emitter and common-base. This is an AC circuit equivalent with batteries and capacitors replaced by short circuits. The key to understanding the wide bandwidth of the cascode configuration is the Miller effect. The Miller effect is the multiplication of the bandwidth robbing collector-base capacitance by voltage gain Av. This C-B capacitance is smaller than the E-B capacitance. Thus, one would think that the C-B capacitance would have little effect. However, in the C-E configuration, the collector output signal is out of phase with the input at the base. The collector signal capacitively coupled back opposes the base signal. Moreover, the collector feedback is (1-Av) times larger than the base signal. Keep in mind that Av is a negative number for the inverting C-E amplifier. Thus, the small C-B capacitance appears (1+A|v|) times larger than its actual value. This capacitive gain reducing feedback increases with frequency, reducing the high frequency response of a C-E amplifier.

PROCEDURE:

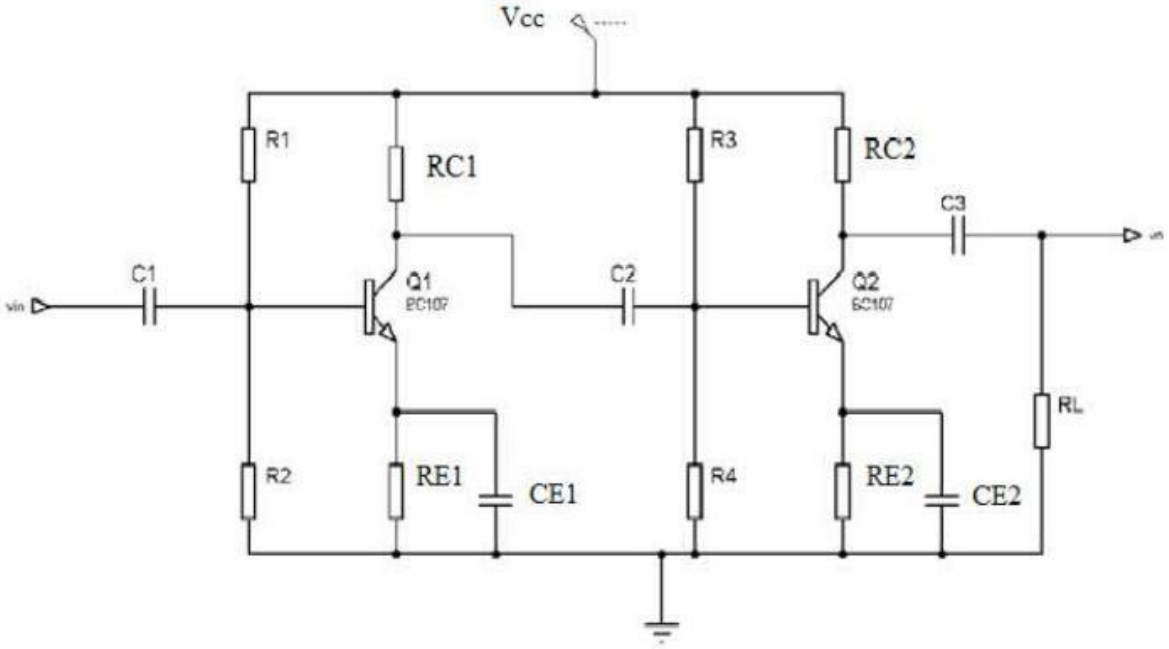
1. Open Pspice software.
2. Goto Pspice AD/Lite in the software
3. Open the file Menu and create a new project
4. Type the program and save the file with extension .cir.
5. Simulate and Run the program and view the output frequency graph.

CIRCUIT DIAGRAM:
CASCODE AMPLIFIER





CASCADE AMPLIFIERS



POST-LAB EXERCISE:

1. Explain about half power frequency?
2. why mid frequency gain is independent to frequency?
3. Give the advantages and disadvantages of cascade amplifier.
4. What is the method to increase the output voltage swing of an amplifier?
5. How load resistances influence the gain of BJT amplifiers?

RESULT:

Thus the analysis of cascade and cascade amplifier was simulated using Spice.

EXPT.NO: 10 ANALYSIS OF FREQUENCY RESPONSE OF BJT AND FET USING SPICE

AIM:

To design and simulate using Spice the BJT and FET and plot their frequency response.

PRE-LAB EXERCISE:

1. Explain positive slope and negative slope?
2. Importance of higher and lower frequency corner?
3. Difference between BJT and FET?
4. Describe bandwidth?
5. Illustrate voltage gain?

COMPONENTS REQUIRED:

Pc with PSPICE software.

THEORY:

Frequency Response of an electric or electronics circuit allows us to see exactly how the output gain (known as the *magnitude response*) and the phase (known as the *phase response*) changes at a particular single frequency, or over a whole range of different frequencies from 0Hz, (d.c.) to many thousands of mega-hertz, (MHz) depending upon the design characteristics of the circuit.

Generally, the frequency response analysis of a circuit or system is shown by plotting its gain, that is the size of its output signal to its input signal, Output/Input against a frequency scale over which the circuit or system is expected to operate. Then by knowing the circuits gain, (or loss) at each frequency point helps us to understand how well (or badly) the circuit can distinguish between signals of different frequencies.

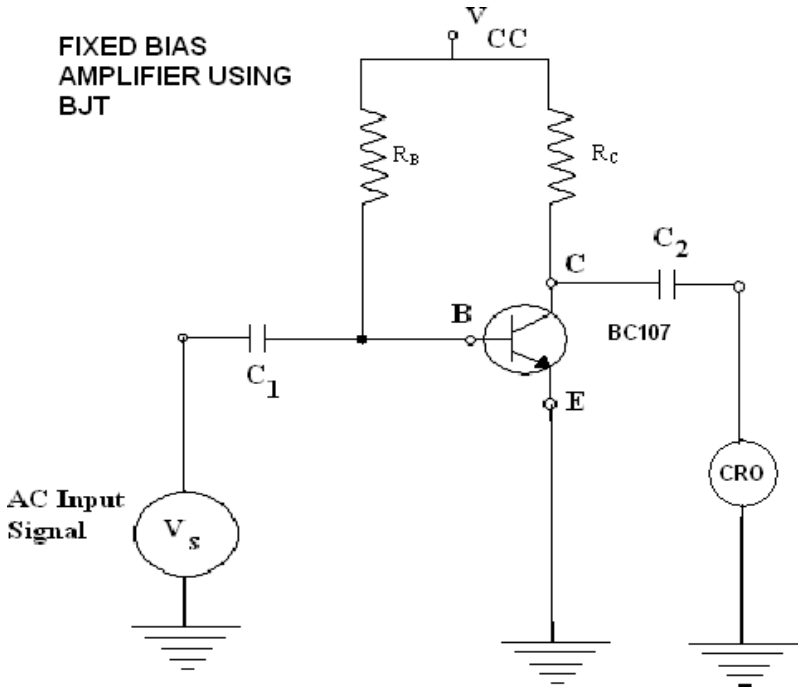
The frequency response of a given frequency dependent circuit can be displayed as a graphical sketch of magnitude (gain) against frequency (f). The horizontal frequency axis is usually plotted on a logarithmic scale while the vertical axis representing the voltage output or gain, is usually drawn as a linear scale in decimal divisions. Since a systems gain can be both positive or negative, the y-axis can therefore have both positive and negative values.

PROCEDURE:

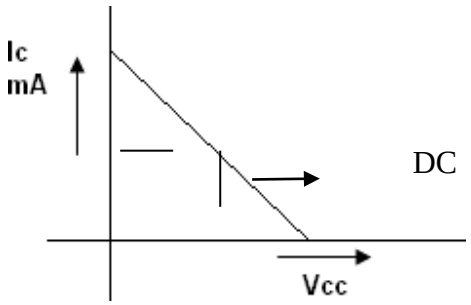
1. Open Pspice software.
2. Goto Pspice AD/Lite in the software
3. Open the file Menu and create a new project
4. Type the program and save the file with extension .cir.
5. Simulate and Run the program and view the output frequency graph.

CIRCUIT DIAGRAM:
CASCODE AMPLIFIER

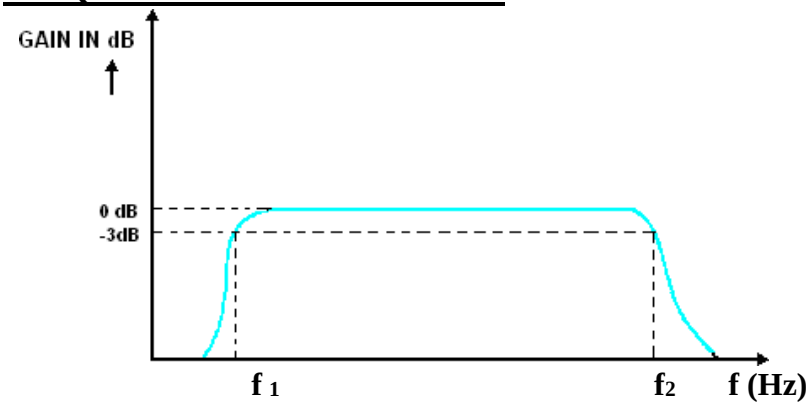
CIRCUIT DIAGRAM:



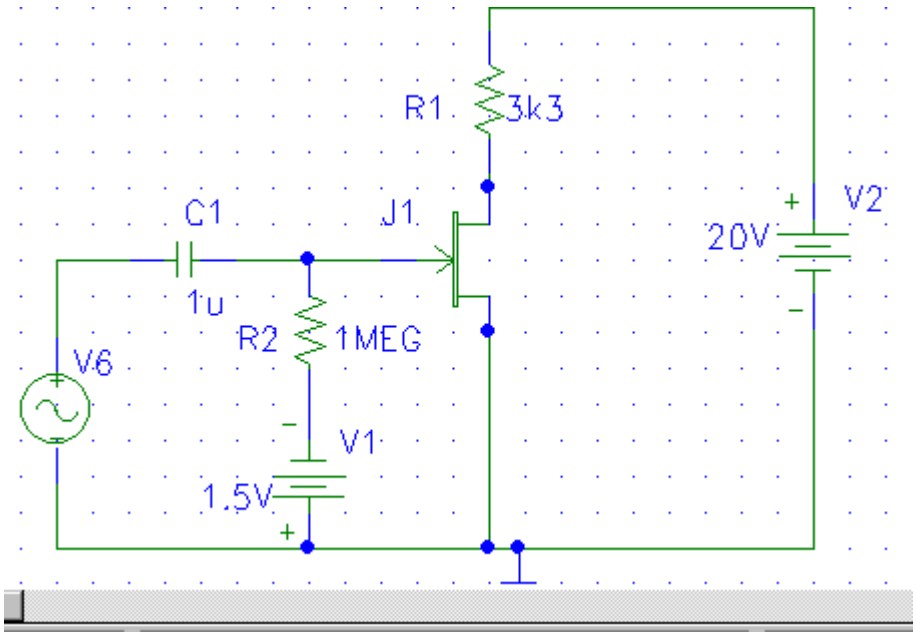
MODEL GRAPH: To locate Q point:

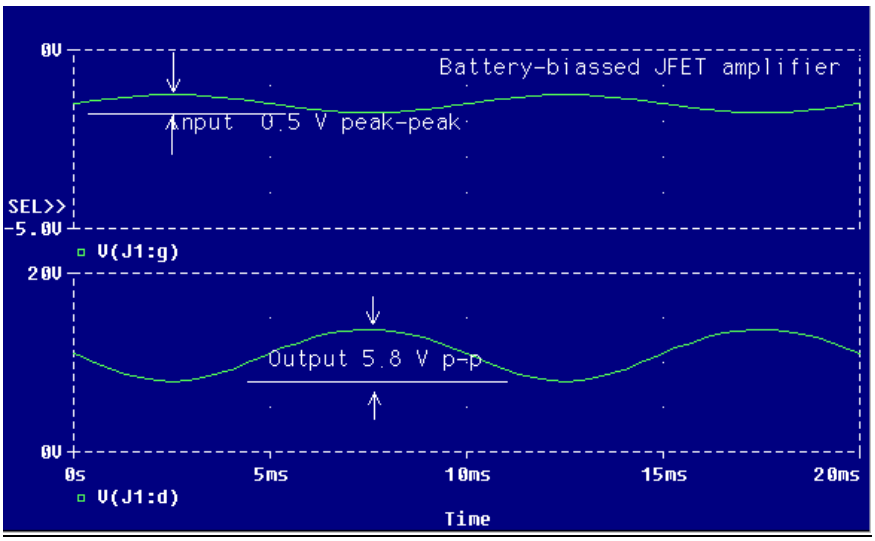


FREQUENCY RESPONSE CURVE



FET





POST-LAB EXERCISE:

1. Explain about frequency respose?
2. Plot the frequency response of BJT?
3. Give the advantages and disadvantages of BJT.
4. What is the method to increase response?
5. How would you plot the frequency response of MOSFET?

RESULT:

Thus the analysis of BJT and was simulated using Spice and frequency response was plotted.

EXPT NO. : 11 **STUDY OF LOGIC GATES AND FLIP FLOPS**
DATE :

AIM:

To study the basic logic gates, Flip Flop's and verifies their truth tables.

COMPONENTS REQUIRED:

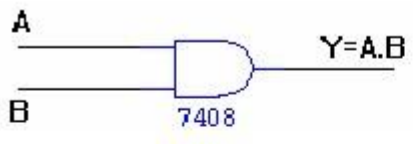
SL No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	X-OR GATE	IC 7486	1
7.	X-NOR GATE	IC747266	1
8.	AND GATE 3 I/P	IC 7411	1
9.	NAND GATE 3 I/P	IC 7410	1
10.	D –Flip Flop	IC 7474	1
11.	JK – Flip Flop	IC 7476	1
12.	IC TRAINER KIT	-	1
13.	PATCH CORD	-	14

PRE-LAB EXCERICE:

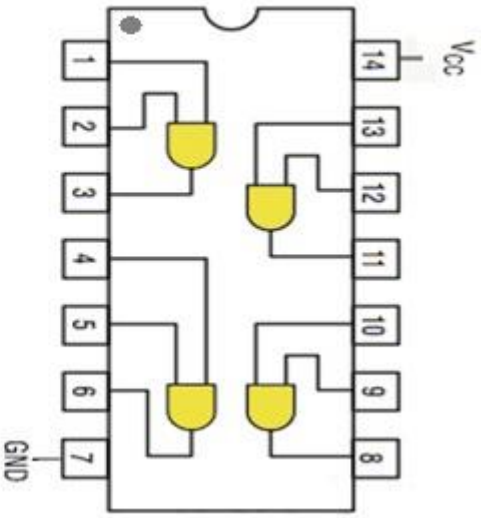
1. Differentiate Bit, Byte, and Nibble.
2. Explain the term universal gate.
3. What is a truth table? What is its significance in logic operations?
4. Define Minterm.& Maxterm.
5. What is sequential logic circuit?
6. What is latch?
7. What are the types of Latch?
8. What is Flip-flop?
9. What is the difference between latch & Flip-Flop?
10. What is the need of triggering?
11. What are the types of triggering?
12. What are the types Flip-flop?

AND GATE:

SYMBOL



PIN DIAGRAM

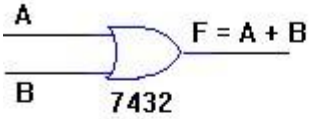


TRUTH TABLE

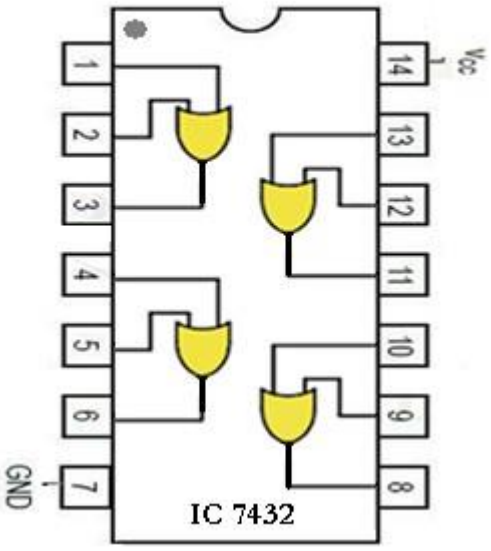
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE:

SYMBOL :



PIN DIAGRAM :

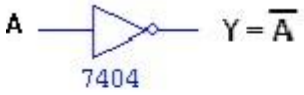


TRUTH TABLE

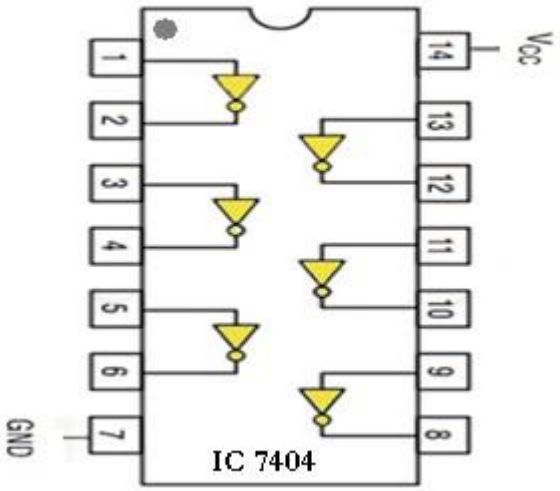
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

SYMBOL



PIN DIAGRAM

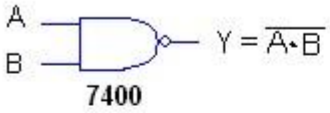


TRUTH TABLE :

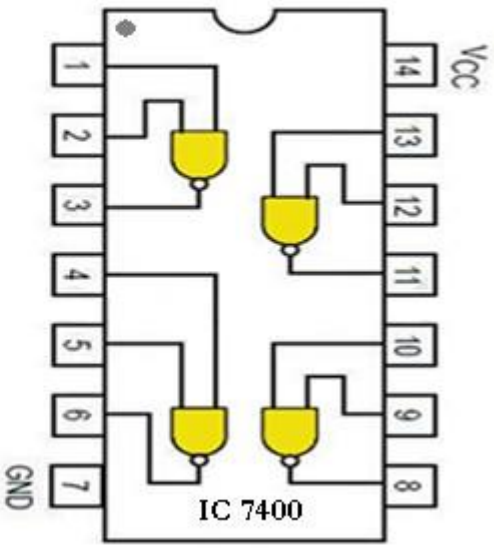
A	$\overline{A}$
0	1
1	0

2-INPUT NAND GATE:

SYMBOL



PIN DIAGRAM



TRUTH TABLE

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

THEORY:

Digital electronics is based on the binary number system. Instead of voltages which vary continuously, as in analog electronics, digital circuits involve voltages which take one of only two possible values. In our case these are 0 and 5 volts (TTL logic), but they are often referred to as LOW and HIGH, or FALSE and TRUE, or as the binary digits 0 and 1.The basic building blocks of digital electronics are logic gates which perform simple binary logic functions (AND, OR, NOT, etc.). From these devices, one can construct more complex circuits to do arithmetic, act as memory elements, and so on. Logic gates and other digital components come in the form of integrated circuits (ICs) which consist of small semiconductor chips packaged in a ceramic or plastic case with many pins.

The ICs are labeled by numbers like 74LSxx, where LS is technologies and xx is a number identifying the type of device.

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE (7408):

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE (7432):

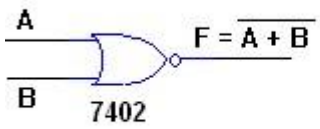
The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE (7404):

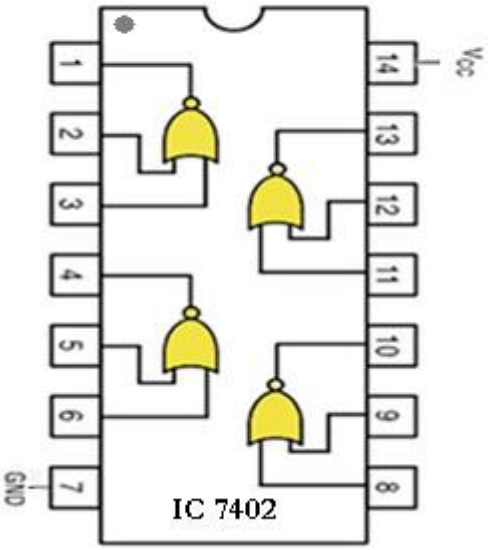
The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high. (i.e., output is Complement of the input)

NOR GATE:

SYMBOL :



PIN DIAGRAM :

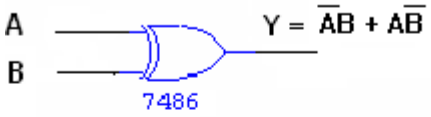


TRUTH TABLE

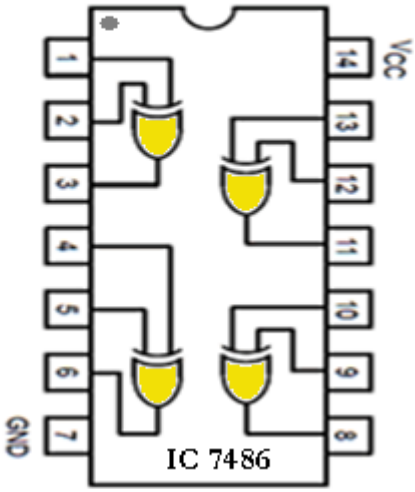
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

X-OR GATE:

SYMBOL



PIN DIAGRAM



TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

NAND GATE (7400):

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low. The output is low level when both inputs are high.

NOR GATE (7402):

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR (Exclusive OR) GATE (7486):

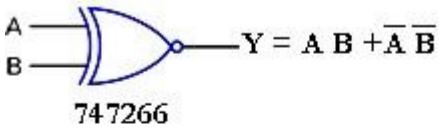
The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

X-NOR (Exclusive NOR) GATE (747266):

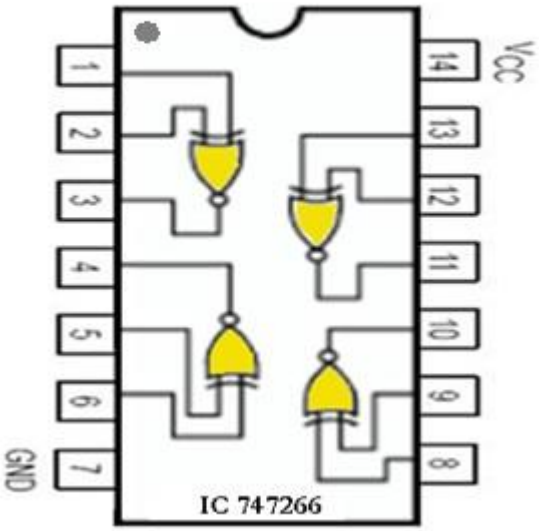
The output is high when both the inputs are low and both the inputs are high. The different inputs will produce low output (i.e. Logic ‘0’).

X-NOR GATE :

SYMBOL



PIN DIAGRAM

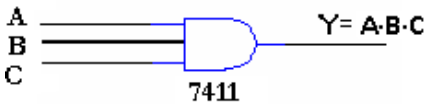


TRUTH TABLE :

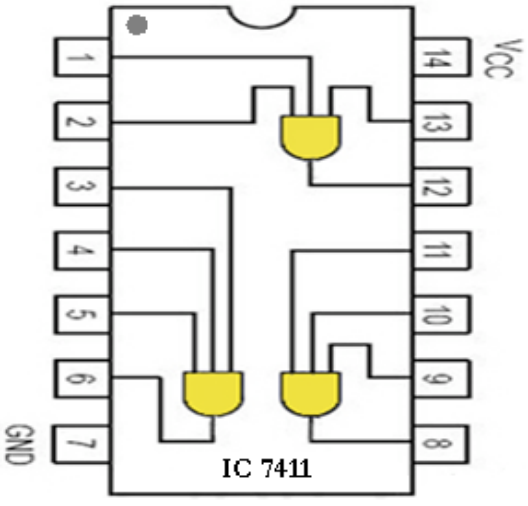
A	B	AB + $\overline{A}\overline{B}$
0	0	1
0	1	0
1	0	0
1	1	1

3-INPUT AND GATE :

SYMBOL



PIN DIAGRAM



TRUTH TABLE

A	B	C	A·B·C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

PROCEDURE:

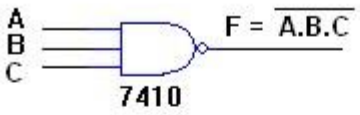
(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

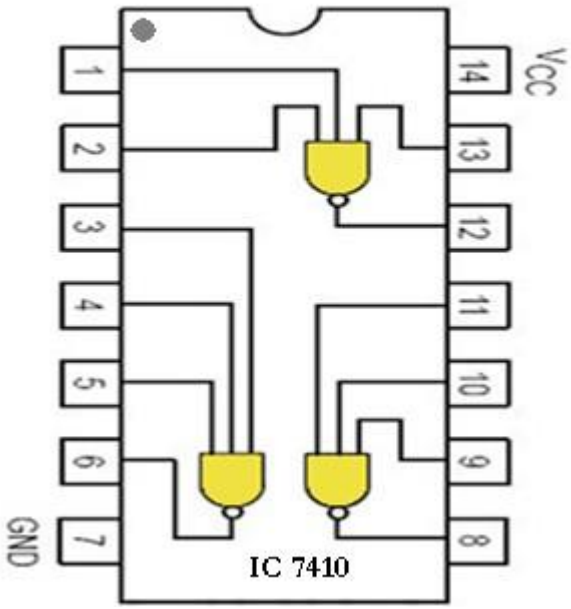
(iii) Observe the output and verify the truth table.

3-INPUT NAND GATE:

SYMBOL



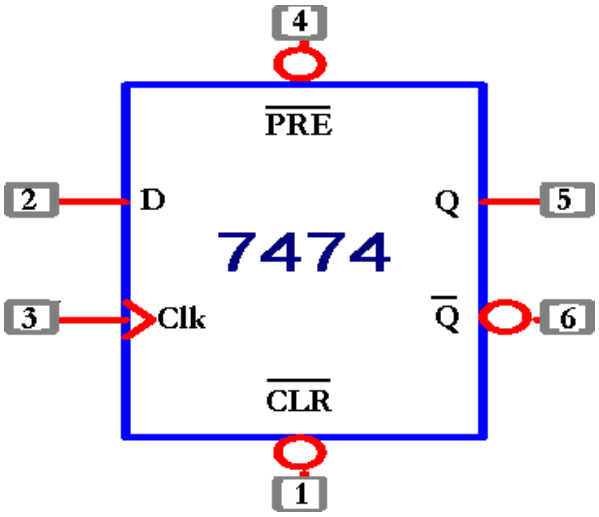
PIN DIAGRAM



TRUTH TABLE

A	B	C	$\overline{A.B.C}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

LOGIC DIAGRAM:



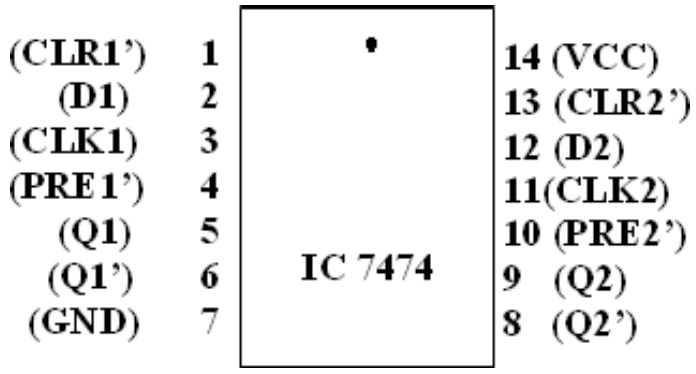
TRUTH TABLE:

Clock	Input D	Output Q
L	X	No change
H	0	0
H	1	1

FUNCTION TABLE:

CLK	D	Q	Q'
1	1	1	0
1	0	0	1

PIN DIAGRAM:



Theory:

A flip-flop is a simplest kind of sequential circuit that has only two states. It can be a binary 1 or 0. It is also used as a memory cell as it stores one bit of information.

D FLIPFLOP:

It is a single input version of the flip-flop. It accepts single data and provides output which is same as the applied input. It is called Delay flip flop. The output of the D FF as follows the input.

JK FLIP-FLOP:

JK flip-flops are far more versatile than RS and D-type flip-flops and they can perform many more functions than simple latches. JK Flip-flops 7476 which use level-clocking. It is important to remember that for normal operation the preset and clear inputs should be held (tied positive).

PROCEDURE:

i. The power supply to D flip-flop and JK flip-flop is switched on.
ii. The truth tables of flip flops are verified. In a JK flip flop, first we will consider the asynchronous operation of the flip flops. The J and K inputs have no effects on the asynchronous operation.

APPLICATIONS:

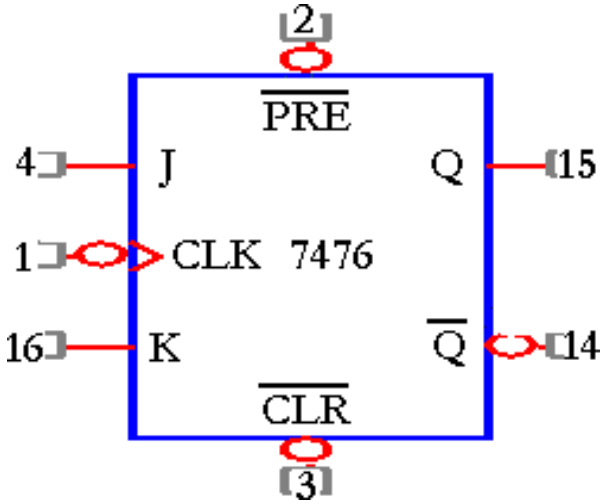
i. It finds immense use in parallel data storage.
ii. It is used in shift registers and counter circuits.
iii. It can also be used in frequency divider.

POST-LAB EXCERICE:

1. What is meant by logic family?
2. State two advantages of CMOS logic.
3. What is a tri-state gate?
4. Define fan out for a logic circuit.
5. What are the applications of latch?
6. What is Excitation table?
7. What is Master-slave JK Flip-flop?
8. What is called transition (state) table?
9. Draw the symbol of SR, JK, T & D Flip-flop?
10. How to realize one Flip-flop using another Flip-flop?
11. What are the applications of Flip-flop?
12. What is the full form of SR, JK, T & D?

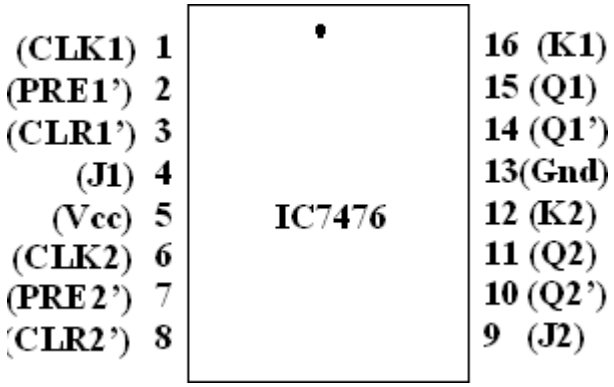
LOGIC DIAGRAM:

Truth Table



Inputs			Output Q
CLK	J	K	
X	X	X	Invalid
X	X	X	1
X	X	X	0
clk	0	0	Nochange
clk	0	1	0
clk	1	0	1
clk	1	1	Toggle

PIN DIAGRAM:



RESULT:

Thus different types of logic gates and Flip flops are studied and their truth table were verified.

EXPT NO. : 12 DESIGN AND IMPLEMENTATION OF CODE CONVERTORS UNSIG LOGIC GATES

AIM:

To design and implement 4-bit

(i) BCD to excess-3 code converter

(ii) Excess-3 to BCD code converter

(iii) Binary to gray code converter

(iv) Gray to binary code converter

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	X-OR GATE	IC 7486	1
2.	AND GATE	IC 7408	1
3.	OR GATE	IC 7432	1
4.	NOT GATE	IC 7404	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	35

PRE-LAB EXCERICE:

1. What is the need for code converter?
2. How do you convert binary numbers to corresponding Gray codes using a converter?
3. Define a code converter logic circuit.
4. How do you convert Gray code numbers to corresponding binary numbers using a converter?
5. What are the steps involved in the BCD to binary conversion process?

THEORY:

A code converter is a combinational logic circuit that changes the data presented in one type of binary code to another type of binary code.

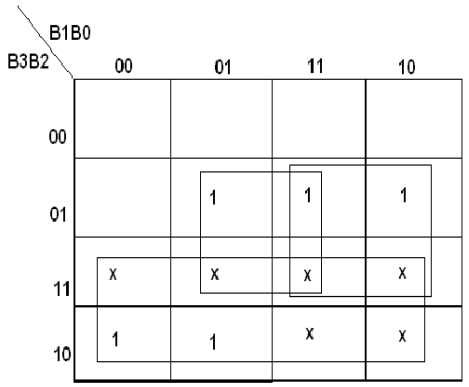
To convert from BCD to Excess-3 code, the input lines must supply the bit combination of elements as specified by code and the output lines generate the corresponding bit combination of code. The Excess-3 code represents a decimal number, in binary form, as a number greater than 3. An excess-3 code is obtained by adding 3 to a decimal number. The excess-3 code is a self -complementing code.

BCD TO EXCESS-3 CONVERTOR

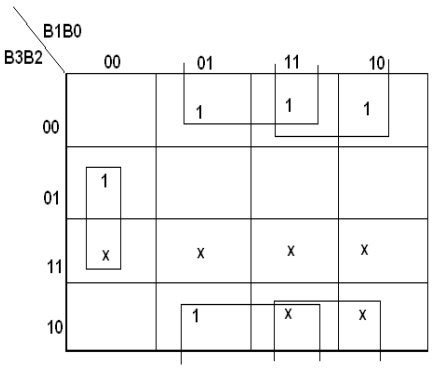
TRUTH TABLE:

BCD input				Excess – 3 output			
B3	**B2**	**B1**	**B0**	**E3**	**E2**	**E1**	**E0**
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

K-Map for E_3 and E_2:

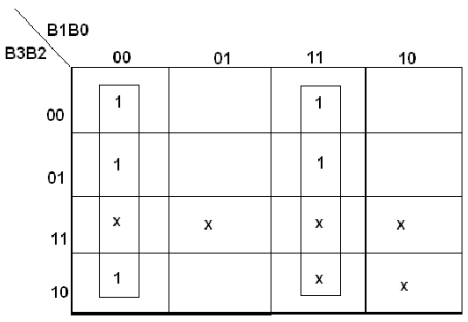


E3 = B3 + B2 (B0 + B1)

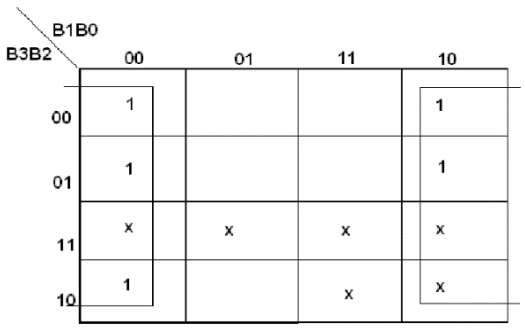


$E2 = B2 \oplus (B1 + B0)$

K-Map for E_1 and E_0:

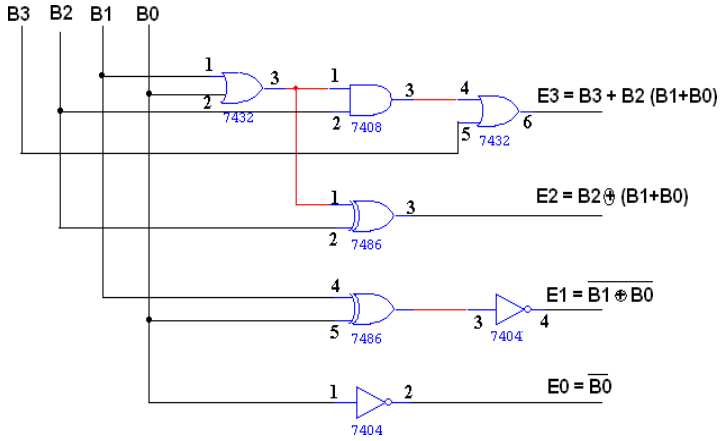


$E1 = B1 \overline{\oplus} B0$



$E0 = \overline{B0}$

LOGIC DIAGRAM:

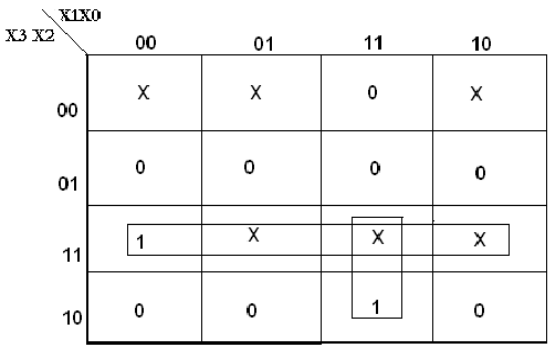


EXCESS-3 TO BCD CONVERTOR

TRUTH TABLE:

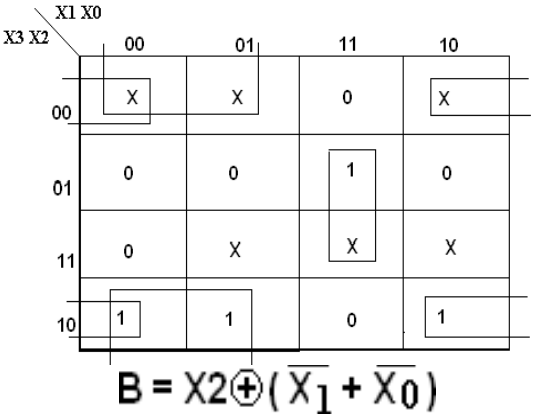
Excess – 3 Input				BCD Output			
X3	**X2**	**X1**	**X0**	**D**	**C**	**B**	**A**
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

K-Map for A:



A = X3 X2 + X1 X0 X3

K-Map for B:



$B = X2 \oplus (\overline{X_1} + \overline{X_0})$

Each one of the four maps represent one of the four outputs of the circuit as a function of the four input variables. A two-level logic diagram may be obtained directly from the Boolean expressions derived by the maps. These are various other possibilities for a logic diagram that implements this circuit.

K-Map for C:

X3 X2 \ X1 X0	00	01	11	10
00	X	X	0	X
01	0	1	X	1
11	0	X	X	X
10	X	1	0	1

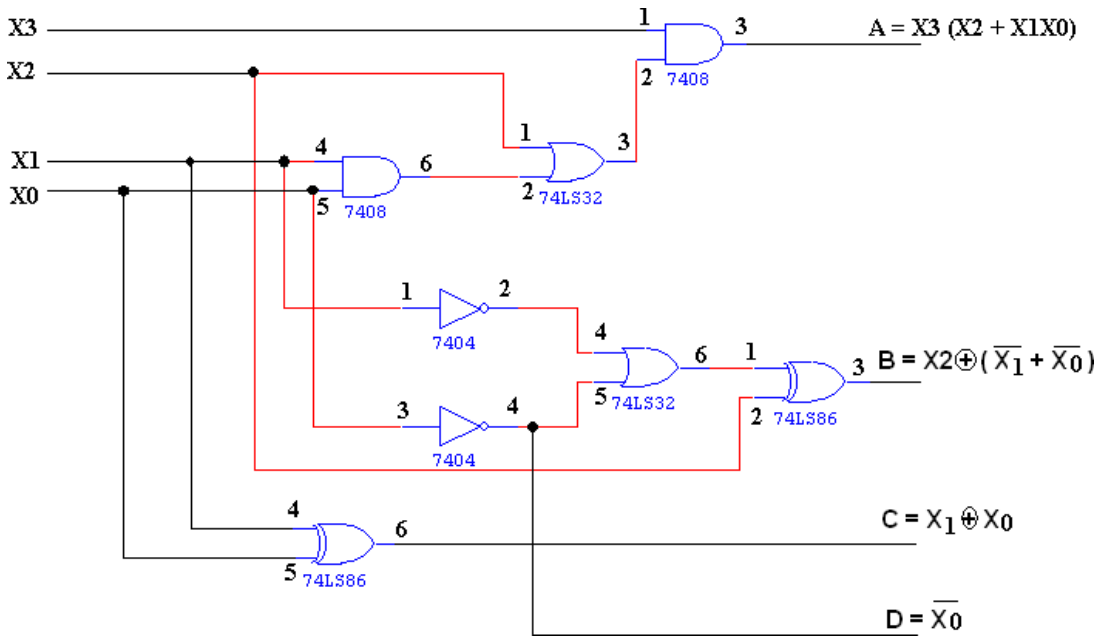
$C = X_1 \oplus X_0$

K-Map for D:

X3 X2 \ X1 X0	00	01	11	10
00	X	X	0	X
01	1	0	0	1
11	1	X	X	X
10	1	0	0	1

$D = \overline{X_0}$

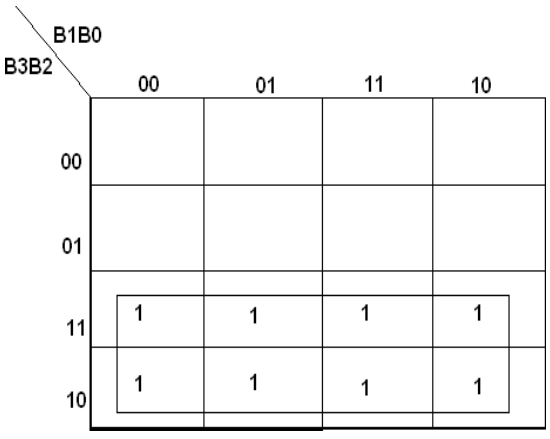
LOGIC DIAGRAM:

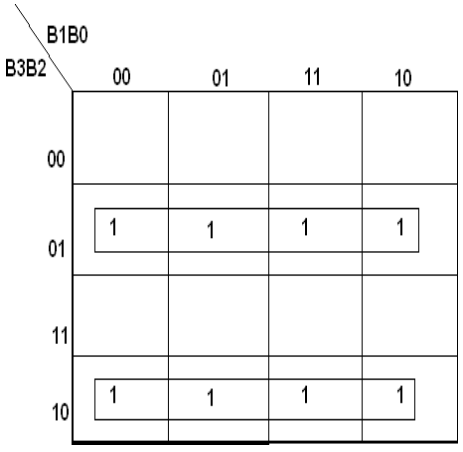


TRUTH TABLE:

Binary input				Gray code output			
B3	**B2**	**B1**	**B0**	**G3**	**G2**	**G1**	**G0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

K-Map for G_3 and G2





$G_3 = B_3$

$G2 = B3 \oplus B2 = B'_3 B_2 + B'_2 B_3$

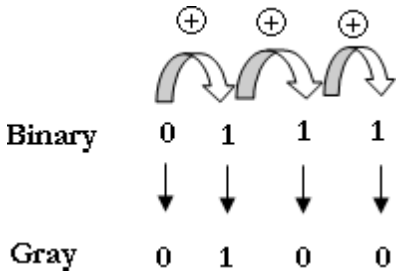
THEORY:

A code converter is a combinational logic circuit that changes the data presented in one type of binary code to another type of binary code.

BINARY TO GRAY CODE CONVERSION:

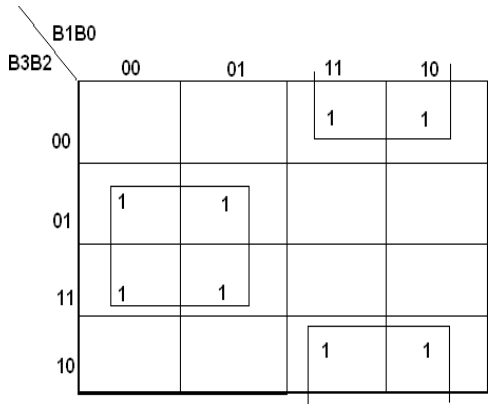
The advantage of gray code is that two adjacent code numbers differ by only one bit. It is used in some types of analog to digital converters.

- The MSB of the gray code is same as the MSB of the binary code.
- The second bit of the gray code is obtained by adding the first & second bits of binary code after eliminating carry, (or) XOR operation of two inputs.
- The third bit of the gray code is obtained by adding the second & third bits of binary code after eliminating carry & so on.

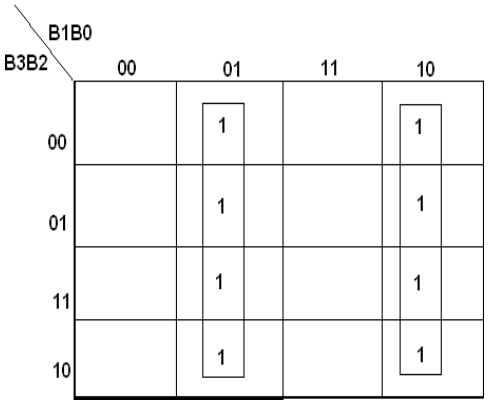


Gray code is a non-weighted code.

K-Map for G_1 and G_0:

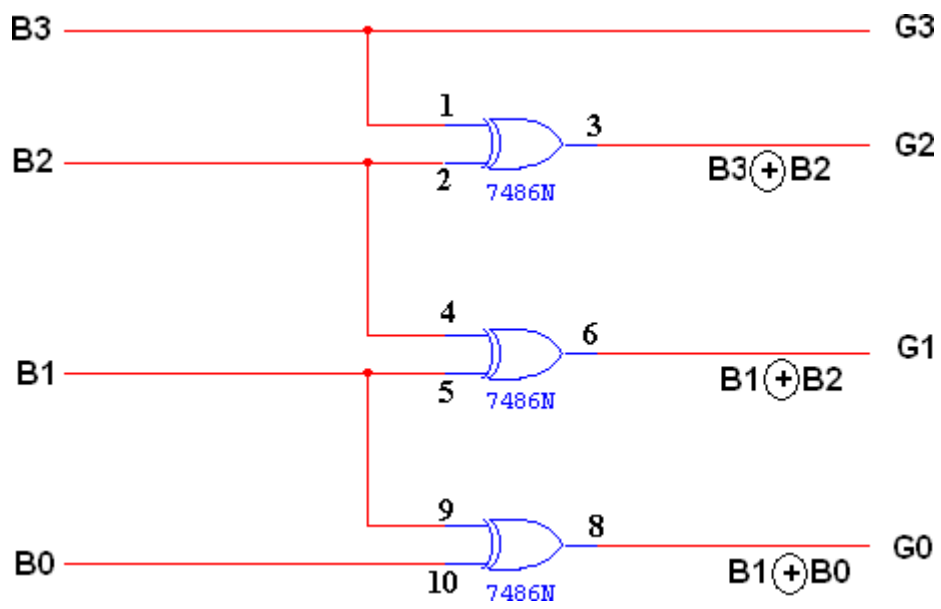


$G1 = B1 \oplus B2 = B_1 B'_2 + B_2 B'_1$



$G0 = B1 \oplus B0 = B_1 B'_0 + B'_1 B_0$

LOGIC DIAGRAM:

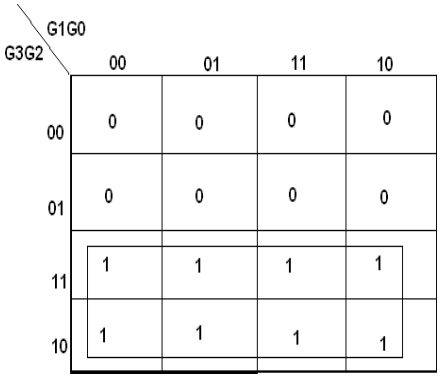


GRAY CODE TO BINARY CONVERTOR

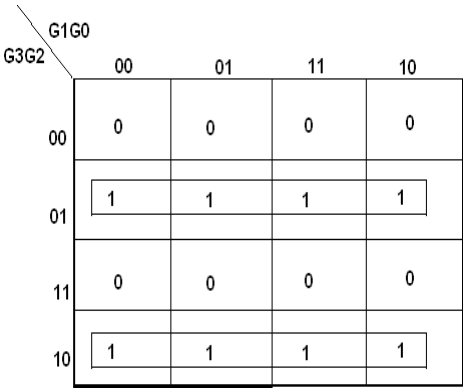
TRUTH TABLE:

Gray Code				Binary Code			
G3	**G2**	**G1**	**G0**	**B3**	**B2**	**B1**	**B0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

K-Map for B_3 and B_2::



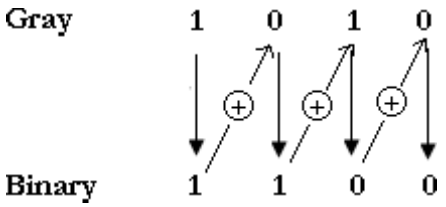
B3 = G3



B2 = G3⊕G2

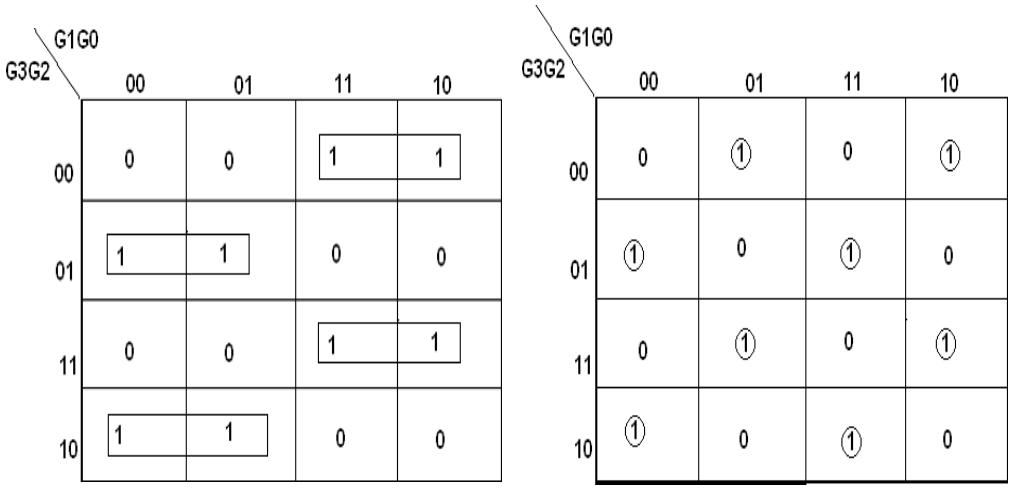
GRAY TO BINARY CODE CONVERSION:

- The MSB of the binary code is the same as the MSB of the gray code.
- The second bit of the binary code is obtained by adding the second bit of gray code and first bit of the binary code after eliminating carry.
- The third bit of the binary code is obtained by adding the second bit of binary code & third bit of gray code after eliminating carry & so on.

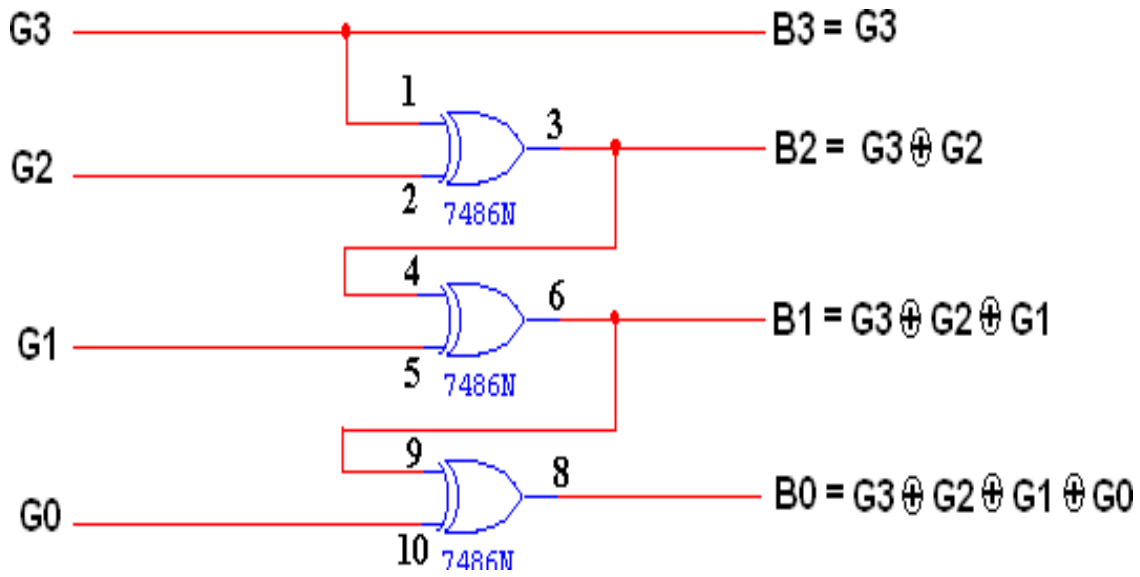


The input variable are designated as B3, B2, B1, B0 and the output variables are designated as G3, G2, G1, Go. from the truth table, combinational circuit is designed. The Boolean functions are obtained from K-Map for each output variable. A code converter is a circuit that makes the two systems compatible even though each uses a different binary code.

K-Map for B_1 and B_0:



LOGIC DIAGRAM:



PROCEDURE:

(i) Connections were given as per circuit diagram.
(ii) Logical inputs were given as per truth table
(iii) Observe the logical output and verify with the truth tables.

APPLICATIONS:

Code converters are circuits that make two systems compatible even though each of them used a different mode.

POST-LAB EXCERICE:

1. What is Gray code?
2. What are alphanumeric codes?
3. Draw the flow diagram for Gray to binary conversion.
4. What is ASCII code?
5. What is EBCDIC?

RESULT: Thus the different types of code converters were designed, constructed and their truth tables were verified.

EXPT NO. : 13 DESIGN & IMPLEMENTATIONOF 4-BIT ADDER/ SUBTRACTOR AND BCD ADDER USING IC 7483

AIM:

To design and implement 4-bit adder /subtractor and BCD adder using IC 7483.

COMPONENTS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QTY.
1.	IC	IC 7483	1
2.	EX-OR GATE	IC 7486	1
3.	NOT GATE	IC 7404	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	40

POST-LAB EXCERICE:

1. What is the need of binary adder?
2. What are the advantage & disadvantage of parallel adder?
3. What is ripple carry adder?
4. What is carry look ahead adder?
5. What is serial adder?

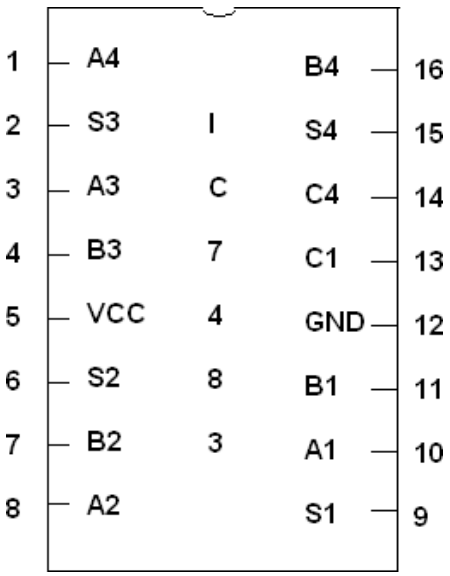
4 BIT BINARY ADDER:

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of next full adder in chain. The augends bits of 'A' and the addend bits of 'B' are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C_0 and it ripples through the full adder to the output carry C_4.

DATA TABLE FOR 4-BIT BIANRY ADDER / SUBTRACTOR :

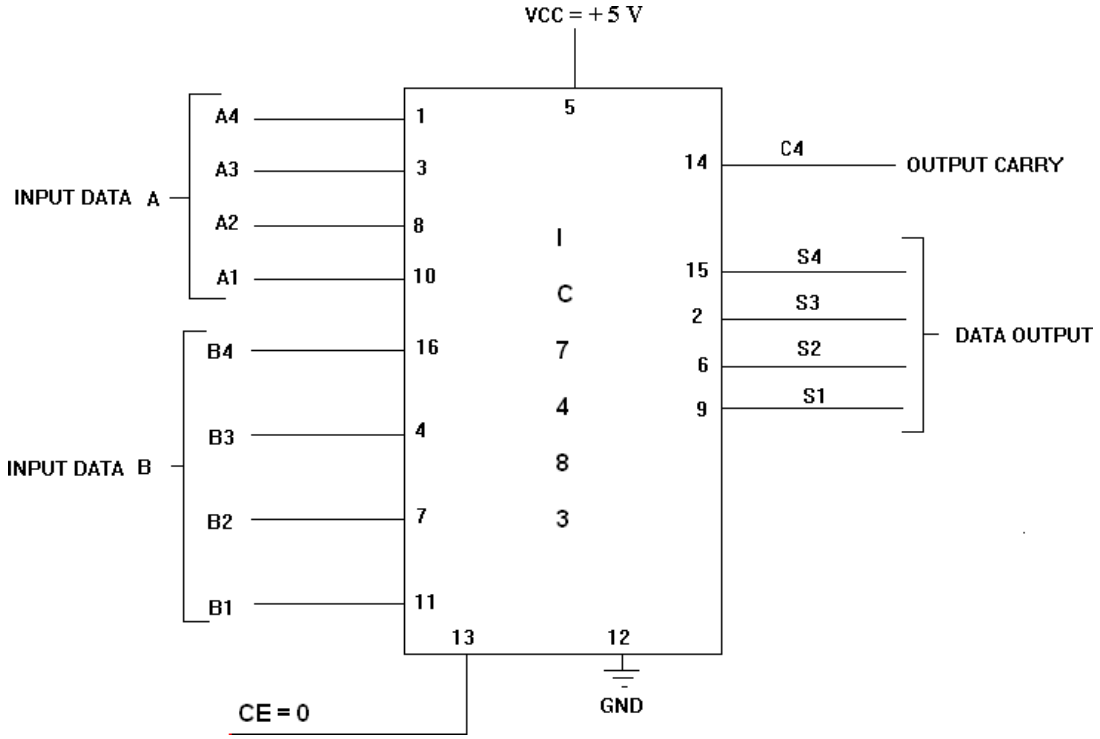
Input Data A				Input Data B				Addition					Subtraction				
A4	A3	A2	A1	B4	B3	B2	B1	C	S4	S3	S2	S1	B	D4	D3	D2	D1
1	0	0	0	0	0	1	0	0	1	0	1	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	1	0
0	0	0	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	0	1	1	1	1
1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	1	0	1

PIN DIAGRAM FOR IC 7483:

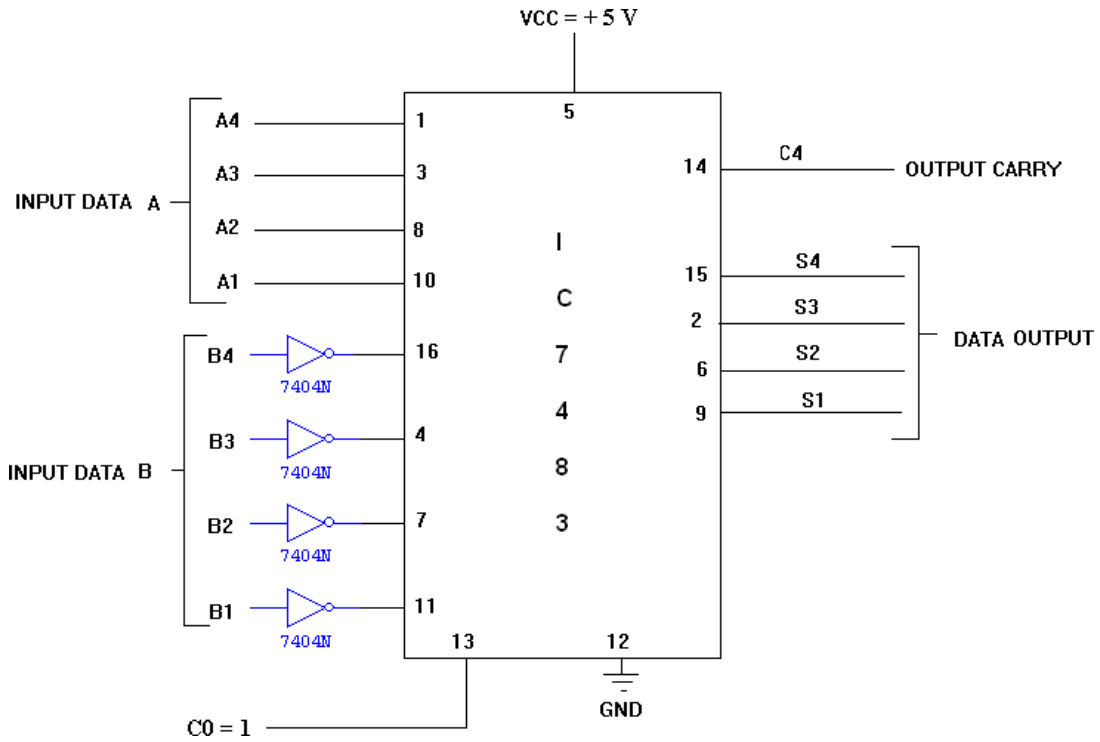


LOGIC DIAGRAM:

4-BIT BINARY ADDER



4-BIT BINARY SUBTRACTOR



Addition:

When addition is carried out the Invert is kept low so that bits B_3, B2,B1,B0 pass on to the full adders without any change and take part in the addition process in the normal way. Note that when the Invert is low, the carry-in for the first full adder is 0, as the carry input for the first adder is connected to the Inverter input, which is held low when addition is carried out.
The addition sequence for this adder is as follows

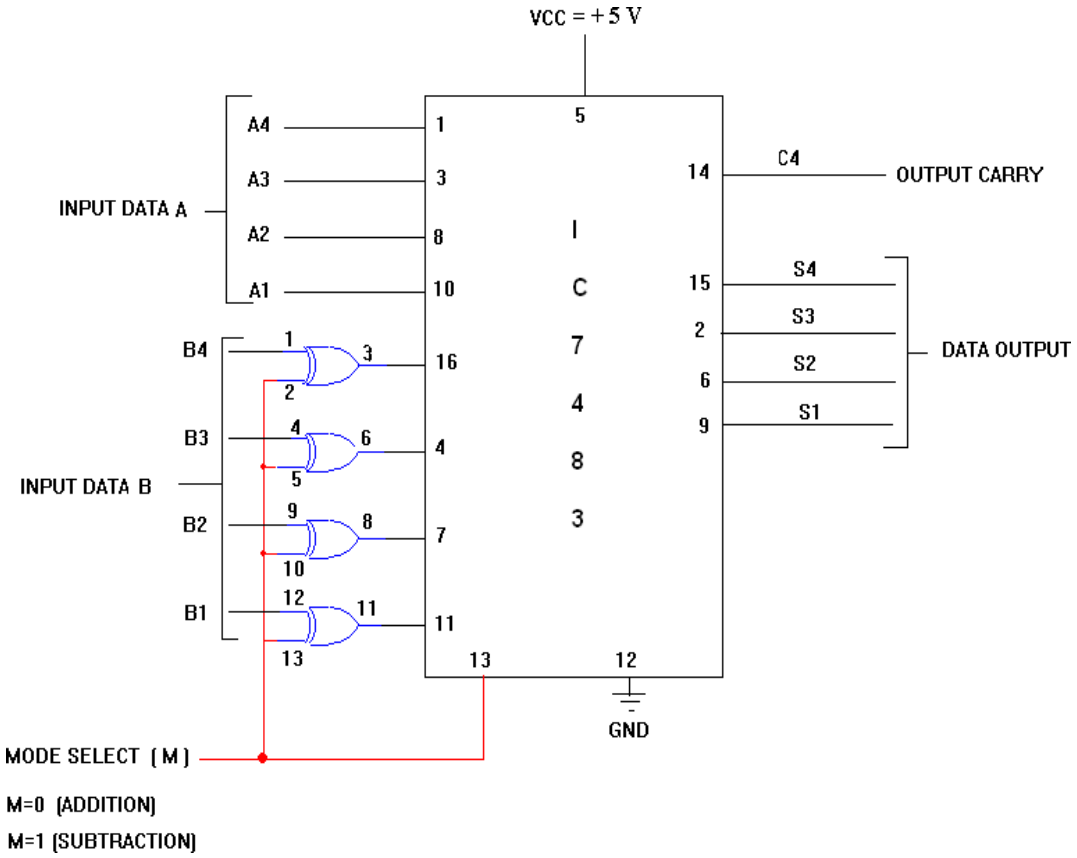
C_4	C_3	C_2	C_1	C_0	Carry
	A_3	A_2	A_1	A_0	Augend
	B_3	B_2	B_1	B_0	Addend
	S_3	S_2	S_1	S_0	Sum

4 BIT BINARY SUBTRACTOR:

The circuit for subtracting A-B consists of an adder with inverters, placed between each data input 'B' and the corresponding input of full adder. The input carry C_0 must be equal to 1 when performing subtraction.
During subtraction the Invert is held high, which complements all the B inputs to the full adders. Therefore, the B inputs to the full adders are in 1's complement form. As the Invert is also connected to the carry input of the first full-adder, and it is already high, this results in 1 being added to the 1's complement of the B input number. Thus, the resultant is the 2's complement of the B input.

Subtraction is effected by adding the 2's complement of the B input, so derived, to the A input as follows:

4-BIT BINARY ADDER/SUBTRACTOR



Minuend	A_3	A_2	A_1	A_0	
Subtrahend	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$	2's complement of B
Difference	S_3	S_2	S_1	S_0	

4 BIT BINARY ADDER/SUBTRACTOR:

The addition and subtraction operation can be combined into one circuit with one common binary adder. The mode input M controls the operation. When M=0, the circuit is adder circuit. When M=1, it becomes subtractor.

The 4 bit parallel binary adder/Subtractor performs both addition and subtraction. It has two 4 bits inputs A4A3A2A1 and B4B3B2B1. The Mode [M] control line is connected with C0. The EX-OR gates are used as controlled inverters.

When Mode [M] = 0 (Each X-OR gate receives input M and one of the inputs of B we have $B \oplus 0 = B$), the controlled inverter allows the addend B4 B3 B2 B1 without any change to the input of the full adder and carry input C0 become 0. Now the augends (A4 A3 A2 A1) and addend (B4B3B2B1) are added with C0=0and produce a sum and carry (C4).

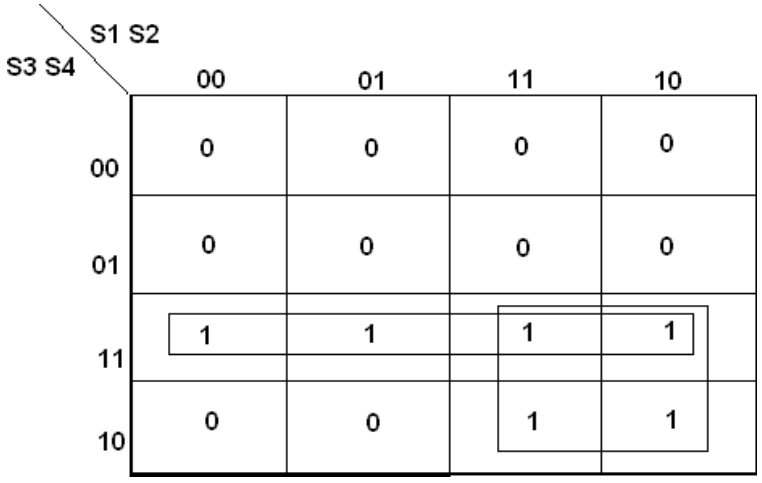
When Mode [M] =1 (When M=1, we have $B \oplus 1 = \overline{B}$ and C_0=1), the controlled inverter produces the 1's complement of the addend B4B3B2B1 and carry input C0 becomes 1. Since 1 is given to C0, it is added to the 1'complement of the addend producing 2's complement of the addend. Now the augends (A4 A3 A2 A1) and 2's complement of addend (B4 B3 B2 B1) are added to produce the sum i.e. the difference between augends and addend and carry(C4) i.e. the borrow output of 4 bit Subtractor.

BCD ADDER

TRUTH TABLE:

BCD SUM				CARRY
S4	**S3**	**S2**	**S1**	**C**
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

K- MAP Simplification



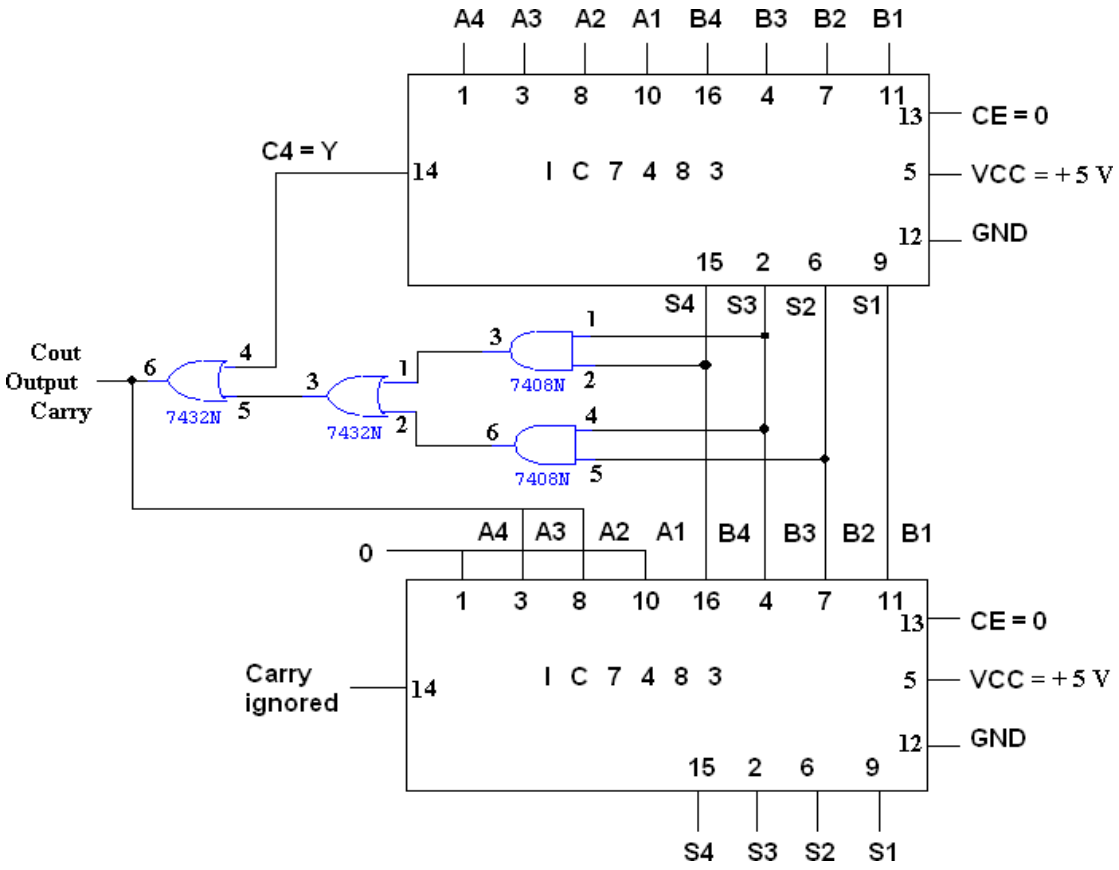
Y = S4 (S3 + S2)

4 BIT BCD ADDER:

Consider the arithmetic addition of two decimal digits in BCD, together with an input carry from a previous stage. Since each input digit does not exceed 9, the output sum cannot be greater than 19, the 1 in the sum being an input carry. The output of two decimal digits must be represented in BCD and should appear in the form listed in the columns.

ABCD adder that adds 2 BCD digits and produce a sum digit in BCD. The 2 decimal digits, together with the input carry, are first added in the top 4 bit adder to produce the binary sum.

LOGIC DIAGRAM:



BCD ADDER O/P VERIFICATION: Give Set of 4 bits for A & B and verify Output. Then check it manually.

APPLICATIONS: Digital computers and calculators consist of arithmetic and logic circuits. The basic blocks of arithmetic unit in digital computers are adders and subtractors.

PROCEDURE:

(i) Connections were given as per circuit diagram.

(ii) Logical inputs were given as per truth table

(iii) Observe the logical output and verify with the truth tables.

POST-LAB EXCERICE:

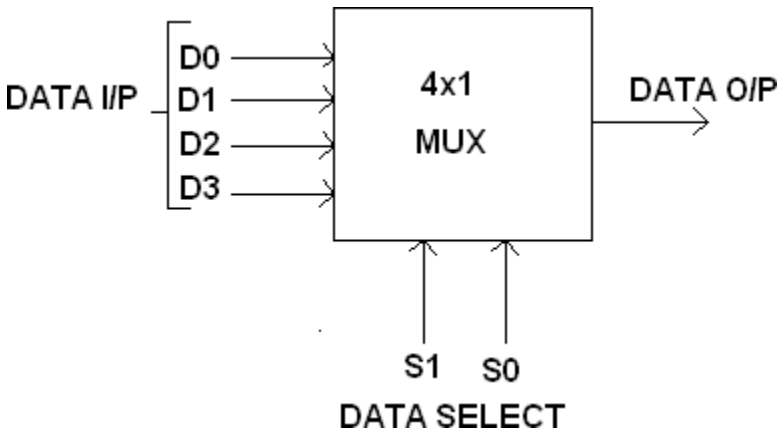
1. Compare serial adder & parallel adder?
2. What is BCD adder?
3. What are the advantages of complement arithmetic?
4. What is binary multiplier?
5. What is binary divider?

RESULT:

Thus the 4 bit binary Adder/Subtractor, BCD Adder using basic gates and IC7483 were constructed and their operations were verified.

4:1 MULTIPLEXER

BLOCK DIAGRAM:



FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

EXPT NO. : 14 DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER USING LOGIC GATES & STUDY OF IC 74150 AND IC 74154

AIM:

i. To design and implement 4 x 1 MUX and 1x 4 DEMUX using logic gates and study of IC 74150 and IC 74154.

ii. To implement the Boolean function F (A, B, C) = ∑m (1,3,4,7) with A as input.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	32

PRE-LAB EXCERICE:

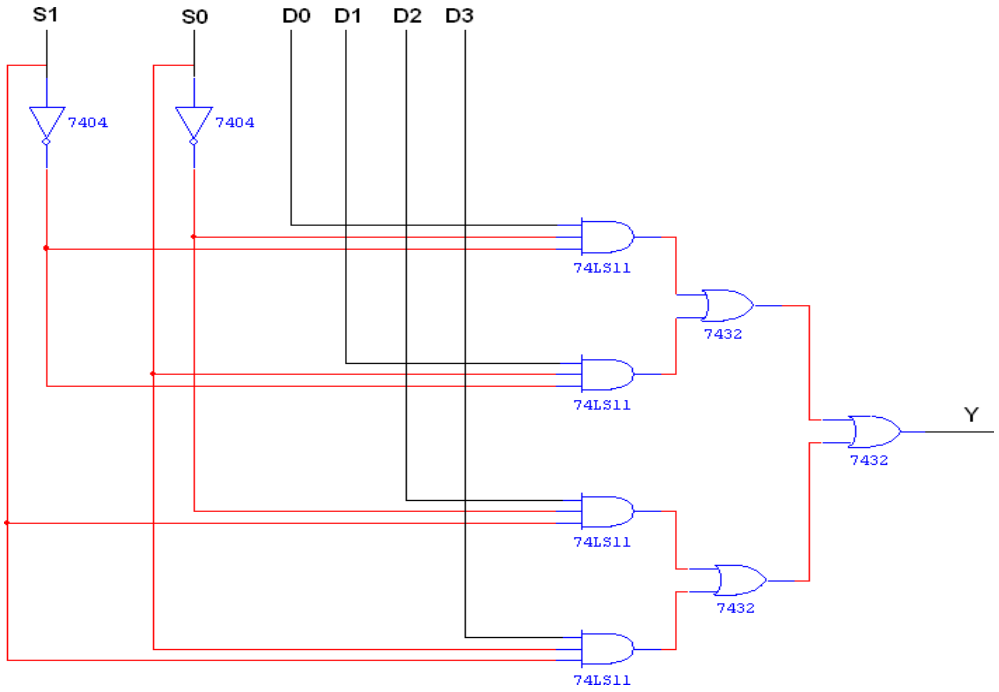
1. What is another name of multiplexer?
2. What is a four channel multiplexer?
3. What is the function of a multiplexer's select inputs?
4. What are the major applications of multiplexers?
5. Identify each MSI device? (a)74157 (b) 71151 (c) 74150

THEORY:

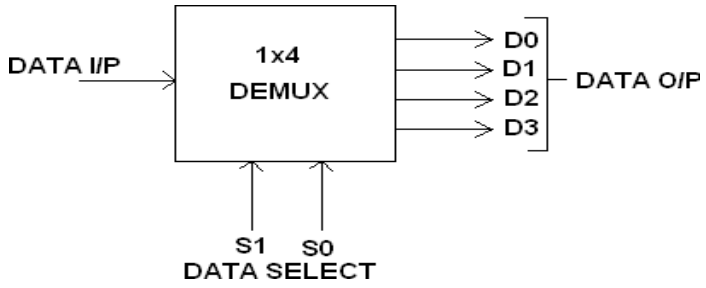
MULTIPLEXER:

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

LOGIC DIAGRAM FOR MULTIPLEXER:



BLOCK DIAGRAM:



FUNCTION TABLE:

S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

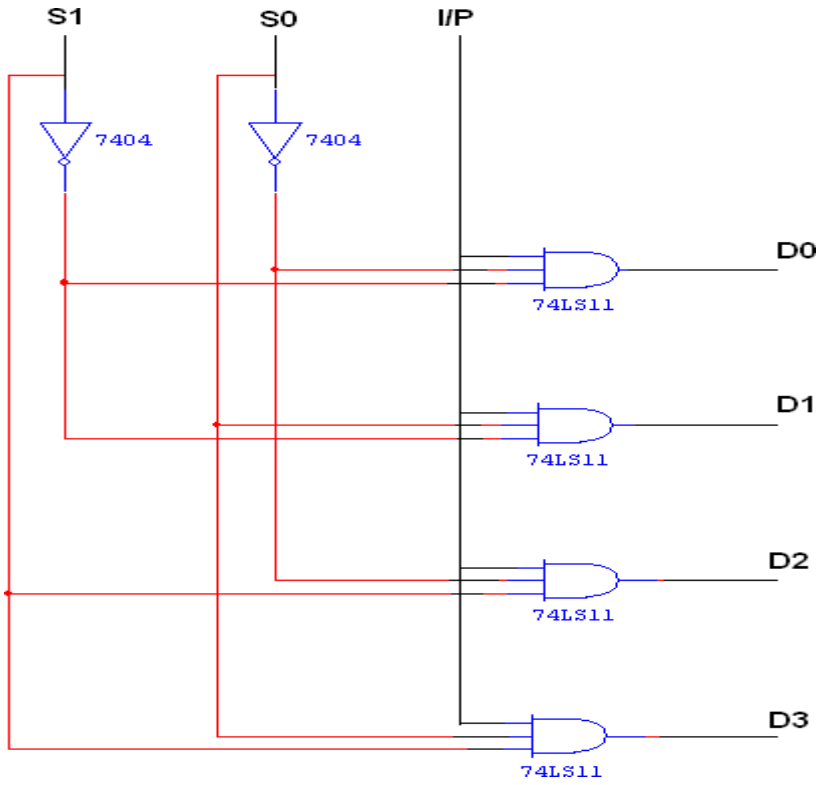
In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

1:4 DEMULTIPLEXER

TRUTH TABLE:

INPUT			OUTPUT			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

LOGIC DIAGRAM FOR DEMULTIPLEXER:



FUNCTION TABLE:

SI	SO	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

IMPLEMENTATION TABLE:

	D0	D1	D2	D3
$\overline{A}$	0	(1)	(4)	5
A	2	(3)	6	(7)
	0	1	$\overline{A}$	A

TRUTH TABLE:

F(A,B,C) = ∑m (1,3,4,7)

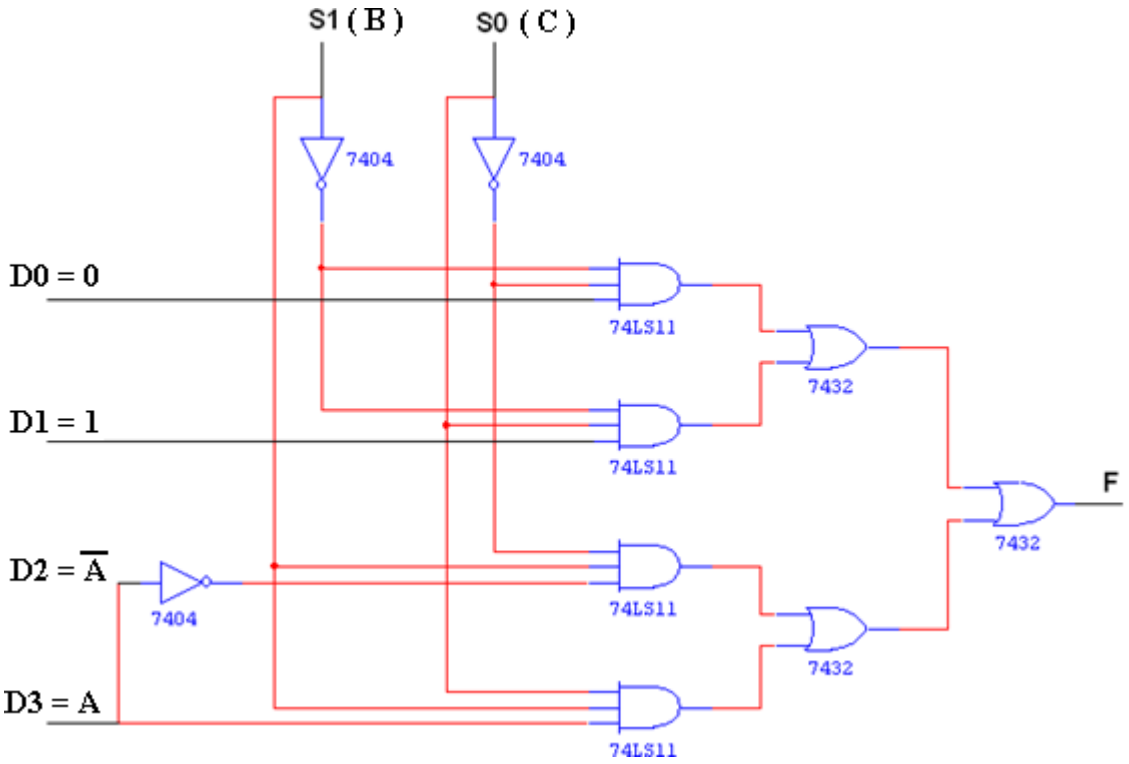
MIN TERM	DATA A	S1 B	S0 C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

MULTIPLEXER IMPLEMENTATIONS:

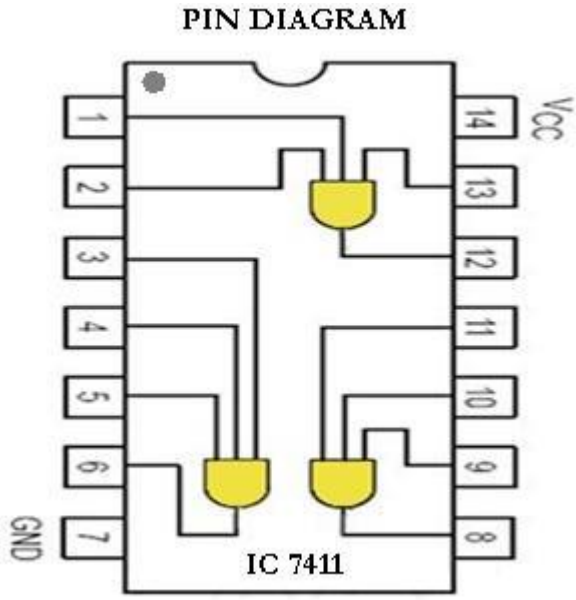
A digital multiplexer is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line. It is also called a data selector since it selects one of many inputs and steers the information to the output. It has several data input lines and a single output line. The selection of the particular input line is controlled by a set of selection lines.

General procedure for implementing any Boolean function of n variables with a multiplexer with n-1 selection inputs and 2^{n-1} data inputs, The Boolean function is first listed in atruth table. The first n-1 variables in the table are applied to the selection inputs of the multiplexer. For each combination of the selection variables we evaluate the output as function of the last variable. This function can be 0,1 the variable, or the complement of the variable. These values are then applied to the data inputs in the proper order.

LOGIC DIAGRAM USING BASIC GATES:



3 I/P AND GATE:



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

APPLICATION:

i. It can be used to implement logic functions in SOP form.

ii. It can be used to as a parallel to serial converter.

POST-LAB EXCERICE:

1. What is another name of demultiplexer?
2. What are the differences between a MUX & DEMUX?
3. How would you construct a logic function generator using multiplexers?
4. Draw logic symbol of a 4-to-1 multiplexer.
5. How many pins in IC74150?

RESULT:

Thus the multiplexer and De-multiplexer using logic gates were designed and implemented and studied about IC 74150 and IC 74154.

EXPT NO. : 15 DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER USING LOGIC GATES & STUDY OF IC 7445 AND IC 74147

AIM:

To design and implement encoder and decoder using logic gates and study of IC 7445 and IC 74147.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P NAND GATE	IC 7410	2
2.	OR GATE	IC 7432	3
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	27

PRE-LAB EXCERICE:

1. What is meant by encoder?
2. What is meant by decoder?
3. What is priority encoder?
4. What are the applications of encoder and decoder?
5. What is BCD to seven segment decoder?

THEORY:

ENCODER:

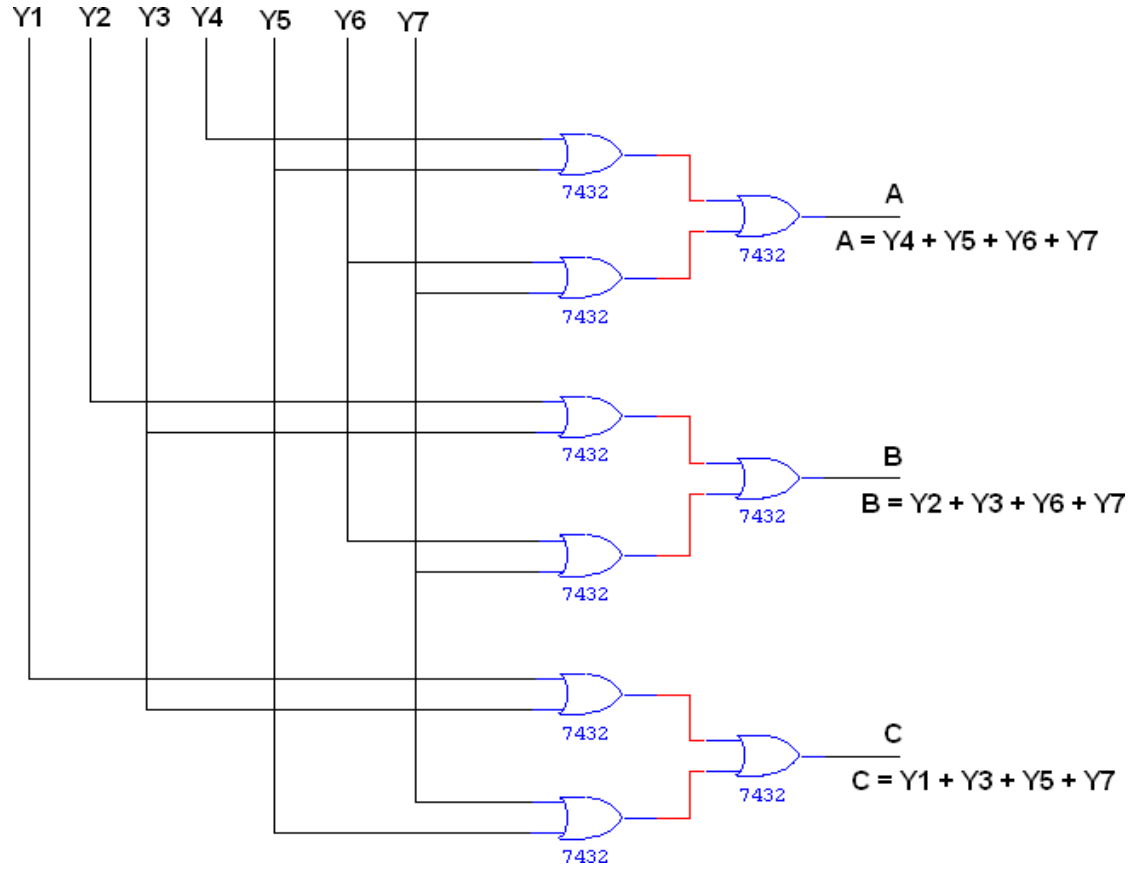
An encoder is a digital circuit that perform inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.

ENCODER

TRUTH TABLE:

INPUT								OUTPUT		
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

LOGIC DIAGRAM

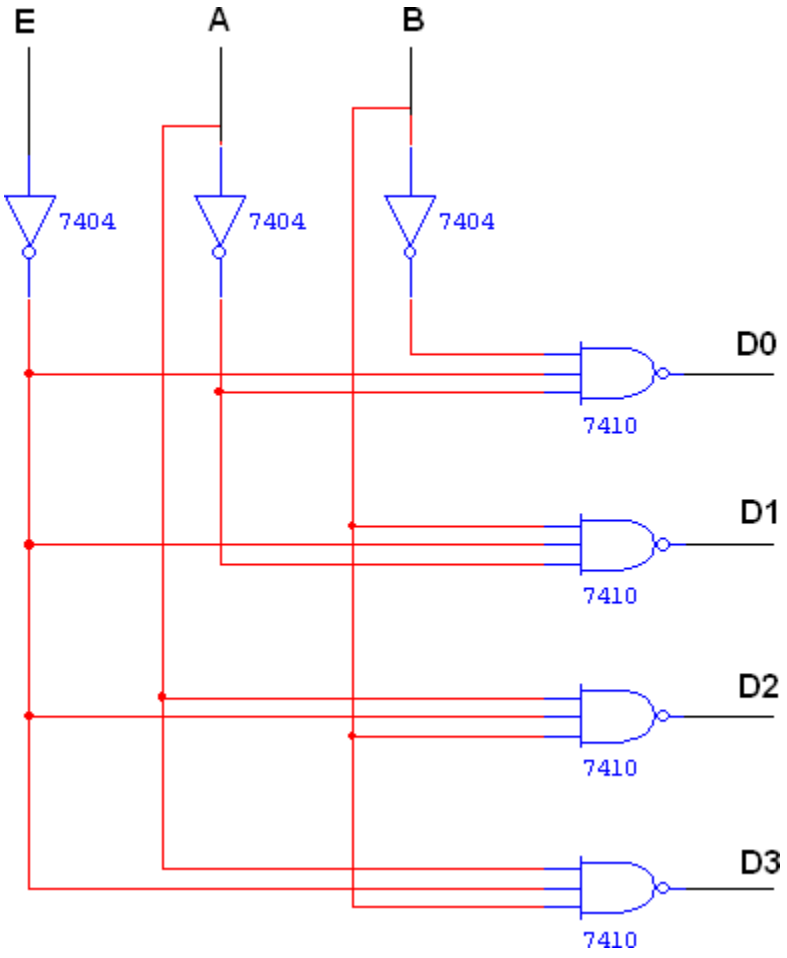


DECODER

TRUTH TABLE:

INPUT			OUTPUT			
E	**A**	**B**	**D0**	**D1**	**D2**	**D3**
1	0	0	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

LOGIC DIAGRAM:



DECODER:

A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

POST-LAB EXCERICE:

1. Can more than one decoder output be activated at one time? Justify your answer.
2. What is the function of a decoder's enable input(s)?
3. How does an encoder differ from decoder?
4. How does a priority encoder differ from an ordinary encoder?
5. What is decimal to BCD encoder?

RESULT:

Thus the encoder and decoder using logic gates was designed and implemented and studied about IC 7445 and IC 74147.

EXPT NO. : 16

Date:

CONSTRUCTION AND VERIFICATION OF 4 BIT RIPPLE COUNTER AND MOD 10/MOD 12 RIPPLE COUNTER

AIM:

To design and verify 4 bit ripple counter mod 10/ mod 12 ripple counter.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	JK FLIP FLOP	IC 7476	2
2.	NAND GATE	IC 7400	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	30

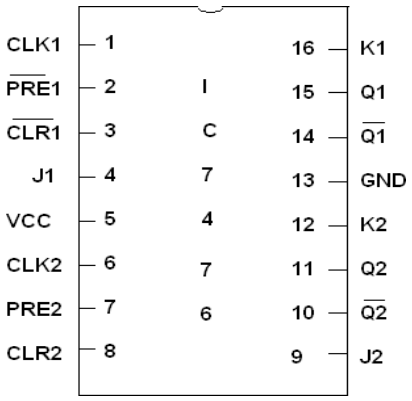
PRE-LAB EXCERICE:

1. What is counter?
2. What are the types of counter?
3. Distinguish between a ripple counter & a synchronous counter.
4. Define the modulus of a counter.
5. How is a modulus counter built using count reset?

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or Q output of previous stage. A soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

PIN DIAGRAM FOR IC 7476:

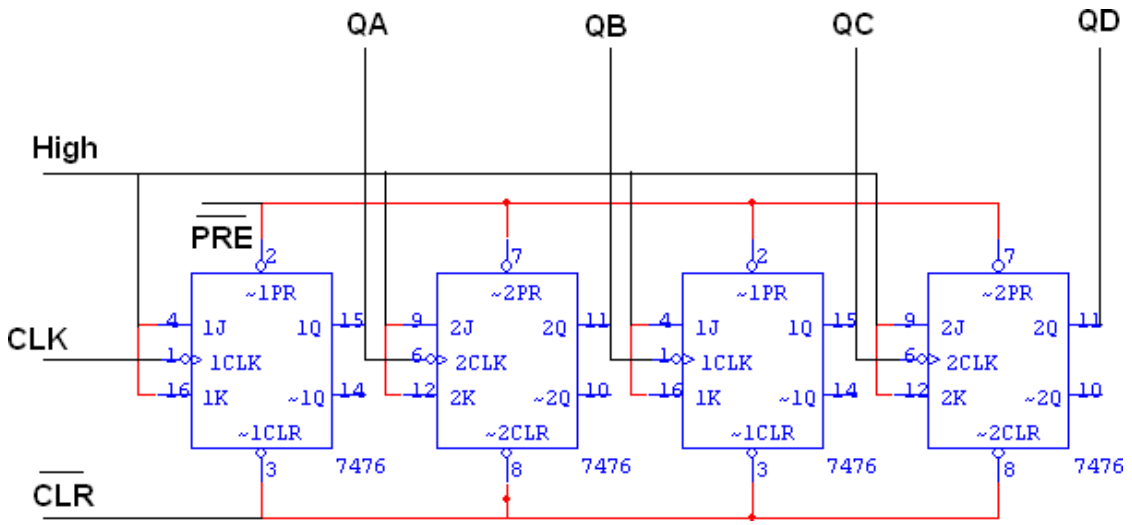


4 BIT RIPPLE COUNTER

TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

LOGIC DIAGRAM:



NOTE:

In 4 bit Ripple counter, Mod-10, and Mod-12 Ripple counter

Use One IC7476 for FF A & C and another One IC7476 for FF B & D.

MOD - 10 RIPPLE COUNTER

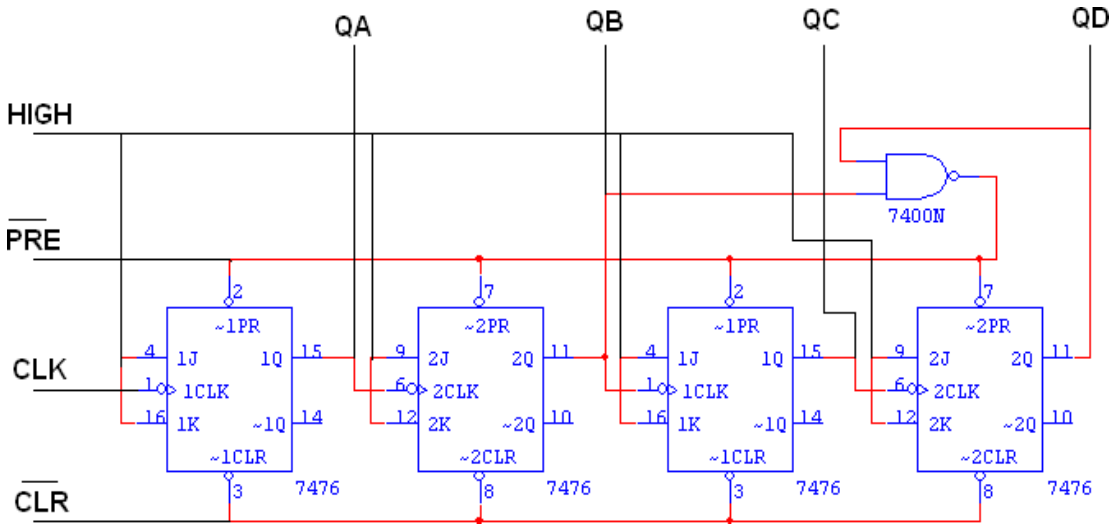
TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

LOGIC DIAGRAM:



MOD - 12 RIPPLE COUNTER

TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

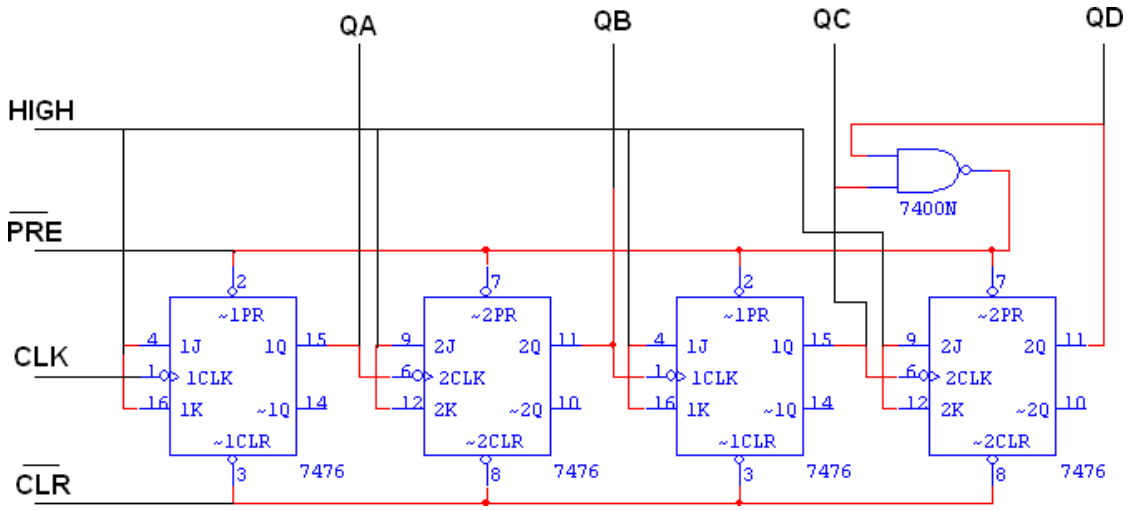
APPLICATIONS:

It is used as frequency divider in digital time pieces such as electronic digital clocks, automobile digital clock and frequency counters.

POST-LAB EXCERICE:

1. What is an in asynchronous sequential circuit?
2. What is a sequence generator?
3. What is an asynchronous decade counter?
4. Define synchronous counter.
5. What is Johnson counter?

LOGIC DIAGRAM:



RESULT:

Thus the 4 bit ripple counter and Mod-10 /Mod-12 ripple counter were constructed and their state tables were verified.

EXPT NO. : 17

Date:

DESIGN AND IMPLEMENTATION OF 3 BIT SYNCHRONOUS UP/DOWN COUNTER

AIM:

To design and implement 3 bit synchronous up/down counter.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	JK FLIP FLOP	IC 7476	2
2.	3 I/P AND GATE	IC 7411	1
3.	OR GATE	IC 7432	1
4.	XOR GATE	IC 7486	1
5.	NOT GATE	IC 7404	1
6.	IC TRAINER KIT	-	1
7.	PATCH CORDS	-	35

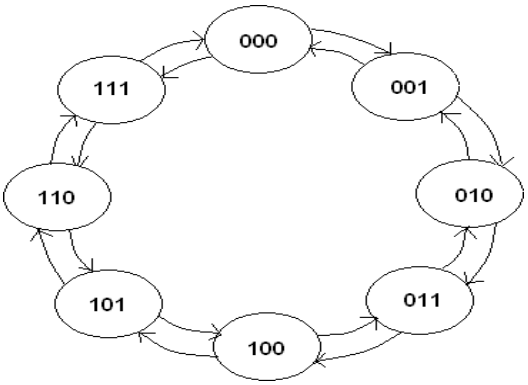
PRE-LAB EXCERICE:

1. Define up-down counter.
2. Define decade, BCD & modulo counter.
3. What is another name of shift counter?
4. What are the advantages of synchronous counter over ripple counter?
5. What are the differences between synchronous counter & asynchronous counter?

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

STATE DIAGRAM:



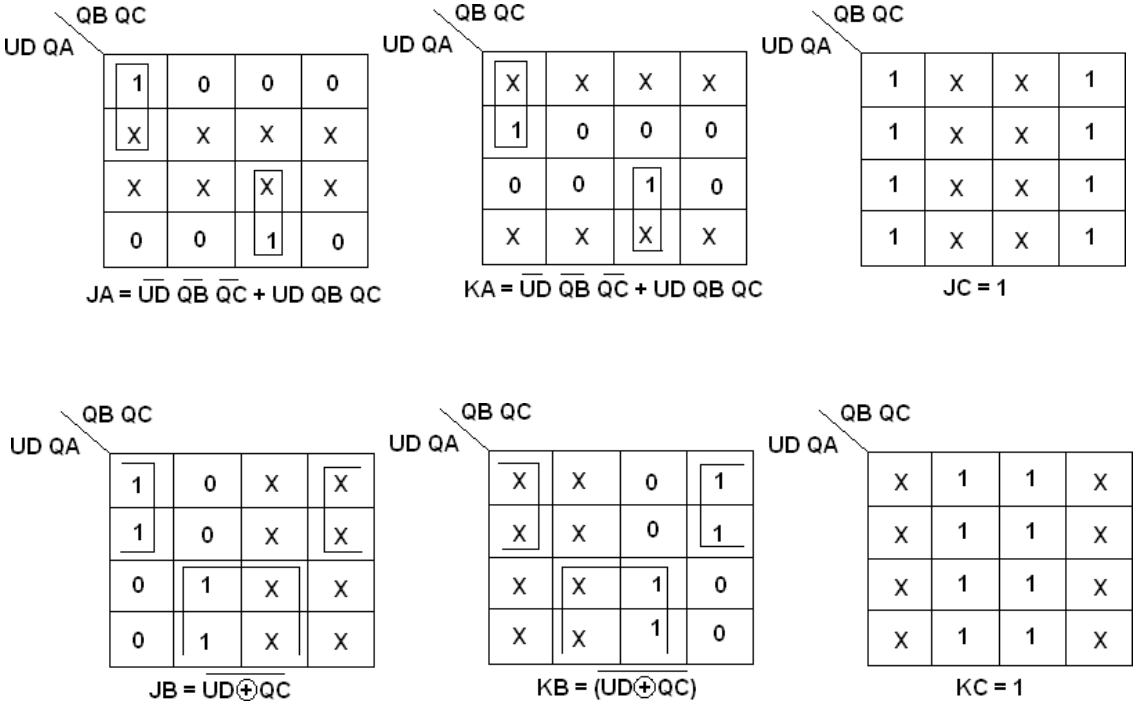
CHARACTERISTICS TABLE:

Q	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

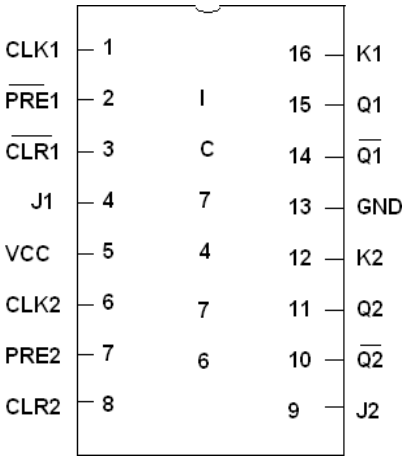
TRUTH TABLE:

Input Up/Down	Present State			Next State			A		B		C	
	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	1	1	1	X	1	X	1	X
0	1	1	1	1	1	0	X	0	X	0	X	1
0	1	1	0	1	0	1	X	0	X	1	1	X
0	1	0	1	1	0	0	X	0	0	X	X	1
0	1	0	0	0	1	1	X	1	1	X	1	X
0	0	1	1	0	1	0	0	X	X	0	X	1
0	0	1	0	0	0	1	0	X	X	1	1	X
0	0	0	1	0	0	0	0	X	0	X	X	1
1	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	0	0	X	1	X	X	1
1	0	1	0	0	1	1	0	X	X	0	1	X
1	0	1	1	1	0	0	1	X	X	1	X	1
1	1	0	0	1	0	1	X	0	0	X	1	X
1	1	0	1	1	1	0	X	0	1	X	X	1
1	1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	1	0	0	0	X	1	X	1	X	1

K MAP



PIN DIAGRAM FOR IC 7476:



PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

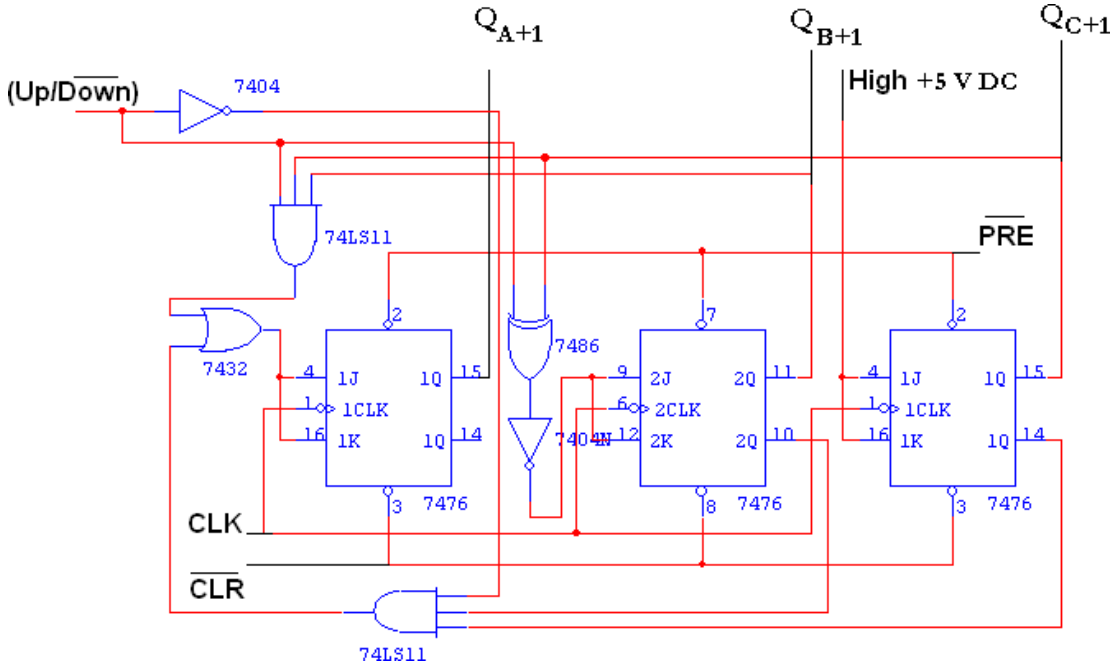
APPLICATIONS:

It is used as frequency dividers in digital timepieces such as electronic digital clocks, automobile digital clocks and frequency counters.

POST-LAB EXCERICE:

1. What is another name of synchronous counter?
2. What is the maximum frequency of operation of synchronous counter?
3. What is pre-settable (programmable) counter?
4. What is excitation table?
5. How the counter can be use in digital clock?

LOGIC DIAGRAM:



RESULT:

Thus the 3 bit synchronous up-down counter was designed, implemented and their state table was verified.

EXPT. NO: 18

Date:

DESING & IMPLEMENTATION OF 2 BIT MAGNITUDE COMPARATOR

Aim:

To design and implement a 2bit magnitude comparator using logic gates

COMPONENTS REQUIRED:

Sl. No.	COMPONENT	SPECIFICATION	QTY.
1.	EX-NOR	IC 747266	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	AND GATE	IC7408	1
5.	IC TRAINER KIT	-	1
6.	PATCH CORDS	-	40

PRE-LAB EXCERICE:

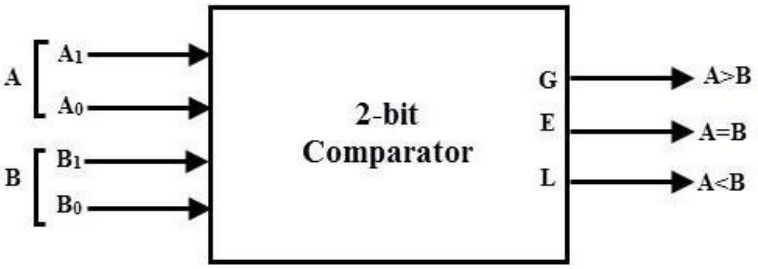
1. What is magnitude comparator?
2. Define most significant bit.
3. Why magnitude comparator is needed?
4. Which gate is a basic comparator?
5. How many inputs are required for a digital comparator?

THEORY:

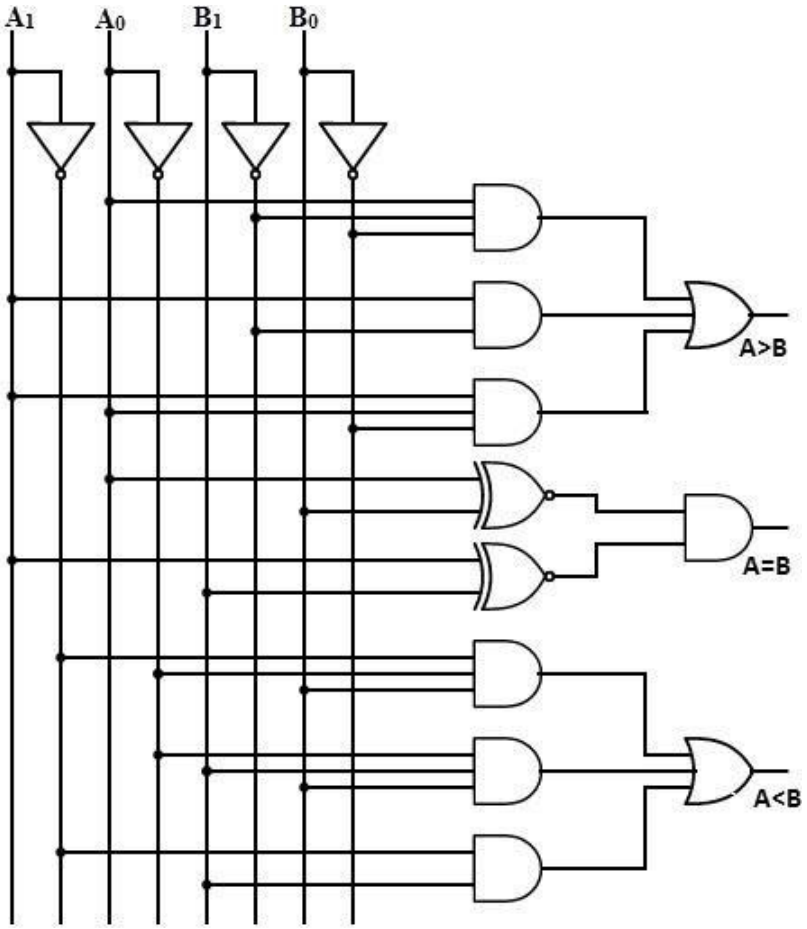
A 2-bit comparator compares two binary numbers, each of two bits and produces their relation such as one number is equal or greater than or less than the other. The figure below shows the block diagram of a two-bit comparator which has four inputs and three outputs.

The first number A is designated as A = A1A0 and the second number is designated as B = B1B0. This comparator produces three outputs as G (G = 1 if A>B), E (E = 1, if A = B) and L (L = 1 if A<B).

BLOCK DIAGRAM:



LOGIC DIAGRAM:



TRUTH TABLE:

Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

K-MAP:

A>B

A_1A_0 \ B_1B_0	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

A=B

A_1A_0 \ B_1B_0	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

$$A>B:\ G = A0\,\overline{B1}\ \ \overline{B0} + A1\,\overline{B1} + A1\ A0\,\overline{B0}$$

$$A = B:\ E = \overline{A1}\ \ \overline{A0}\ \overline{B1}\ \ \overline{B0} + \overline{A1}\ A0\ \ \overline{B1}\ B0 + A1\ A0\ B1\ B0 + A1\,\overline{A0}\ B1\ \overline{B0}$$

$$= \overline{A1}\ \ \overline{B1}\ (\overline{A0}\ \ \overline{B0} + A0\ B0) + A1\ B1\ (A0\ B0 + \overline{A0}\ \ \overline{B0}\ )$$

$$= (A0\ B0 + \overline{A0}\ \ \overline{B0})\ (A1\ B1 + \ \overline{A1}\ \ \overline{B1})$$

$$= (A0\ \text{Ex-NOR}\ B0)\ (A1\ \text{Ex-NOR}\ B1)$$

$$A < B:\ L = \overline{A1}\ \ B1 + \overline{A0}\ B1\ B0 + \overline{A1}\ \ \overline{A0}\ B0$$

By using above obtained Boolean equation for each output, the logic diagram can be implemented by using NOT gates, AND gates, OR gates and Ex-NOR gates.

POST- LAB EXERCISE:

1. If two numbers are not equal then binary variable will be….?
2. What is inequality?
3. Tell the applications of magnitude comparator.
4. How many types of digital comparators are there?
5. TTL 74LS85 is which type of magnitude comparator?

Result:

Thus the 2-bit magnitude comparator was designed and the values are compared.