SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

III SEMESTER

1906306–DIGITAL FUNDAMENTALS AND COMMUNICATION

(Common to Department of Cyber Security)

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Prepared by

Dr. K. Ayyar, Associate Professor / EIE

Ms. V. Mangaiyarkarasi, Assistant Professor (Sr.Gr) / EIE

Ms. K. Rathna Priya, Assistant Professor (O. G) / EIE

Ms. M.Ramjan-Begum, Assistant Professor (O.G) / EIE

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Department of Computer Science and Engineering

SUBJECT: 1906306–DIGITAL FUNDAMENTALS AND COMMUNICATION

SEM / YEAR: III / II

UNIT -1BOOLEAN ALGEBRA AND LOGIC GATES			
Review of Number Systems– Boolean Algebra and Theorems – Boolean Functions – Simplification of Boolean Functions using Karnaugh Map– Logic Gates – NAND and NOR Implementations.			
PART – A			
Q.No.	**Questions**	**BT Level**	**Competence**
1.	Classify the different types of number system.	**BLT-4**	Analyze
2.	Examine binary number system.	**BLT-3**	Apply
3.	Transform the given binary number to hexadecimal $(111.110110)_2$.	**BLT-5**	Evaluate
4.	Convert the decimal number $(23)_{10}$ to equivalent binary number.	**BLT-2**	Understand
5.	Find the decimal equivalent of $(346)_7$.	**BLT-4**	Analyze
6.	Convert the following number from one base to octal. $(69.363)_7$.	**BLT-2**	Understand
7.	Convert $(627)_8$ to binary.	**BLT-2**	Understand
8.	Convert 0.13567 decimal number to its hexadecimal equivalent.	**BLT-2**	Understand
9.	Convert $(62.375)_{10}$ to binary number.	**BLT-2**	Understand
10.	State DE Morgan's theorem.	**BLT-1**	Remember
11.	Construct OR Gate using only NAND Gate.	**BLT-6**	Create
12.	Using DE Morgan's theorem, find (a) $\overline{A+B+C} = \bar{A}\bar{B}\bar{C}$ (b) $\overline{A(B+C)}$	**BLT-4**	Analyze
13.	State the associative law of Boolean algebra.	**BLT-1**	Remember
14.	Write down the truth table of XOR gate.	**BLT-5**	Evaluate
15.	Name the two canonical forms for Boolean algebra.	**BLT-1**	Remember
16.	What is prime implicant?	**BLT-1**	Remember
17.	What are the advantages of K-map?	**BLT-1**	Remember
18.	Find complements for the function *F=(xy+y'z+xz)x*	**BLT-4**	Analyze
19.	Simplify (x+y)(x+y') to a minimum number of literals.	**BLT-3**	Apply
20.	Find the value of x=$\bar{A}BC$ ($\overline{A+B}$) if A=0, B=1, C=1 and D=1	**BLT-6**	Create
21.	Find the minterm expansion of xy + yz + xy'z	**BLT-5**	Evaluate
22.	State Duality principle.	**BLT-1**	Remember
23.	Simplify the function F = $\sum(1,3,6,7)$ using K – map.	**BLT-3**	Apply
24.	Simplify the function F(A,B,C) = $\sum(0,2,3,4,6,7)$ using K –	**BLT-3**	Apply

	map.		
	PART B		
1.	Convert the following decimal numbers to binary, octal and hexadecimal. **(i)** $(455)_{10}$ **(6)** **(ii)** $(256.22)_{10}$ **(7)**	**BLT-1**	Remember
2.	Convert the following binary number to decimal, octal and hexadecimal. **(i)** $(11101)_2$ **(6)** **(ii)** $(100010.011)_2$ **(7)**	**BLT-1**	Remember
3.	Convert the following hexadecimal number to decimal, binary and octal. **(i)** $(1D)_{16}$ **(6)** **(ii)** $(22.6)_{16}$ **(7)**	**BLT-1**	Remember
4.	Convert the expression in standard POS form **(i)** f (A, B, C) = (A + C) . B **(6)** **(ii)** f(A, B, C) = (A + B) . (A + C) **(7)**	**BLT-1**	Remember
5.	Express the Boolean function F = XY + $\bar{X}$Z in a product of maxterm form and also to standard POS. **(13)**	**BLT-3**	Apply
6.	Examine the following SOP expression to an equivalent POS expression $\bar{A}\bar{B}\bar{C}$ + $\bar{A}$B$\bar{C}$ + $\bar{A}$BC + A$\bar{B}$C + ABC. **(13)**	**BLT-3**	Apply
7.	Minimize the given expression using F = X$\bar{Y}$Z + $\bar{X}\bar{Y}$Z + $\bar{X}$YZ + X$\bar{Y}\bar{Z}$ + $\bar{X}\bar{Y}\bar{Z}$ **(i)** K-map **(6)** **(ii)** Boolean laws **(7)**	**BLT-4**	Analyze
8.	Simplify the following expression using K – Map method and draw its logic diagram. Y = $\sum m$ (7,9,10,11,12,13,14,15) **(13)**	**BLT-2**	Understand
9.	Simplify the Boolean expression using K – Map in POS form. Y(A,B,C) = (A + $\bar{B}$ + C) ($\bar{A}$ + $\bar{B}$ + C) (A + $\bar{B}$ + $\bar{C}$) ($\bar{A}$ + $\bar{B}$ + $\bar{C}$) **(13)**	**BLT-2**	Understand
10.	Simplify the Boolean expression using K- Map Y (A, B, C) = ($\bar{A}$ + B) . (A + $\bar{C}$) **(13)**	**BLT-2**	Understand
11.	Minimize the Boolean expression using K – Map. Also implement the circuit using logic gates. Y (A, B, C, D) = $\prod M$ (0, 1, 4, 5, 6, 8, 9, 10, 13, 14, 15) **(13)**	**BLT-4**	Analyze
12.	Simplify the following expression using K- Map Y (A, B, C) = $\sum m$ (0, 1, 3, 5, 6) + d (2, 4) **(13)**	**BLT-2**	Understand
13.	Implement the following Boolean function with NAND – NAND logic. F = AB + ABC + $\bar{A}$BC + A$\bar{B}$ + D **(13)**	**BLT-6**	Create
14.	Realize the following Boolean function with only NOR gates. Y = AC + BC + AB + D **(13)**	**BLT-3**	Apply
15.	Perform the following Boolean function with NOR – NOR logic F = ($\bar{A}$ + B) C . **(13)**	**BLT-3**	Apply

16.	Deduce and implement the following POS function using NOR gates. f (A, B, C, D) = $\prod M$ (0, 1, 2, 3, 12, 13, 14, 15) **(13)**	**BLT-5**	Evaluate
17.	Deduce and implement the following SOP function using NOR gates. f (A, B, C, D) = $\sum m$ (0, 1, 4, 5, 10, 11, 14, 15) **(13)**	**BLT-3**	Apply
	PART C		
1.	Transform the following octal number to decimal , binary and hexadecimal **(i)** $(35)_8$ **(8)** **(ii)** $(42.3)_8$ **(7)**	**BLT-5**	Evaluate
2.	Deduce the following Boolean expression Y(A, B, C, D) = $\sum m$ (1, 2, 5, 6, 8, 9) **(15)**	**BLT-5**	Evaluate
3.	Realize and Reduce the following expression : F (A, B, C, D) = $\sum m$ (0, 7, 8, 9, 10, 12) + d (2, 5, 13) **(15)**	**BLT-5**	Evaluate
4.	Truncate the given Boolean expression : Y(A,B,C,D) = $\prod M$(4, 5, 7, 8, 12) . d (1, 2, 3, 9, 11, 14) **(15)**	**BLT-6**	Create
5.	Compile the following Boolean function with NAND – NAND logic F = (A, B, C) = $\sum m$ (0, 1, 3, 5, 6, 7) **(15)**	**BLT-6**	Create

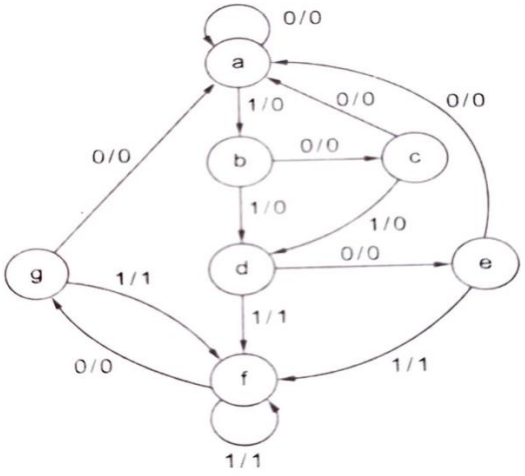
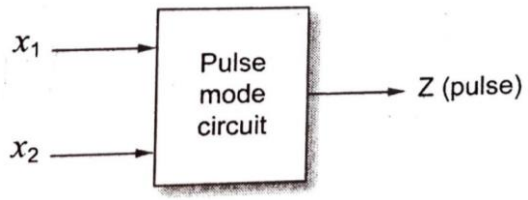
UNIT – II COMBINATIONAL LOGIC			
Combinational Circuits – Analysis and Design Procedures – Circuits for Arithmetic Operations, Code Conversion – Decoders and Encoders – Multiplexers and Demultiplexers – Introduction to HDL – HDL Models of Combinational circuits.			
PART – A			
Q.No.	**Questions**	**BT Level**	**Competence**
1.	Mention some of the combinational circuits.	**BLT-3**	Apply
2.	List out various applications of multiplexer.	**BLT-2**	Understand
3.	What is meant by look ahead carry?	**BLT-1**	Remember
4.	Give the logical expression for sum output and carry output of a full adder.	**BLT-2**	Understand
5.	Design a half subtractor using basic gate.	**BLT-5**	Evaluate
6.	Draw a logic diagram of a 4 line to 1 line multiplexer.	**BLT-2**	Understand
7.	Draw the logic diagram of a serial adder.	**BLT-2**	Understand
8.	Design a three bit even parity generator.	**BLT-5**	Evaluate
9.	Develop a single bit magnitude comparator two words A and B.	**BLT-6**	Create
10.	What is a combinational circuit? Give an example.	**BLT-1**	Remember
11.	Implement the following function using suitable multiplexer. F(x, y, z)=∑m(0, 2, 5, 7)	**BLT-3**	Apply
12.	Point out the design procedure for combinational circuits.	**BLT-4**	Analyze
13.	Define half adder and full adder.	**BLT-1**	Remember
14.	Which adder inspect carry look ahead logic to ensure that carry propagation between subsequent stages of addition does not limit addition speed?	**BLT-3**	Apply

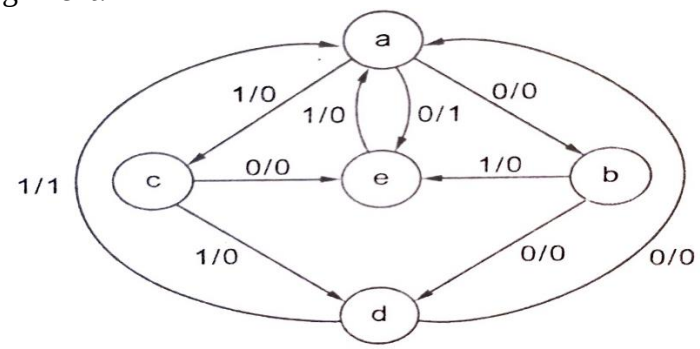
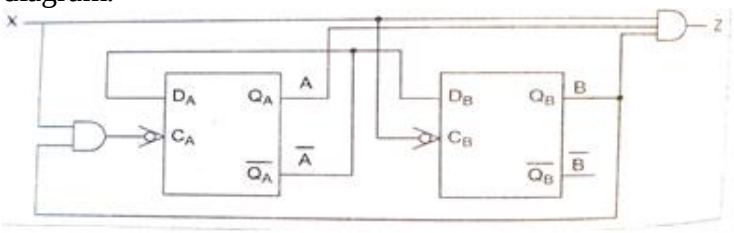
15.	What is BCD adder?	**BLT-1**	Remember
16.	Point out the applications of multiplexer.	**BLT-4**	Analyze
17.	What is DEMUX?	**BLT-1**	Remember
18.	Assess decoder.	**BLT-4**	Analyze
19.	What is encoder?	**BLT-1**	Remember
20.	Give the applications of DEMUX.	**BLT-2**	Understand
21.	Prioritize the operator precedence of Verilog HDL.	**BLT-6**	Create
22.	Compare decoder and demultiplexer.	**BLT-4**	Analyze
23.	Examine logic synthesis and simulation.	**BLT-3**	Apply
24.	Evaluate the function of an enable input on a multiplexer.	**BLT-5**	Evaluate
	PART B		
1.	Write concise notes on **(i)** Combinational logic **(6)** **(ii)** Design procedure **(7)**	**BLT-1**	Remember
2.	Describe the following combinational circuits in detail **(i)** Half adder **(6)** **(ii)** Full adder **(7)**	**BLT-2**	Understand
3.	Analyze and describe the following in detail **(i)** Performs subtraction on 2 binary inputs and produce two binary outputs as a difference and a borrow. **(6)** **(ii)** Performs subtraction on 3 binary inputs and produce output as a difference and a carry bit. **(7)**	**BLT-4**	Analyze
4.	Explain 4 : 1 multiplexer in detail with truth table and sketch the logic diagram. **(13)**	**BLT-3**	Apply
5.	Design a suitable multiplexer which has 3 selection lines, eight input lines and one output. Verify with truth table and logic diagram. **(13)**	**BLT-6**	Create
6.	Implement the Boolean function using 4 : 1 multiplexer F (A, B, C) = $\sum(1, 3, 6, 7)$ **(13)**	**BLT-3**	Apply
7.	Realize the following Boolean expression using a suitable multiplexer F (A,B,C,D) = $\sum(0, 1, 3, 5, 7, 9, 11, 14, 15)$ **(13)**	**BLT-5**	Evaluate
8.	Discuss in detail about 1 to 4 Demultiplexer which performs conversion from serial to parallel. **(13)**	**BLT-1**	Remember
9.	Describe the combinational circuit which has single data input and 8 data outputs. Verify with truth table and logic diagram. **(13)**	**BLT-2**	Understand
10.	Explain the operation of Encoder with an Example. **(13)**	**BLT-2**	Understand
11.	Design a Binary to BCD converters. Also implement the logic diagram. **(13)**	**BLT-6**	Create
12.	Discuss in detail about 4 bit BCD to Excess - 3 code converters with K Map Simplification and logic diagram. **(13)**	**BLT-1**	Remember
13.	Convert Excess 3 code to BCD code using K Map Simplification and verify with logic diagram. **(13)**	**BLT-4**	Analyze
14.	Explain in detail about Binary to Gray code converters. **(13)**	**BLT-2**	Understand
15.	Why Gray codes are used in rotary and optical encoders? Explain in detail about Gray code to Binary code converters. **(13)**	**BLT-4**	Analyze

16.	Enumerate in detail about Hardware description language (HDL) which is used to describe the structure and behavior of electronic digital circuits. **(13)**	**BLT-1**	Remember
17.	Explain in detail about Operators in Verilog HDL. Write a Verilog code for half adder circuit. **(13)**	**BLT-3**	Apply
	PART C		
1.	Design a combinational logic circuit with three input variable A,B,C that will produce a output as 1 whenever the variable A or C , both A and C are logic 1. **(15)**	**BLT-5**	Evaluate
2.	Realize the given Boolean function using two 4 : 1 MUX F (A, B, C, D) = $\sum m$ (0, 1, 2, 4, 6, 9, 12, 14) **(15)**	**BLT-5**	Evaluate
3.	Develop a combinational circuit that converts binary information from n input lines to a maximum 2^n unique output lines. Each output line will be activated for only one of the possible combination of inputs. **(15)**	**BLT-6**	Create
4.	Consider the decoder which as three inputs (A, B, C) and eight outputs (Y_0 - Y_7). Design the 3 to 8 line decoder. **(15)**	**BLT-6**	Create
5.	Design a BCD to Binary converters using K map and prove it with logic model. **(15)**	**BLT-6**	Create

UNIT III SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL LOGIC			
Sequential Circuits – Latches and Flip Flops – Analysis and Design Procedures – State Reduction and State Assignment –HDL for Sequential Logic Circuits. Analysis and Design of Asynchronous Sequential Circuits– Hazards.			
PART – A			
Q.No.	**Questions**	**BT Level**	**Competence**
1.	Define latches.	**BLT-1**	Remember
2.	Examine the characteristics equation of JK flipflop.	**BLT-3**	Apply
3.	Convert D flipflop to T flipflop.	**BLT-4**	Analyze
4.	Distinguish between combinational circuits and sequential circuits.	**BLT-3**	Apply
5.	Classify sequential circuits.	**BLT-3**	Apply
6.	Distinguish between synchronous sequential circuits and asynchronous sequential circuits.	**BLT-3**	Apply
7.	Sketch T flip flop.	**BLT-2**	Understand
8.	Assess the need for state assignment.	**BLT-4**	Analyze
9.	What is Excitation table?	**BLT-1**	Remember
10.	What is race around condition in flip flop?	**BLT-1**	Remember
11.	Outline sequential circuit with an example.	**BLT-2**	Understand
12.	List the different types of flipflop.	**BLT-2**	Understand
13.	Which flip flop is preferred to design a binary counter?	**BLT-5**	Evaluate

14.	Point out few applications of flip flop.	**BLT-4**	Analyze
15.	Infer the output of SR flip flop When the set is disabled and reset is enabled**.**	**BLT-6**	Create
16.	List the two types of asynchronous sequential circuits.	**BLT-2**	Understand
17.	Differentiate fundamental mode and pulse mode asynchronous sequential circuits.	**BLT-2**	Understand
18.	Interpret the main cause of HAZARDS in logic networks.	**BLT-5**	Evaluate
19.	What is fundamental mode circuit?	**BLT-1**	Remember
20.	What are pulse mode circuits?	**BLT-1**	Remember
21.	Formulate the steps for the design of asynchronous sequential circuit in pulse mode?	**BLT-6**	Create
22.	Analyze the ways in which hazards get eliminated.	**BLT-4**	Analyze
23.	What is static hazards?	**BLT-1**	Remember
24.	How the race around condition can be avoided in JK flipflop?	**BLT-5**	Evaluate
	PART B		
1.	With the help of block diagram, discuss Sequential circuits. Compare combinational circuits and Sequential circuits and also explain its classification. **(13)**	**BLT-2**	Understand
2.	Construct Latches using cross coupled NOR gates and cross coupled NAND gates and explain in detail. **(13)**	**BLT-3**	Apply
3.	Write down the characteristic equation and explain the operation of JK flip flop. **(13)**	**BLT-3**	Apply
4.	Assess the truth table of clocked SR flip flop with logic diagram. **(13)**	**BLT-4**	Analyze
5.	Realize the logic diagram of D-FF using NAND gates and explain. **(13)**	**BLT-5**	Evaluate
6.	How will you convert the following flip flop? (i) Convert JK flip flop to SR flip flop (ii) Convert D flip flop to JK flip flop (iii)Convert T flip flop to SR flip flop **(13)**	**BLT-5**	Evaluate
7.	Explain the working of T flip flop in detail. Construct T flip flop using JK flip flop. **(13)**	**BLT-1**	Remember
8.	Examine the sequential operation of edge triggered JK flip flop for the following cases (i) If J=0 and K=0 (ii) If J=0 and K=1 (iii)If J=1 and K=0 (iv)If J=1 and K=1 **(13)**	**BLT-3**	Apply
9.	How does State minimization or state reduction techniques help sequential circuits? Explain in detail. **(13)**	**BLT-4**	Analyze
10.	Elucidate the process of assigning binary values to the states of a sequential machine with the necessary rules, state diagrams and truth tables. **(13)**	**BLT-1**	Remember

11.	Design a sequential circuit for a given state diagram, use state reduction if necessary and also use D - flip-flop.  **(13)**	**BLT-6**	Create
12.	Illustrate pulse mode asynchronous sequential circuit with state variable transition table and timing diagram. **(13)**	**BLT-2**	Understand
13.	Design an asynchronous sequential circuit whose output respond for every even numbered clock pulse. **(13)**	**BLT-6**	Create
14.	Write concise notes in detail about **(i)** Hazards **(6)** **(ii)** Dynamic Hazards **(7)**	**BLT-1**	Remember
15.	Check whether the following expression contains a hazard or not. F(A,B,C,D) = $\bar{A}\bar{B}$D + $\bar{A}$BC + ABD. **(13)**	**BLT-1**	Remember
16.	Describe the essential hazards that could occur in asynchronous sequential circuit and explain in detail. **(13)**	**BLT-2**	Understand
17.	Give the hazard free realization for the following Boolean function. **(i)** F(A,B,C,D) = $\sum m$ (0, 1, 5, 6, 7, 9, 11) **(6)** **(ii)** F(W,X,Y,Z) = $\sum m$ (0, 2, 6, 7, 8, 10, 12) **(7)**	**BLT-2**	Understand
	PART C		
1.	Formulate a flip flop using NAND gates in which clock signal is directly connected to the JK flip flop and it is connected through inverter to the SR flip flop. Explain with neat block diagrams, timing diagram and logic diagrams. **(15)**	**BLT-5**	Evaluate
2.	Design a pulse mode circuit having two input lines x_1 and x_2 and one output line Z as shown in fig. The circuit should produce an output pulse to coincide with the last input pulse in the sequence $x_1 - x_2 - x_2$. No other input sequence should produce an output pulse.  **(15)**	**BLT-6**	Create
3.	Design a sequential circuit for a state diagram shown below.	**BLT-6**	Create

	Use state assignment rules for assigning states and compare the required combinational circuit with random state assignment.  **(15)**		
4.	Consider the asynchronous sequential circuit driven by the pulse shown below. Analyse the circuit and draw the timing diagram.  **(15)**	**BLT-6**	Create
5.	Express the importance of simulator for simulating a digital system in HDL models of sequential circuit. **(15)**	**BLT-5**	Evaluate

UNIT IV ANALOG MODULATION			
Amplitude Modulation – AM, DSBSC, SSBSC, VSB – PSD, modulators and demodulators – Angle modulation – PM and FM – PSD, modulators and demodulators – Super heterodyne receivers.			
PART- A			
Q.No.	**Questions**	**BT Level**	**Competence**
1.	Define amplitude and angle modulation.	**BLT-1**	Remember
2.	Illustrate AM and FM signals produced by a single tone signal.	**BLT-3**	Apply
3.	What is the relationship between frequency and phase modulation?	**BLT-2**	Understand
4.	Compare AM with DSB-SC and SSB-SC.	**BLT-4**	Analyze
5.	Draw the spectrum of an AM signal.	**BLT-4**	Analyze
6.	What is the bandwidth of the FM signal if the frequency sensitivity of the modulator is 25 KHz per volt?	**BLT-3**	Apply
7.	What is the need for modulation?	**BLT-2**	Understand
8.	Define angle modulation.	**BLT-1**	Remember
9.	What is modulation index and percent modulation?	**BLT-2**	Understand
10.	Define amplitude modulation.	**BLT-1**	Remember
11.	Differentiate between narrow band and wide band FM.	**BLT-4**	Analyze

12.		Explain demodulation.	**BLT-5**	Evaluate
13.		Illustrate the spectrum of an FM signal.	**BLT-6**	Create
14.		Define PM.	**BLT-1**	Remember
15.		Distinguish between FM and PM.	**BLT-4**	Analyze
16.		Write about modulation and modulation index.	**BLT-3**	Apply
17.		Discuss percent modulation and modulation index in AM.	**BLT-6**	Create
18.		Calculate percentage modulation in AM if carrier amplitude is 20 V and modulating signal is of 15V.	**BLT-5**	Evaluate
19.		State Carson's rule of FM bandwidth.	**BLT-2**	Understand
20.		A 107.6 MHZ carrier is frequency modulated by a 7 kHZ sine wave. The resultant FM signal has a frequency of 50 kHZ. Determine the modulation index of the FM wave.	**BLT-5**	Evaluate
21.		Write the two major limitations of the standard form of amplitude modulation.	**BLT-3**	Apply
22.		Define modulation index for FM.	**BLT-1**	Remember
23.		Define frequency deviation.	**BLT-1**	Remember
24.		State instantaneous phase deviation.	**BLT-2**	Understand
		PART-B		
1.	**(i)**	For an AM DSBFC transmitter with an unmodulated carrier with power Pc = 100W that is modulated simultaneously by three modulating signals with coefficients of modulation m_1= 0.2, m_2= 0.4 and m_3= 0.5, Determine : 1) Total coefficient of modulation 2) Upper and lower sideband power 3) Total transmitted power. **(6)**	**BLT-5**	Evaluate
	(ii)	Draw the block diagram of Armstrong indirect FM transmitter and describe its operation. **(7)**	**BLT-4**	Analyze
2.	**(i)**	Write the advantages and disadvantages of angle modulation. **(6)**	**BLT-3**	Apply
	(ii)	Write about the indirect method of generating wideband FM signal. **(7)**		
3.		Describe frequency discrimination method of generating SSB modulated wave and a method to demodulate it. What are the design issues involved in this method of generation? What is the cause and effect of phase error in demodulated signal? **(13)**	**BLT-1**	Remember
4.		Develop the expression for the instantaneous voltage of SSB wave. **(13)**	**BLT-6**	Create
5.	**(i)**	Develop the expression for instantaneous voltage of AM wave. **(6)**	**BLT-6**	Create
	(ii)	Describe the relationship between the instantaneous carrier frequency and the modulating signal for FM.	**BLT-1**	Remember

		(7)		
6.	With the help of mathematical expressions explain about Amplitude modulation and its generation. **(13)**		**BLT-2**	Understand
7.	**(i)**	Draw the phasor diagram of a wideband FM and explain about the bandwidth of FM signal. **(6)**	**BLT-4**	Analyze
	(ii)	Explain the difference between phase modulation and frequency modulation. **(7)**	**BLT-2**	Understand
8.	**(i)**	In modulation by several sine waves simultaneously, the bandwidth of AM requires twice the highest modulation frequency. Prove this concept using appropriate expressions. **(6)**	**BLT-5**	Evaluate
	(ii)	Determine the percentage power saving when the carrier and one of the sidebands are suppressed in an AM wave modulated to a depth of 100 percent and 50 percent. **(7)**		
9.	**(i)**	Describe frequency modulation and phase modulation and their inter-relationship. **(6)**	**BLT-2**	Understand
	(ii)	Explain the frequency analysis of angle modulated waves. **(7)**		
10.	Write the equations for AM voltage and power distribution. **(13)**		**BLT-3**	Apply
11.	**(i)**	Write a note on frequency deviation of FM wave. (**7**)	**BLT-3**	Apply
	(ii)	What is the need for modulation? **(6)**	**BLT-1**	Remember
12.	**(i)**	Explain with block diagram of a FM transmitter with direct modulation. **(6)**	**BLT-2**	Understand
	(ii)	Describe the generation of FM. **(7)**	**BLT-2**	Understand
13.	**(i)**	Discuss about spectral characteristics of FM signal. **(6)**	**BLT-1**	Remember
	(ii)	Derive for carrier power and transmitter power in AM in terms of modulation index. **(7)**	**BLT-4**	Analyze
14.	**(i)**	Differentiate between AM and FM. **(6)**	**BLT-4**	Analyze
	(ii)	Define FM and PM modulation with their equations. Describe the generation of FM wave using Armstrong method. **(7)**	**BLT-1**	Remember
15.	**(i)**	Explain the principles of amplitude modulation. **(7)**	**BLT-1**	Remember
	(ii)	Explain the bandwidth requirement for FM and define carson's rule. **(6)**		
16.	Describe the relationship between FM and PM along with modulation index, Bandwidth requirement and Average power. **(13)**		**BLT-1**	Remember
17.	Illustrate the Armstrong method of FM generation and compare NBFM and WBFM. **(13)**		**BLT-4**	Analyze

PART-C				
1.	For an envelope with +Vmax=30Vp and +Vmin=+10Vp, determine. 1) Unmodulated carrier amplitude. 2) Modulated carrier amplitude. 3) Peak change in the amplitude of the envelope. 4) Modulation coefficient. 5) Percent modulation. **(15)**		**BLT-5**	Evaluate
2.	An audio frequency signal 10 $\sin(2\pi 500t)$ is used to amplitude modulate a carrier of $50\sin(2\pi 10^5 t)$. Calculate 1) Modulation index 2) Sideband frequencies 3) Amplitude of each sideband frequencies 4) Bandwidth 5) Total power dissipated to load of 600Ω. **(15)**		**BLT-5**	Evaluate
3.	Explain frequency modulation and phase modulation and their inter-relationship. **(15)**		**BLT-5**	Evaluate
4.	**(i)**	Derive the expression for the power calculation in DSB-SC–AM wave. **(8)**	**BLT-6**	Create
	(ii)	A broadcast transmitter radiates 20KW when the modulation percentage is 75%. Calculate carrier power and power of each sidebands. **(7)**	**BLT-5**	Evaluate
5.	Construct frequency discrimination method of generating SSB modulated wave and a method to demodulate it. Discuss the design issues involved in this method of generation. What is the cause and effect of phase error in demodulated signal? **(15)**		**BLT-6**	**Create**

UNIT V DIGITAL MODULATION			
Low pass sampling theorem – Quantization – PAM – Line coding – PCM, DPCM, DM, and ADPCM and ADM, Time Division Multiplexing, Frequency Division Multiplexing. Phase shift keying – BPSK, DPSK, QPSK			
PART- A			
Q.No.	**Questions**	**BT Level**	**Competence**
1.	State Sampling theorem.	**BLT-1**	Remember
2.	What do you understand by the term aliasing.	**BLT-1**	Remember
3.	What is the slope overload error? How it can be minimized?	**BLT-1**	Remember
4.	What are the drawbacks of PAM signal?	**BLT-1**	Remember
5.	Write the Advantages and Disadvantages of Digital Communication.	**BLT-3**	Apply

6.	Define Quantization Error. [Or] Quantization noise.		**BLT-1**	Remember
7.	Why Quantization is required? (Or) Why do we need equalization in base band pulse transmission?		**BLT-2**	Understand
8.	What is the Comparison between natural PAM and Flat top sampling?		**BLT-2**	Understand
9.	Define Nyquist rate.		**BLT-1**	Remember
10.	What is meant by aliasing effect?		**BLT-2**	Understand
11.	How the message can be recovered from PAM?		**BLT-2**	Understand
12.	Write an expression for bandwidth of binary PCM with N messages each with a maximum frequency of *fm* Hz.		**BLT-3**	Apply
13.	Mention the merits of DPCM.		**BLT-3**	Apply
14.	What is the main difference in DPCM and DM?		**BLT-5**	Evaluate
15.	Write the Advantages and Disadvantages of "Delta Modulation"		**BLT-3**	Apply
16.	What are the two limitation of delta modulation?		**BLT-4**	Analyze
17.	List the Applications of PCM.		**BLT-5**	Evaluate
18.	What is meant by adaptive delta modulation?		**BLT-5**	Evaluate
19.	What is meant by DPSK?		**BLT-6**	Create
20.	What is the difference between PSK and FSK?		**BLT-4**	Analyze
21.	Write the advantages of BPSK.		**BLT-6**	Create
22.	Compare bandwidth efficiency of BPSK and QPSK modulated signals.		**BLT-4**	Analyze
23.	What is meant by offset QPSK?		**BLT-2**	Understand
24.	What is the difference between TDM and FDM.		**BLT-4**	Analyze
	PART-B			
1.	Explain DM with transmitter and receiver block diagram. Comment on its advantage and drawbacks. **(13)**		**BLT-3**	Apply
2.	Explain coherent BFSK modulation and demodulation with block diagram and waveforms. **(13)**		**BLT-1**	Remember
3.	With neat sketch, explain the generation of DM signals. State the drawbacks of DM and suggest a method to correct it. **(13)**		**BLT-3**	Apply
4.	Explain the QPSK modulation schemes with its constellation diagram. **(13)**		**BLT-2**	Understand
5.	**(i)**	Explain PCM systems with neat diagram. **(8)**	**BLT-1**	Remember
	(ii)	Explain the process of "Companding" and its Characteristics. **(5)**	**BLT-1**	Remember
6.	**(i)**	With a neat block diagram, describe the PAM modulation and demodulation process and develop an expression for PAM wave. **(8)**	**BLT-1**	Remember
	(ii)	Compare PAM, PWM and PPM. **(5)**	**BLT-1**	Remember

7.	List the advantages of digital carrier system and describe MSK techniques with neat diagram. **(13)**		**BLT-1**	Remember
8.	**(i)**	Explain in detail the applications of digital modulation techniques. **(7)**	**BLT-1**	Remember
	(ii)	Briefly describe the concept of QAM and draw the constellation diagram of 16 QAM. **(6)**	**BLT-3**	Apply
9.	**(i)**	How does ADM differ from DM, Support your answer with block diagram and waveform. **(6)**	**BLT-2**	Understand
	(ii)	Enumerate the generation of PWM wave with neat sketch. **(7)**		
10.	Explain with the block diagram QPSK Transmitter and Receiver. Also analyse about the bandwidth considerations for QPSK. **(13)**		**BLT-2**	Understand
11.	With a neat block diagram, explain BPSK transmitter and receiver. Also analyse the spectrum and bandwidth considerations of BPSK. **(13)**		**BLT-5**	Evaluate
12.	Explain DPCM with required diagram. How does it differ from PCM? **(13)**		**BLT-2**	Understand
13.	**(i)**	Describe in detail Frequency shift keying method with necessary diagrams. **(7)**	**BLT-3**	Apply
	(ii)	Discuss GMSK with advantages and disadvantages. **(6)**	**BLT-4**	Analyze
14.	**(i)**	Discuss about the working principle of ASK modulator and detector with neat diagram. **(6)**	**BLT-4**	Analyze
	(ii)	What is DPSK? Discuss its operation with the required diagrams. **(7)**		
15.	**(i)**	Analyse modulation and demodulation of PPM? **(6)**	**BLT-4**	Analyze
	(ii)	Tell about uniform quantization, noise and SNR in PCM. **(7)**		
16.	State and prove sampling theorem. Obtain the reconstructed signal and explain about aliasing? **(13)**		**BLT-5**	Evaluate
17.	Explain in detail about QPSK modulator and demodulator with neat diagram and also compare with BPSK.		**BLT-6**	Create
	PART – C			
1.	**(i)**	Compare between ASK, BPSK, QPSK and FSK digital modulation techniques. **(7)**	**BLT-6**	Create
	(ii)	Represent QPSK signals in the signal space to find the distance between the signal points. Give the spectrum of QPSK signal. **(8)**		
2.	Draw the transmitter and receiver block diagram of		**BLT-5**	Evaluate

	Binary Phase shift keying scheme and compare its error performance with Binary Frequency Shift keying scheme. **(15)**			
3.	**(i)**	Explain the QPSK modulation schemes with its constellation diagram. **(8)**	**BLT-6**	Create
	(ii)	Briefly describe the concept of QAM and draw the constellation diagram of QAM. **(7)**		
4.	**(i)**	A data bit sequence consists of the following string of bits 10 11 10 10. Evaluate and draw the nature of waveform transmitted by BPSK transmitter. **(8)**	**BTL-5**	Evaluate
	(ii)	For an 8 PSK modulator with an input data rate equal to 10 Mbps & a carrier frequency of 70 MHz, measure minimum double sided Nyquist bw, Baud rate, Sketch the output spectrum. Judge the results with BPSK & QPSK modulators. **(7)**		
5.	How would you compare the various digital communication systems? **(15)**		**BLT-6**	Create