SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF MEDICAL ELECTRONICS

QUESTION BANK

III SEMESTER

1910301 ANALOG ELECTRONICS

Regulation – 2019

Academic Year 2022 – 23(Odd)

Prepared by

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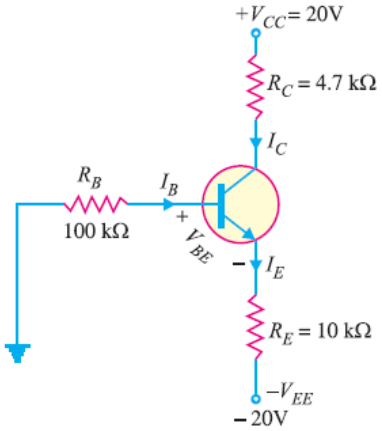
SUBJECT : 1910301 – ANALOG ELECTRONICS

SEM / YEAR: III / II

UNIT I - BJT AC ANALYSIS			
BJT Transistor Modelling, The re transistor model, Common emitter fixed bias, Voltage divider bias, Emitter follower configuration. Darlington connection- DC bias; The Hybrid equivalent model, Approximate Hybrid Equivalent Circuit- Fixed bias, Voltage divider, Emitter follower configuration; Complete Hybrid equivalent model, Hybrid π Model.			
PART – A			
Q.No	**Questions**	**BT Level**	**Domain**
1.	Define biasing and its need.	**BTL 1**	Remembering
2.	Name the commonly used model in the small – signal ac analysis of transistor networks.	**BTL 1**	Remembering
3.	Outline the methods used for transistor biasing. Which one is popular?	**BTL 2**	Understanding
4.	Express the importance of Darlington circuit.	**BTL 2**	Understanding
5.	Examine the hybrid model of BJT in CE configuration.	**BTL 1**	Remembering
6.	Mention the requirements for biasing circuits.	**BTL 3**	Applying
7.	Give the limitations of h-parameters.	**BTL 2**	Understanding
8.	Draw the fixed bias single stage transistor circuit.	**BTL 3**	Applying
9.	Differentiate small signal equivalent & hybrid π equivalent circuit.	**BTL 4**	Analyzing
10.	Distinguish between dc and ac load line with suitable diagram.	**BTL 2**	Understanding
11.	Summarize the amplifiers classification according to the input.	**BTL 2**	Understanding
12.	Name the elements in the hybrid π model.	**BTL 1**	Remembering
13.	Write the techniques used to improve input impedance.	**BTL 3**	Applying
14.	Mention the need for bootstrapped Darlington circuit.	**BTL 4**	Analyzing
15.	Draw the hybrid π equivalent model of the BJT.	**BTL 3**	Applying
16.	Write the current amplification factors of the three transistor amplifier configurations.	**BTL 2**	Understanding
17.	List out the advantages of h parameter.	**BTL 1**	Remembering
18.	Short circuit CE current gain of transistor is 25 at a frequency of 2 MHz if f_β = 200 kHz Examine i) h_{fe} ii) find $\|A_i\|$ at frequency of 10 MHz and 100 MHz.	**BTL 4**	Analyzing
19.	Quote the requirements for biasing circuits.	**BTL 1**	Remembering

20.	Calculate the stability factor S for a fixed bias circuit.		**BTL 3**	Applying
21.	How can a DC equivalent circuit of an amplifier be obtained?		**BTL 4**	Analyzing
22.	What does bootstrapping mean? Why bootstrapping is done in a buffer amplifier?		**BTL 4**	Analyzing
23.	Determine the elements in hybrid-π model of BJT.		**BTL 3**	Applying
24.	Which amplifier is called as voltage follower? Why?		**BTL 4**	Analyzing
	PART – B			
1.	Illustrate the working of a voltage divider biasing circuit and calculate the stability factor for BJT.	**(13)**	**BTL 3**	Applying
2.	Examine the Common Emitter r_e model of npn transistor.	**(13)**	**BTL 3**	Applying
3.	(i) Distinguish between CE,CB and CC amplifiers. (ii) Explain the concept of bootstrapping.	**(6)** **(7)**	**BTL 2**	Understanding
4.	Find the equation for the CE short circuit current gain Ai as a function of frequency using hybrid - π model.	**(13)**	**BTL 1**	Remembering
5.	Draw the h-parameter equivalent circuit for a typical common emitter amplifier and derive expression for A_i, A_v, R_i and R_o.	**(13)**	**BTL 3**	Applying
6.	With suitable diagram, explain about fixed bias Common-Emitter Configuration with un bypassed R_E .	**(13)**	**BTL 4**	Analyzing
7.	(i) Summarize the characteristics and features of emitter follower circuit. (ii) Illustrate the working of darlington amplifier with neat sketch.	**(6)** **(7)**	**BTL 2**	Understanding
8.	For a BJT with a voltage divider bias circuit, find the change in Q-point with the variation in β when the circuit contains an emitter resistor. Let the biasing resistors be R_{B1} = 56kΩ, R_{B2}=12.2 kΩ, R_C = 2kΩ, R_E = 0.4kΩ, V_{CC} = 10V, $V_{BE(ON)}$ = 0.7V and β =100.	**(13)**	**BTL 1**	Remembering
9.	Examine the operation of a Voltage Divider biasing in Common-Emitter Configuration.	**(13)**	**BTL 4**	Analyzing
10.	Explain bootstrapped Darlington emitter follower with necessary equations.	**(13)**	**BTL 4**	Analyzing
11.	With neat diagram, explain hybrid π Model of Common Emitter configuration.	**(13)**	**BTL 2**	Understanding
12.	Explain voltage divider bias method for BJT and derive an expression for stability factor.	**(13)**	**BTL 1**	Remembering
13.	(i) Analyze the transconductance, gm for hybrid π Model of Common Emitter configuration. (ii) Outline the biasing methods for BJT.	**(8)** **(5)**	**BTL 4**	Analyzing
14.	Briefly write the concept of the Common Emitter amplifier using approximate h-model.	**(13)**	**BTL 1**	Remembering
15.	(i)Summarize the merits and limitations of common base amplifier. (ii)Discuss the characteristics and uses of Common Emitter amplifier.	**(6)** **(7)**	**BTL 2**	Understanding
16.	Explain how will you determine the h-parameters of a transistor experimentally?	**(13)**	**BTL 3**	Applying
17.	Derive the expression for input impedence ,output impedence and voltage gain of a common emitter amplifier.	**(13)**	**BTL 1**	Remembering
	PART-C			

1.	The hybrid parameters for a CE amplifier are h_{ie} =1000 ohms, h_{oe} = 25 x 10^{-6} ohms, h_{fe}=150 *and* h_{re}=1.2 x 10^{-4}. The transistor has a load resistance of 10 kΩ in collector and supplied from signal source of resistance 5 kΩ.Analyze the values of input impedance, output impedance, current gain and voltage gain.	**(15)**	**BTL 4**	Analyzing
2.	Determine A_i, A_v, Ri, R_o, A_{is}, A_{vs} of a single stage Common Emitter amplifier with R_s = 500 Ω, R_L = 2000Ω, hfe = 50, hie =1kΩ, hoe = 25μ A/V and hre = $2x10^{-4.}$	**(15)**	**BTL 3**	Applying
3.	A given transistor with I_c =10mA (Collector current), V_{CE} =10 V (Collector-Emitter voltage) and at room temperature has the following set of low frequency parameters: hie=500Ω, hoe=$10^{-5}A/V$, hfe=100 *and* hre=10^{-4}. Examine the values of all hybrid -π parameters of a low frequency model and draw the equivalent low frequency hybrid -π model.	**(15)**	**BTL 1**	Remembering
4.	Design a voltage divider bias circuit for bipolar junction transistor to establish the quiescent point at V_{CE} =12V,I_C =1.5mA,Stability factor S≤ 3,β =50,V_{BE}=0.7V,V_{CC} = 22.5V and R_C=5.6 kΩ.	**(15)**	**BTL 2**	Understanding
5.	For the emitter bias circuit shown in Figure, find I_E, I_C, V_C and V_C and V_{CE} for β= 85 and V_{BE} = 0.7V. 	**(15)**	**BTL 1**	Remembering

UNIT II - FIELD EFFECT TRANSISTORS

Construction and Characteristics of JFETs, Transfer Characteristics, Depletion type MOSFET, Enhancement type MOSFET. FET Amplifiers: JFET small signal model, Fixed bias configuration, Self bias configuration, Voltage divider configuration, Common Gate configuration. Source- Follower Configuration, Cascade configuration.

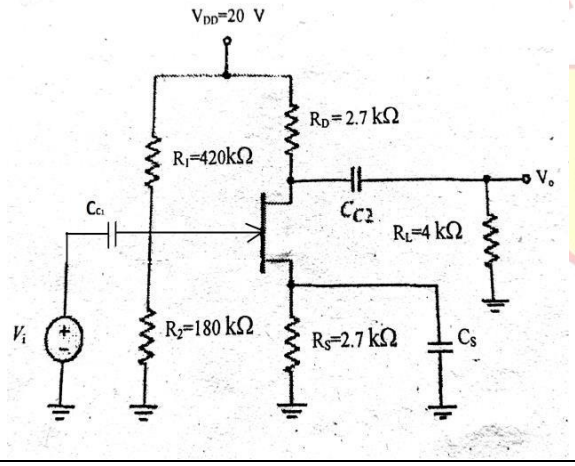
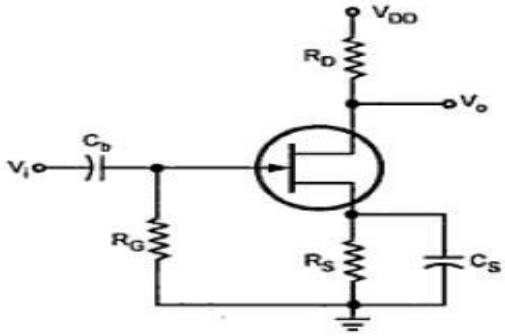
PART – A

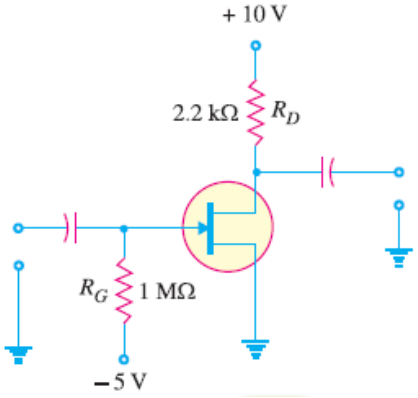
Q.No	Questions	BT Level	Domain
1.	List the advantages of common drain amplifier.	**BTL 1**	Remembering
2.	Analyze the output impedance for the MOSFET amplifier given: K_n = 1mA/V, V_{TN} = 1.2V, A_V = 0.855 ,λ = 0.01V^{-1}, and I_{DQ} = 1mA.	**BTL 4**	Analyzing
3.	How a MOSFET can be used to amplify a time varying voltage?	**BTL 1**	Remembering
4.	Differentiate the three FET configurations (CS, CD and CG).	**BTL 4**	Analyzing
5.	Comparison between JFET and MOSFET.	**BTL 1**	Remembering
6.	The parameters for the transistor below are K_n = 0.5 mA/V^2, V_{TN} = 1.2V, and λ = 0. Simplify V_{DS} and V_{GS} for IQ=50 μA.	**BTL 4**	Analyzing

7.	Express the value of ideal voltage gain for a certain JFET which has a g_m of 4 mS. with an external drain resistance of 1.5kΩ.	**BTL 2**	Understanding
8.	Predict the value of Transconductance,when V_{GS} of a FET changes from -3.1V to -3V, the drain current changes from 1 mA	**BTL 2**	Understanding
9.	Identify the impact of including a source resistor in the FET amplifier.	**BTL 1**	Remembering
10.	Analyze the hybrid small signal model of Common Gate configuration.	**BTL 4**	Analyzing
11.	If the midband gain of an amplifier is 100 and half power frequencies are f_L =40Hz and f_H=16kHz. Calculate the amplifier gain at 20Hz and 20kHz frequency.	**BTL 3**	Applying
12.	Construct a basic circuit for an operation of enhancement type MOSFET.	**BTL 4**	Analyzing
13.	Mention the methods used for biasing circuits in FET.	**BTL 2**	Understanding
14.	List the characteristics of JFET.	**BTL 2**	Understanding
15.	Express the drain current equation of JFET.	**BTL 2**	Understanding
16.	Draw the block diagram of two stage cascaded amplifier.	**BTL 3**	Applying
17.	Construct a small signal model of JFET.	**BTL 3**	Applying
18.	Cite three basic configuration of FET.	**BTL 1**	Remembering
19.	Why transformer coupling is not used in the initial stages of a multistage amplifier?	**BTL 1**	Remembering
20.	Two amplifiers having gain of 20 dB and 40 dB are cascaded. Infer the overall gain in dB.	**BTL 2**	Understanding
21.	What do you understand by pinch off voltage and out of voltage?	**BTL 4**	Analyzing
22.	Draw the transfer characteristic for n-channel depletion type MOSFET?	**BTL 3**	Applying
23.	Mention the three regions that are present in the drain source characteristics of JFET?	**BTL 3**	Applying
24.	Write the relative disadvantages of an FET over that of a BJT?	**BTL 3**	Applying

PART – B

1.	Illustrate the construction and operation of MOSFET with neat diagram.	**(13)**	**BTL 3**	Applying
2.	Describe the construction and working of (i) n-channel JFET. (ii) p-channel JFET.	 **(7)** **(6)**	**BTL 2**	Understanding
3.	(i) How to compute the small signal parameters for a MOSFET. (ii) Analyze and configure a common-source amplifier with source resistor.	**(7)** **(6)**	**BTL 4**	Analyzing
4.	Describe the biasing methods of MOSFET.	**(13)**	**BTL 2**	Understanding
5.	Examine Z_i, A_v, A_i and Z_o for FET amplifier with voltage divider bias using hybrid model.	**(13)**	**BTL 3**	Applying
6.	With neat sketch explain two stage cascaded amplifier and analyze its overall A_v, A_t, R_t and R_o.	**(13)**	**BTL 4**	Analyzing
7.	(i) Interpret how JFET can be used as an amplifier (ii) Examine the drain and transfer characteristics of JFET.	**(6)** **(7)**	**BTL 3**	Applying
8.	Outline the need for cascading and explain the block diagram of two stage cascaded amplifier.	**(13)**	**BTL 1**	Remembering
9.	Sketch the diagram of a Common drain amplifier and derive the expression for the voltage gain.	**(13)**	**BTL 1**	Remembering

10.	(i) List the biasing methods of MOSFET and derive an expression for stability factor. (ii) Explain the expression for common gate circuit of JFET.	**(6)** **(7)**	**BTL 1**	Remembering
11.	Describe a small signal low frequency model for JFET and derive an expression for Z_i, A_V, A_i and Z_O.	**(13)**	**BTL 2**	Understanding
12.	Analyze a simple JFET source-follower amplifier circuit and discuss the general AC circuit characteristics.	**(13)**	**BTL 4**	Analyzing
13.	Draw the small-signal high-frequency circuit of a common source amplifier and derive the expression for voltage gain.	**(13)**	**BTL 1**	Remembering
14.	With the help of a neat diagram explain the operation of an n-channel enhancement type MOSFET.	**(13)**	**BTL 2**	Understanding
15.	Draw the circuit diagram of a common gate amplifier.Derive the expression for its voltage gain and input resistance.	**(13)**	**BTL 3**	Applying
16.	How a small signal high frequency model is different from low frequency model. Explain briefly.	**(13)**	**BTL 4**	Analyzing
17.	What are the biasing methods available to achieve the required bias in a junction field effect transistor. Explain any one biasing	**(13)**	**BTL 3**	Applying
	PART – C			
1.	Design the circuit shown below with transistor parameters I_{DSS} = 12mA, V_p = -4V and λ = 0.008V^{-1}. Determine the small signal voltage gain $A_v=V_o/V_i$. 	**(15)**	**BTL 2**	Understanding
2.	The amplifier shown in Fig. an n-channel FET for which, I_D=0.8mA, V_P = -2V, V_{dd} = 24V and I_{DSS}=1.6mA. Assume that rd>Rd. Examine the parameters V_{GS}, g_m, Rs. 	**(15)**	**BTL 1**	Remembering
3.	With a neat diagram, explain the source and drain resistance biasing of MOSFET.	**(15)**	**BTL 3**	Applying
4.	Formulate the stability factors for any two biasing methods in detail.	**(15)**	**BTL 1**	Remembering

5.	A JFET in Fig. 4 has values of VGS (off) = – 8V and I_{DSS} = 16 mA. Determine the values of VGS, ID and VDS for the circuit. 	**(15)**	**BTL 4**	Analyzing

UNIT III - BJT AND JFET FREQUENCY RESPONSE

Logarithms, Decibels, Low frequency response – BJT Amplifier with RL, Low frequency response-FET Amplifier, Miller effect capacitance, High frequency response – BJT Amplifier, High frequency response-FET Amplifier, Multistage Frequency Effects.

PART – A

Q.No	Questions	BT Level	Domain
1.	What is the effect of miller's capacitance on the frequency response of an amplifier?	**BTL 1**	Remembering
2.	Define rise time. Give the relationship between bandwidth and rise time.	**BTL 1**	Remembering
3.	For an amplifier, midband gain = 100 and lower cutoff frequency is 1 kHz. Find the gain of an amplifier at frequency 20 Hz.	**BTL 3**	Applying
4.	Estimate transistor switching times.	**BTL 2**	Understanding
5.	Draw the high frequency equivalent model for MOSFET.	**BTL 3**	Applying
6.	Quote the reason for reduction in gain for lower and higher frequencies in case of amplifiers.	**BTL 1**	Remembering
7.	If the rise time of a BJT is 35 nano seconds. Identify the bandwidth that can be obtained using this BJT.	**BTL 1**	Remembering
8.	Analyze the expressions for gain bandwidth product for voltage and current.	**BTL 4**	Analyzing
9.	Draw the general frequency response curve of an amplifier.	**BTL 3**	Applying
10.	Determine the effect of coupling capacitors on the bandwidth of the amplifier.	**BTL 3**	Applying
11.	Infer the effects of emitter bypass capacitor on high frequency response.	**BTL 4**	Analyzing
12.	Summarize the need of cascading multistage amplifiers.	**BTL 1**	Remembering
13.	Differentiate small signal equivalent & hybrid π equivalent circuit.	**BTL 2**	Understanding
14.	Express the equation of overall lower and upper cutoff frequency of multistage amplifier.	**BTL 2**	Understanding
15.	Express the amplification factor μ of Field Effect Transistor, if r_d = 4 kΩ and g_m = 4 mA/V.	**BTL 2**	Understanding
16.	Compare BJT and MOSFET Amplifiers.	**BTL 4**	Analyzing
17.	List out the advantages of h parameter.	**BTL 1**	Remembering
18.	Identify and mention the limitations of multistage amplifiers.	**BTL 2**	Understanding
19.	Design the high frequency model of FET.	**BTL 3**	Applying
20.	Give the main reason for the drop in gain at the low frequency region & high frequency region.	**BTL 2**	Understanding

21.	Why an NPN transistor has a better high frequency response than the PNP transistor?	**BTL 4**		Analyzing
22.	Write the equation for the output voltage and voltage gain for CS amplifier.	**BTL 3**		Applying
23.	Analyze the importance of emitter bypass capacitor.	**BTL 4**		Analyzing
24.	What are the advantages of representation of gain in decibels? Why thermal runaway is not there in MOSFETs?	**BTL 4**		Analyzing
	PART - B			
1.	(i) Tabulate the effect of capacitors on frequency response. (ii) Describe with neat diagram and derive the expression for cut off frequency of a BJT.	**(6)** **(7)**	**BTL 1**	Remembering
2.	(i) With neat diagram, explain the frequency response of BJT amplifier. (ii) What are the significance of cut off frequencies and Bandwidth of the amplifier.	**(6)** **(7)**	**BTL 4**	Analyzing
3.	How would you describe the relation between rise time, upper cut off frequency and bandwidth.	**(13)**	**BTL 1**	Remembering
4.	Determine the high frequency equivalent circuit of a MOSFET from its geometry and derive the expression for short circuit current gain in the common source configuration.	**(13)**	**BTL 3**	Applying
5.	(i) Draw the Hybrid π equivalent circuit of a BJT. (ii)Using hybrid model, draw the high frequency equivalent circuit of CE amplifier and derive for higher cut-off frequencies.	**(3)** **(10)**	**BTL 3**	Applying
6.	Elaborate the effect of coupling and bypass capacitors.in the low frequency response of BJT amplifier.	**(13)**	**BTL 2**	Understanding
7.	Explain the upper and lower cut off frequencies of multistage amplifier with expressions.	**(13)**	**BTL 1**	Remembering
8.	Summarize the operation of high frequency common source FET amplifier with neat diagram. Derive the expression for (i) voltage gain (ii) input admittance (iii) input capacitance (iv) output admittance.	**(13)**	**BTL 2**	Understanding
9.	(i)Derive the expression for frequency response of multistage amplifier. (ii) List the significance of cut off frequencies and Gain bandwidth product of amplifier.	**(8)** **(5)**	**BTL 1**	Remembering
10.	Describe the high frequency equivalent circuit of FET and hence derive gain bandwidth product for any one configuration.	**(13)**	**BTL 2**	Understanding
11.	Outline the low frequency analysis of amplifier to obtain lower cut-off frequency.	**(13)**	**BTL 4**	Analyzing
12.	Explain the function of transistor and derive the expression for input conductance (g_{be}) and output resistance (g_{ce}) for hybrid – π common emitter transistor model.	**(13)**	**BTL 4**	Analyzing
13.	Summarize the expressions for the short circuit current gain of common emitter amplifier at a high frequency. Define alpha cut-off frequency, beta cut-off frequency and transition frequency and derive their values in terms of the circuit parameters.	**(13)**	**BTL 2**	Understanding
14.	Illustrate the Common Drain Amplifier Circuit and determine the Small signal equivalent circuit at high frequencies.	**(13)**	**BTL 3**	Applying

15.	Derive an expression for lower cut –off frequency of a BJT amplifier.	**(13)**	**BTL 1**	Remembering
16.	Determine the frequency response of multistage amplifier.	**(13)**	**BTL 3**	Applying
17.	Analyze the factors that affect the low frequency response of BJT and JFET.	**(13)**	**BTL 4**	Analyzing
	PART – C			
1.	(i)Design the high frequency analysis of JFET with necessary circuit diagram& gain bandwidth product. (ii)Explain the frequency response of MOSFET CS amplifier.	**(8)** **(7)**	**BTL 2**	Understanding
2.	Obtain the low frequency response and high frequency response of an amplifier, derive its cutoff frequency & discuss the terms rise time and sag.	**(15)**	**BTL 1**	Remembering
3.	Determine the midband gain A_m and upper 3dB frequency f_H of a CS amplifier fed with a signal source having an internal resistance R_{sig}=100kΩ.The amplifier has R_G=4.7MΩ, R_D=R_L=15kΩ, g_m=1mA/V, r_o=150kΩ, c_{gs}=1pF and c_{gd} = 0.4pF.	**(15)**	**BTL 3**	Applying
4.	Label a high frequency equivalent circuit of a FET amplifier and derive the expression for output admittance for common drain configuration.	**(15)**	**BTL 1**	Remembering
5.	Design the BJT amplifier circuit and obtain its high frequency response.	**(15)**	**BTL 4**	Analyzing

UNIT IV- FEEDBACK AND OSCILLATOR CIRCUITS

Feedback concepts, Feedback connection types, Practical feedback circuits, Oscillator operation, FET Phase shift oscillator, Wien bridge oscillator, Tuned Oscillator circuit, Crystal oscillator, UJT construction, UJT Oscillator.

PART - A

Q.No	Questions	BT Level	Domain
1.	The overall gain of a multistage amplifier is 140.When negative voltage feedback is applied the gain is reduced to 17.5.Find the fraction of the output that is feedback to the input.	**BTL 1**	Remembering
2.	Assess the two Barkhausen conditions required for sinusoidal oscillation to be sustained.	**BTL 2**	Understanding
3.	Define intrinsic stand-off ratio in UJT?	**BTL 1**	Remembering
4.	List the disadvantages of negative feedback in amplifiers and how it can be overcome?	**BTL 1**	Remembering
5.	Show the expression for the frequency of oscillations of a in phase shift oscillator.	**BTL 3**	Applying
6.	An amplifier has a current gain of 240 and input impedence of 15kΩ without feedback. If negative current feedback (current attenuation = 0.015) is applied, What will be the input impedence of the amplifier?	**BTL 4**	Analyzing
7.	What is the advantage of a Colpitts oscillator compared to a phase shift oscillator?	**BTL 4**	Analyzing
8.	Which is the most commonly used feedback arrangement in cascaded amplifier and why?	**BTL 1**	Remembering
9.	Name the type of feedback circuit that increases gain of an amplifier.	**BTL 1**	Remembering

10.	Outline the advantages of crystal oscillator.	**BTL 2**	Understanding
11.	Discuss about Nyquist's stability criteria for feedback amplifiers.	**BTL 2**	Understanding
12.	Draw the oscillator model which uses both positive and negative feedback.	**BTL 3**	Applying
13.	Determine the operating frequency of transistor Hartley oscillator if L_1 = 50μH, L_2 = 1mH, and mutual inductance between the coils M = 10 μH and C = 10pF.	**BTL 3**	Applying
14.	Categorize the characteristics of an amplifier which are modified by negative feedback.	**BTL 4**	Analyzing
15.	List out the advantages of phase shift oscillator.	**BTL 1**	Remembering
16.	Analyzing the effects on bandwidth and output impedance due to feedback.	**BTL 4**	Analyzing
17.	Illustrate the expression for frequency of oscillation of a Wein-bridge oscillator.	**BTL 3**	Applying
18.	Distinguish between negative and positive feedback.	**BTL 2**	Understanding
19.	Give the limitations of LC and RC oscillators.	**BTL 2**	Understanding
20.	A wein bridge oscillator has an operating frequency at f_0 =10 kHz. If the value of R is 100Ω, obtain the value of the capacitor in the feedback network.	**BTL 3**	Applying
21.	What will happen to the oscillation if the magnitude of the loop gain is greater than unity?	**BTL 4**	Analyzing
22.	A weinbridge oscillator is used for operations at 9KHz. If the value of resistance R is 100KΩ, determine the value of C required?	**BTL 3**	Applying
23.	Differentiate oscillator from amplifier.	**BTL 4**	Analyzing
24.	Draw the electrical equivalent circuit of crystal. and mention its series and parallel resonance frequency	**BTL 3**	Applying

PART - B

1.	With neat block diagram, explain the operation of following feedback amplifiers. (i) Voltage series feedback amplifier. (ii) Current shunt feedback amplifier.	**(7)** **(6)**	**BTL 4**	Analyzing
2.	(i) Explain with neat circuit diagram, the working of Hartley oscillator using transistor. (ii)Derive an expression for frequency of oscillation.	**(6)** **(7)**	**BTL 1**	Remembering
3.	(i) Describe the operation of Wien – Bridge oscillator with suitable diagram. (ii)Derive an expression for frequency of oscillation.	**(6)** **(7)**	**BTL 1**	Remembering
4.	Explain the basic construction and equivalent circuit of a UJT and briefly explain the device operation.	**(13)**	**BTL 3**	Applying
5.	Illustrate the operation of UJT as a relaxation oscillator and express its frequency of oscillation.	**(13)**	**BTL 3**	Applying
6.	(i) With neat circuit diagram, discuss the operation of Colpitts Oscillator with neat circuit diagram. (ii) Derive the expressions for the frequency of oscillation and the condition for maintenance of oscillation.	**(6)** **(7)**	**BTL 2**	Understanding
7.	Describe the construction and working of crystal oscillator with neat diagram.	**(13)**	**BTL 2**	Understanding

8.	Analyze the working principle of Hartley oscillator with neat diagram.	**(13)**	**BTL 4**	Analyzing
9.	An amplifier has a gain of 1000 without feedback and cut-off frequencies are f1 = 1.5 kHz and f2 = 501.5 kHz. If 1% of output voltage of the amplifier is applied as negative feedback, express the new cut-off frequencies ?	**(13)**	**BTL 2**	Understanding
10.	Sketch a circuit diagram of a two stage capacitor coupled BJT amplifier that uses series voltage negative feedback. Explain how the feedback operates.	**(13)**	**BTL 4**	Analyzing
11.	Examine the working of a phase shift oscillator. Discuss its advantages and disadvantages.	**(13)**	**BTL 1**	Remembering
12.	Analyze the operation of current series feedback amplifier and derive its expression for (i)Input resistance. (ii)Output resistance. (iii)Voltage gain. (iv)Feedback ratio.	**(4)** **(4)** **(3)** **(2)**	**BTL 4**	Analyzing
13.	(i) Enumerate the basic concept of feedback. (ii) List the different types of feedback. Explain about the positive feedback.	**(6)** **(7)**	**BTL 1**	Remembering
14.	(i) Mention the condition for oscillation of an oscillator. (ii) Summarize the advantages of negative current feedback on the performance of amplifiers.	**(5)** **(8)**	**BTL 2**	Understanding
15.	With neat circuit diagram, explain the operation of RC Phase shift oscillator using FET.	**(13)**	**BTL 3**	Applying
16.	An amplifier with an open-circuit voltage gain of 1000 has an output resistance of 100 Ω and feeds a resistive load of 900 Ω. Negative voltage feedback is provided by connecting a resistive voltage divider across the output and one-fiftieth of the output voltage is fedback in series with the input signal. Determine the voltage gain with negative feedback.	**(13)**	**BTL 3**	Applying
17.	When negative voltage feedback is applied to an amplifier of gain 100, the overall gain falls to 50. Calculate the fraction of the output voltage feedback, and if this fraction is maintained, calculate the value of the amplifier gain required if the overall stage gain is to be 75.	**(13)**	**BTL 4**	Analyzing
	PART – C			
1.	Determine the frequency of oscillations hen a RC phase shift oscillator has R=12 $k\Omega$,C=0.01 μF and R_C=3.3 $k\Omega$.Also find the minimum current gain needed for this purpose.	**(15)**	**BTL 3**	Applying
2.	(i)When negative voltage feedback is applied to an amplifier of gain 100,the overall gain falls to 50.Find the fraction of the output voltage feedback. If this fraction is maintained , Infer the values of the amplifier gain required if the overall stage gain is to be 75**.** (ii)Calculate the amplifier gain, f_{1f}, f_{2f} and D_f when negative feedback ratio is 0.01. An amplifier has voltage gain of 400, f_1 =50Hz, f_2 = 200kHz and distortion of 10% without feedback.	**(5)** **(10)**	**BTL 4**	Analyzing

3.	(i)In a Colpitts oscillator,C_1=C_2=C and L=100 x 10^{-6}H. The frequency of oscillation is 500 KHz. Determine the value of the capacitance C. (ii)In Colpitts oscillator, the desired frequency is 500 kHz. Find the value of L. Assume C=1000 pF.	**(8)** **(7)**	**BTL 4**	Analyzing
4.	An amplifier has a mid frequency gain of 100 and a bandwidth of 200 kHz. (i)Compute the new bandwidth and gain if 5% negative feedback is introduced. (ii)Evaluate the amount of feedback, if the bandwidth is restricted to 1 MHz.	**(8)** **(7)**	**BTL 1**	Remembering
5.	Design a Colpitts oscillator with capacitance C_1 = 100 pF and C_2 = 7500 pF.The inductance is variable. Determine the range of inductance values, if the frequency of oscillation is to vary between 950 kHz and 2050 kHz.	**(15)**	**BTL 2**	Understanding

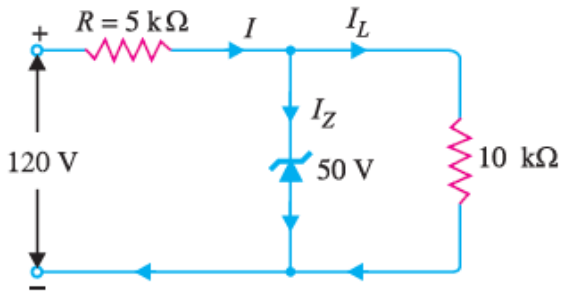
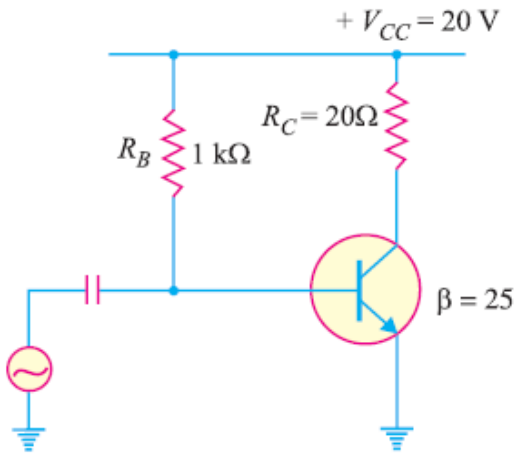
UNIT V - POWER AMPLIFIERS

Definition and amplifier types, Series fed class A amplifier, Transformer coupled class A amplifier, Class B amplifier operation and circuits, Amplifier distortion, Class C and Class D amplifiers. Voltage Regulators: Discrete transistor voltage regulation - Series and Shunt Voltage regulators.

PART –A

Q.No	Questions	BT Level	Domain
1.	Define conversion efficiency of a power amplifier.	**BTL 1**	Remembering
2.	Summarize the temperature effects in power amplifier.	**BTL 2**	Understanding
3.	A transformer-coupled class A power amplifier supplies power to an 80Ωload connected across the secondary of a step-down transformer having a turn ratio 5:1. Calculate the maximum power output for a zero signal collector of 120mA.	**BTL 3**	Applying
4.	What is meant by second order harmonic distortion?	**BTL 1**	Remembering
5.	Mention two conditions to be satisfied by a complementary symmetry power stage.	**BTL 3**	Applying
6.	List out the classifications of Power amplifiers.	**BTL 1**	Remembering
7.	Express the power relations of Class B amplifier.	**BTL 2**	Understanding
8.	Name the types of voltage regulators.	**BTL 1**	Remembering
9.	Identify the typical characteristics for the transformer-coupled circuit.	**BTL 1**	Remembering
10.	Why class A amplifier must not be operated under no signal conditions?	**BTL 4**	Analyzing
11.	Construct the circuit diagram of a Push Pull amplifier.	**BTL 4**	Analyzing
12.	Outline the advantages of the transformer coupled class A power amplifier?	**BTL 2**	Understanding
13.	Differentiate between Voltage and Power amplifier.	**BTL 4**	Analyzing
14.	Interpret the efficiency of Class C amplifier.	**BTL 2**	Understanding
15.	Intrepret the configuration used in complementary symmetry power amplifier. How does it help?	**BTL 2**	Understanding
16.	Draw the output characteristics of class A amplifier.	**BTL 3**	Applying
17.	State the advantages of transformer-coupled class A amplifier over the RC-coupled circuit.	**BTL 1**	Remembering

18.	Compare the efficiencies of all the power amplifiers.	**BTL 4**		Analyzing
19.	Summarize the characteristics of Class B amplifier.	**BTL 2**		Understanding
20.	Mention the applications of Class C amplifier.	**BTL 3**		Applying
21.	Write the derating factor expression of a power transistor?	**BTL 3**		Applying
22.	Where S amplifiers are used?	**BTL 4**		Analyzing
23.	Which amplifier gives minimum distortion?	**BTL 3**		Applying
24.	How do you bias the class A operation?	**BTL 4**		Analyzing
	PART –B			
1.	(i) Explain the working of Transformer coupled Class-A power amplifier with the help of a neat circuit diagram. (ii)Give the expression for dc power input, ac power output and efficiency?	**(8)** **(5)**	**BTL 1**	Remembering
2.	Write about the Class B transformer coupled power amplifier with necessary derivations.	**(13)**	**BTL 1**	Remembering
3.	Examine the circuit operation and output resistance of Class AB power amplifiers.	**(13)**	**BTL 1**	Remembering
4.	Summarize the transfer characteristic, signal waveforms, power dissipation, and power conversion efficiency of Class A amplifier.	**(13)**	**BTL 2**	Understanding
5.	(i) Explain in detail about the Class C power amplifier. (ii) Distinguish between series and shunt voltage regulators.	**(6)** **(7)**	**BTL 2**	Understanding
6.	(i)Illustrate the operation of class-AB power amplifier with a neat sketch. (ii)Describe Class AB power amplifier using MOSFETs.	**(6)** **(7)**	**BTL 2**	Understanding
7.	Enumerate the working of Series fed, directly coupled Class-A power amplifier with the help of a neat circuit diagram. Give the expression for dc power input, ac power output and efficiency?	**(13)**	**BTL 1**	Remembering
8.	Analyze the circuit diagram of class B push pull amplifier and explain its operation. Also prove that its conversion efficiency is 78.5%.	**(13)**	**BTL 4**	Analyzing
9.	(i)Sketch the transformer coupled class A amplifier and compute its maximum efficiency is 50%. (ii)Compare the push-pull class B and complementary symmetry class B amplifier.	**(10)** **(3)**	**BTL 3**	Applying
10.	(i) Construct the circuit diagram of push-pull amplifier and explain why even harmonics are not present in a push- pull amplifier. (ii)Mention two additional advantages of this circuit over that of a single transistor amplifier.	**(10)** **(3)**	**BTL 3**	Applying
11.	Outline the power amplifier classes with respect to its operating cycle, position of Q-point and efficiency.	**(13)**	**BTL 4**	Analyzing
12.	(i) Differentiate power MOSFET with BJTs. (ii) Evaluate the temperature effects of Power MOSFET.	**(6)** **(7)**	**BTL 4**	Analyzing
13.	(i)Explain the class AB power amplifier using MOSFET. (ii)Analyze the structure of Power MOSFETs and explain its characteristics.	**(6)** **(7)**	**BTL 4**	Analyzing
14.	Illustrate the working of Class-B power amplifier with the help of a neat circuit diagram.	**(13)**	**BTL 3**	Applying
15.	How do you classify power amplifiers? With the help of suitable sketches compare Class –A,Class –B and Class –C amplifiers.	**(13)**	**BTL 3**	Applying

16.	With neat diagram, explain the operation of Single ended Class –A power amplifier.		**BTL 2**	Understanding
17.	Why a power amplifier is called as Large Signal Amplifier? Explain briefly.		**BTL 3**	Applying
	PART –C			
1.	A class B push pull amplifier supplies power to a resistive load of 12 Ohms. The output transformer has a turn of 3:1 and efficiency of 78.5%. (i) Maximum power output. (ii) Maximum power dissipation in each transistor. (iii) Maximum base and collector current for each transistor Assume hfe=25 and Vcc=20V.	**(5)** **(5)** **(5)**	**BTL 4**	Analyzing
2.	For the Class-B complementary A.F power amplifier, estimate maximum AC power which can be developed, collector dissipation while developing maximum AC power, efficiency, maximum power dissipation per transistor, efficiency under maximum power dissipation condition.	**(15)**	**BTL 2**	Understanding
3.	For the circuit shown ,determine (i) the output voltage (ii) the voltage drop across series resistance (iii) the current through zener diode. 	**(5)** **(5)** **(5)**	**BTL 3**	Applying
4.	Design the circuit diagram of a linear voltage regulator and explain about its types.	**(15)**	**BTL 2**	Understanding
5.	Examine the (i) output power (ii) input power and (iii) collector efficiency of the amplifier circuit shown in Figure. It is given that input voltage results in a base current of 10 mA peak. 	**(15)**	**BTL 1**	Remembering