SRM VALLIAMMAI ENGINEERINGCOLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur–603203

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VI SEMESTER

1906008 - EMBEDDED AND REAL TIME SYSTEMS

Regulation–2019

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(Even Semester)

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SUBJECT : 1906008–EMBEDDEDAND REAL TIME SYSTEMS

SEM / YEAR : VI / III-Year B.E.

UNIT I - INTRODUCTION TO EMBEDDED SYSTEM DESIGN

Complex systems and microprocessors– Embedded system design process –Design example: Model train controller- Design methodologies- Design flows - Requirement Analysis – Specifications-System analysis and architecture design – Quality Assurance techniques - Designing with computing platforms – consumer electronics architecture – platform-level performance analysis.

PART -A

Q. No	Questions	BT level	Domain
1.	Define Embedded system.	BTL 1	Remembering
2.	What are the applications of an embedded system?	BTL 1	Remembering
3.	What are the typical characteristics of an embedded system?	BTL 1	Remembering
4.	List the important considerations when selecting a processor.	BTL 2	Understanding
5.	Classify the processors in embedded system	BTL 4	Analyzing
6.	List the steps in embedded system design process.	BTL 2	Understanding
7.	Mention the challenges in the design of embedded computing system.	BTL 3	Applying
8.	List the non-functional requirements of an Embedded Architecture.	BTL 1	Remembering
9.	Give the major levels of abstraction in the Embedded system design.	BTL 3	Applying
10.	What are the services to be provided by consumer electronics?	BTL 1	Remembering
11.	What you mean by real time computing?	BTL 2	Understanding
12.	Identify the various issues in real time computing.	BTL 2	Understanding
13.	Mention the observations of quality management of ISO 9000.	BTL 2	Understanding
14.	Draw the functional architecture diagram of multimedia player.	BTL 3	Applying
15.	Interpret the importance of DCC in train controller.	BTL 3	Applying
16.	Illustrate the need of flash file systems in consumer electronics.	BTL 3	Applying
17.	Assess the characteristics of embedded computing.	BTL 4	Analyzing
18.	Categorize the steps involved in system analysis using CRC card.	BTL 4	Analyzing

19.	Write the requirements chart for GPS moving map system.		BTL 1	Remembering
20.	Justify the need of UML language for Embedded system design.		BTL 4	Analyzing
21.	Depict the UML notation for display class.		BTL 4	Analyzing
22.	Summarize the five levels of maturity in CMM model.		BTL 2	Understanding
23.	Sketch the block diagram of moving map GPS system		BTL 2	Understanding
24.	What software factors might be considered when choosing a computing platform?		BTL 4	Analyzing
	PART-B			
1.	Discuss in detail about the characteristics features of Embedded computing applications	(13)	BTL 2	Understanding
2.	Write in detail about the challenges in embedded computing system design.	(13)	BTL 4	Analyzing
3.	Briefly Illustrate the performance of embedded computing systems.	(13)	BTL 2	Understanding
4.	Explain in detail about various levels of abstraction in the embedded system design process with necessary diagrams	(13)	BTL 3	Applying
5.	Analyze the requirements and write the requirement chart needed for designing a GPS moving map in embedded system design process.	(13)	BTL 4	Analyzing
6.	Write down the major operations and data flows of a GPS moving map and draw its hardware and software architecture diagrams.	(13)	BTL 3	Applying
7.	(i). Explain a Model Train Controller with suitable diagrams. (ii). Outline the design steps of Model Train Controller in detail.	(5) (8)	BTL 2	Understanding
8.	Describe the goal of design methodology in detail.	(13)	BTL 1	Remembering
9.	Illustrate with diagrams the system design methods using waterfall, spiral and successive refinement model.	(13)	BTL 2	Understanding
10.	Explain briefly about hardware/software design system, hierarchical design flows and concurrent engineering models with necessary diagrams.	(13)	BTL 4	Analyzing
11.	Describe in detail about Control-Oriented Specification Languages used in design of embedded system with necessary diagrams.	(13)	BTL 3	Applying
12.	What is CRC and explain the system analysis and architecture design using CRC card Layout.	(13)	BTL 1	Remembering
13.	What is Quality assurance? and explain briefly about the quality assurance techniques	(13)	BTL 1	Remembering
14.	Write short note on the following in terms of consumer electronics system architecture. i. Use cases and requirements. ii. Platforms and Operating Systems.	(6) (7)	BTL 1	Remembering

15.	Examine in detail the about the main components of designing with computing platforms.	(13)	BTL 4	Analyzing
16.	With necessary diagram explain the need of platform level performance analysis.	(13)	BTL 3	Applying
17.	**(i).** What are the factors to be considered while designing an Embedded System Process? **(ii).** State the importance of Structural and Behavioral description in detail.	(6) (7)	BTL 4	Analyzing
	PART -C			
1.	Summarize the different factors involved in embedded system design process of GPS moving map with necessary illustrations.	(15)	BTL 1	Remembering
2.	Justify the need of Quality Assurance techniques in Embedded design and explain.	(15)	BTL 2	Understanding
3.	Develop the requirement, specification, and state diagram of a model train controller with necessary illustrations.	(15)	BTL 3	Applying
4.	Analyze the steps involved in complex embedded system design with an example of consumer electronics architecture in detail.	(15)	BTL 4	Analyzing
5.	Design an Alarm clock and explain the various steps involved in the design of computing system.	(15)	BTL 4	Analyzing

UNIT II - ARM PROCESSOR AND PERIPHERALS

ARM Architecture Versions – ARM Architecture – Instruction Set – Stacks and Subroutines – Features of the LPC 214X Family – Peripherals – The Timer Unit – Pulse Width Modulation Unit – UART – Block Diagram of ARM9 and ARM Cortex M3 MCUhavard.

PART A

Q. No	Questions	BT Level	Competence
1.	List the functions of ARM processor in Supervisory mode.	BTL 1	Remembering
2.	Write down the main differences between Von Neumann and Harvard architecture.	BTL 3	Applying
3.	Differentiate CISC and RISC architectures.	BTL 3	Applying
4.	What is "Thumb" in ARM processor?	BTL 1	Remembering
5.	List the three different profiles of ARM cortex Processor.	BTL 1	Remembering
6.	Differentiate between assembler and compiler.	BTL 3	Applying
7.	Name the registers set of ARM processor.	BTL 1	Remembering
8.	What is the use of CPSR Register?	BTL 4	Analyzing
9.	What is instruction pupelining?	BTL 1	Remembering
10.	Write down the significance of TST instruction.	BTL 2	Understanding
11.	State the usage of EQU directive in programming.	BTL 2	Understanding
12.	Draw the sequence of actions needed for a nested procedure.	BTL 4	Analyzing
13.	What is meant by idle mode in processors?	BTL 3	Applying

14.	Outline the significance of SWI instruction.		BTL 2	Understanding
15.	Compare the differences between MULS and MULSEQ.		BTL 3	Applying
16.	Find the methods to terminate the power down mode.		BTL 3	Applying
17.	Give the maximum size of the constant that can be used in the immediate mode?		BTL 3	Applying
18.	Distinguish between PCLK and CCLK.		BTL 4	Analyzing
19.	For a GPIO pin to be made to act as an ON/OFF switch, what are the registers to be used?		BTL 4	Analyzing
20.	Write the difference between single and double edged PWM.		BTL 4	Analyzing
21.	Mention the important features that make ARM ideal for embedded applications.		BTL 2	Understanding
22.	What will be the output of the instruction MOV R11, R2?		BTL 4	Analyzing
23.	How does the prescalar in a timer unit function?		BTL 2	Understanding
24.	What is interrupt Latency?		BTL 1	Remembering
PART – B				
1.	With necessary diagrams briefly explain about the register set of ARM processor.	(13)	BTL 1	Remembering
2.	Describe briefly about the operating modes of ARM and also explain about mode switching.	(13)	BTL 2	Understanding
3.	Illustrate in detail about the interrupt vector table by providing the vector address of each interrupt supported by ARM.	(13)	BTL 4	Analyzing
4.	(i) Classify the ARM instruction set. (ii) Explain any one type of instruction set with example.	(3) (10)	BTL 4	Analyzing
5.	Write the general structure of an Assembly language line and explain briefly about directives used in ARM with examples for each directive.	(13)	BTL 1	Remembering
6.	What are the types of stacks and subroutines supported by ARM processor? Explain with the instruction sets.	(13)	BTL 2	Understanding
7.	Explain the following indexed addressing mode with a sample instruction. i) Pre indexed Addressing mode. ii) Post indexed Addressing mode.	(7) (6)	BTL 4	Analyzing
8.	Discuss in detail about Arithmetic and logical instructions of ARM with examples for each.	(13)	BTL 4	Analyzing
9.	Explain in detail about Compare and branch instructions of ARM with examples for each.	(13)	BTL 3	Applying
10.	With neat block diagram explain the architecture of LPC2148 ARM7 MCU and its features.	(13)	BTL 3	Applying
11.	Illustrate briefly about Rotate and Shift instructions of ARM with examples for each.	(13)	BTL 3	Applying
12.	Explain in detail about the working of timer unit of LPC2148 with its associated registers.	(13)	BTL 4	Analyzing
13.	With neat block diagram illustrate the working of a UART in LPC214x ARM.	(13)	BTL 3	Applying

14.	Draw the architecture of ARM Cortex M3 MCU processor and describe its functional units.	(13)	BTL 6	Creating
15.	Describe briefly about the concepts behind single edge controlled PWM.	(13)	BTL 2	Understanding
16.	(i) Calculate the value of the clock to be given in PWMMR0 andPWMMR3 to get a pulse train of period 5 ms and duty cycle of 25%. (ii) List the features of LPC 214x processor.	(7) (6)	BTL 5	Evaluating
17.	With necessary illustrations explain the features of the ARM 9 processor Core.	(13)	BTL 1	Remembering
	PART – C			
1	Write a program to find the sum of 3X + 4Y + 9Z, where X = 2, Y = 3 and Z = 4 using ARM Processor instruction set.	(15)	BTL 3	Applying
2	Find the output of the program using ARM instructions for $3X^2 + 5Y^2$, where X = 8 and Y = 5.	(15)	BTL 4	Analyzing
3	Summarize the procedure to generate the square wave from Timer unit in LPC214x chip with an example code.	(15)	BTL 2	Understanding
4	(i). With necessary illustrations, explain the control registers of PWM unit. (ii) Determine the values to be entered in the PWMPCR register for the following situations? i) Single edge control for PWM3. ii) Double edge control for PWM3. iii) Single edge control for PWM1, 2 and 3.	(6) (9)	BTL 1	Remembering
5.	The content of registers is given as below R1 = 0xEF00DE12, R2 = 0x0456123F, R5 = 4, R6 = 28. What is the output result in the destination register when the following instructions are executed? i) LSL R1, #8 ii) ASR R1,R5 iii) ROR R2,R6 iv) LSR R2,#5	(4) (4) (4) (3)	BTL 4	Analyzing

UNIT III <u>EMBEDDED PROGRAMMING</u>
Components for embedded programs- Models of programs- Assembly, linking and loading – compilation techniques- Program level performance analysis – Software performance optimization – Program level energy and power analysis and optimization – Analysis and optimization of program size- Program validation and testing.
PART A

Q. No	Questions	BT Level	Competence
1	Mention the different components for embedded programs.	BTL 1	Remembering
2	State the basic principle of compilation technique.	BTL 1	Remembering
3	Name any two techniques used to optimize execution time of program.	BTL 1	Remembering
4	Mention the various compilation techniques.	BTL 1	Remembering
5	What does a linker do?	BTL 1	Remembering
6	State the difference between program location counter and program counter.	BTL 1	Remembering
7	Illustrate the need of symbol table in Assemblers.	BTL 2	Understanding
8	Outline the significance of CDFG.	BTL 2	Understanding
9	Summarize the two ways used for performing input and output operations	BTL 2	Understanding
10	Describe about the elements of program performance.	BTL 2	Understanding
11	Draw a Data Flow Graph and Control/ Data Flow Graph (CDFG) with an example.	BTL 3	Applying
12	Interpret the differences between loop fusion and loop tiling	BTL 3	Applying
13	Find the limitation of polling techniques.	BTL 3	Applying
14	Compare enqueueing and dequeueing	BTL 4	Analyzing
15	State the importance of Boot-block flash.	BTL 4	Analyzing
16	Differentiate compiler and cross compiler.	BTL 4	Analyzing
17	Write the importance of circular buffer.	BTL 1	Remembering
18	Draw the diagram of software state machine.	BTL 4	Analyzing
19	Draw a Data Flow Graph for the block shown below: r = a+b-c; s = a*r ; t = b-d; r = d+e;	BTL 4	Analyzing
20	How power can be optimized at the program level?	BTL 3	Applying
21	What is program optimization in embedded system?	BTL 1	Remembering
22	How power can be optimized at the program level in embedded system?	BTL 3	Applying
23	What are the basic compilation techniques in embedded systems?	BTL 1	Remembering
24	List out the challenges facing in embedded software testing.	BTL 1	Remembering

PART – B

1	Summarize the components of embedded program and discuss in detail about each component.	(13)	BTL 2	Understanding
2	Describe about stream-oriented programming and circular buffer with example.	(13)	BTL4	Analyzing
3	(i) List the different models of Program. (ii) Briefly explain with neat diagrams on various models of program.	(3) (10)	BTL 1	Remembering
4	Examine the Data flow graph with the help of an example.	(13)	BTL 2	Understanding
5	Illustrate the Control /Data flow graph for a While loop with necessary diagrams and explain.	(13)	BTL 1	Remembering
6	In compilation process, explain the role of i) Assemblers ii) Linkers	(7) (6)	BTL 2	Understanding
7	With the help of a flow chart describe the basic compilation process and explain.	(13)	BTL 3	Applying

8	Determine the code generated for the given conditional code snippet, explain with necessary CDFG.
	if (a + b > 0)
	x = 5;
	else
	x = 7;
		(13)	BTL 4	Analyzing

9	Outline about the Procedure and Data structure with respect to compilers.	(13)	BTL 1	Remembering
10	Interpret the need of dead code elimination to optimize the program with a code snippet.	(13)	BTL 3	Applying
11	Write about the Loop transformation techniques for optimization of code.	(13)	BTL 1	Remembering
12	Outline the Program level energy and power analysis and optimization.	(13)	BTL 4	Analyzing
13	Write about i) Black box Testing ii) White box Testing	 (7) (6)	BTL 1	Remembering
14	(i) With necessary diagrams about the program level performance analysis. (ii) Mention the key features of cache optimizations.	(7) (6)	BTL 3	Applying
15	Outline the verification techniques involves in Embedded Systems	(13)	BTL 4	Analyzing
16	Describe in detail about the assembly linking and loading in Embedded system programming?	(13)	BTL 2	Understanding
17	Interpret the Program level performance analysis in embedded system.	(15)	BTL 3	Applying
	PART C			

1	Write a symbol table for the following code snippet and explain in detail.
	ORG 100
	label1 ADR r4,c
	LDR r0,[r4]
	label2 ADR r4,d
	LDR r1,[r4]
	label3 SUB r0,r0,r1
		(15)	BTL 1	Remembering

2	Describe he statement translation into ARM instruction for the expression a*b + 5*(c-d) with necessary illustrations.	(15)	BTL 2	Understanding
3	Interpret the various methods for Program optimization with necessary examples.	(15)	BTL 3	Applying
4	Outline the different techniques used in software performance optimization.	(15)	BTL 4	Analyzing
5	Why the person generating clear-box program tests should not be the person who wrote the code being tested.	(15)	BTL 4	Analyzing

UNIT IV REAL TIME SYSTEMS

Structure of a Real Time System — Estimating program run times – Task Assignment and Scheduling – Fault Tolerance Techniques – Reliability, Evaluation – Clock Synchronization.

PART A

Q.No.	Questions	BT Level	Competence
1	List out the two Rate Monotonic scheduling conditions.	BTL 1	Remembering
2	Outline the uniprocessor scheduling algorithms.	BTL 1	Remembering
3	Define Performance measures for real time systems.	BTL 1	Remembering
4	What is mean by hardware and software fault?	BTL 1	Remembering
5	State the limitation of Rate Monotonic algorithm.	BTL 1	Remembering
6	Define hardware redundancy.	BTL 1	Remembering
7	Summarize the two steps of tasks for developing a multiprocessor schedule.	BTL 2	Understanding
8	Draw the performance degradation graph of a fault tolerant system	BTL 2	Understanding
9	Explain the forward and backward error recovery.	BTL 2	Understanding
10	Classify the partitioning of the inter-vote interval.	BTL 2	Understanding
11	Illustrate the role of static priority algorithm.	BTL 3	Applying
12	Sketch the frequency response of an ideal VCO.	BTL 3	Applying
13	How will you distinguish static priority algorithm & dynamic priority algorithm?	BTL 3	Applying
14	Outline the features of preemptive and non-preemptive schedule.	BTL 4	Analyzing
15	Compare the difference between release time and deadline.	BTL 4	Analyzing
16	Identify the fault types based on temporal behavior classification.	BTL 4	Analyzing
17	Write the ways of assigning priorities in scheduling.	BTL 2	Understanding
18	What are the features of offline and online scheduling?	BTL 1	Remembering
19	Write about malicious or byzantine failures.	BTL 2	Understanding
20	Compare the difference between periodic, sporadic and aperiodic tasks.	BTL 4	Analyzing
21	Compare between the Rate-Monotonic and Deadline-Monotonic Algorithms.	BTL 4	Analyzing
22	What are the various scheduling criteria for CPU scheduling?	BTL 1	Remembering
23	Draw the state diagram of task?	BTL 2	Understanding
24	Mention some task scheduling algorithms.	BTL 1	Remembering

PART B			
1	Write a short notes on transient faults and the use of state aggregation (13)	BTL 2	Understanding
2	i) List out the sequence of events resulting in triad failure. (6) ii)Explain the methodology to choose the best distribution for obtaining parameter values in model. (7)	BTL 1	Remembering
3	Describe the typical designs for voter reliability with the example of Poisson failures. (13)	BTL 1	Remembering

4	Mention the classification of faults according to their temporal behavior and output behavior and explain. (13)	BTL 1	Remembering
5	Write a detailed note on mathematical understanding of the priority ceiling algorithm using a series of results. (13)	BTL 2	Understanding
6	Summarize the important features on : a) Software Redundancy in Fault tolerance techniques. (6) b) Measuring error propagation times in Fault tolerance synchronization. (7)	BTL 2	Understanding
7	Describe about Rate Monotonic Scheduling Algorithm with examples. (13)	BTL 2	Understanding
8	(i) Explain the permanent faults in series parallel system. (7) (ii) Summarize the performance measures for real time systems? (6)	BTL 3	Applying
9	Outline the features of information redundancy and its principle to obtain a code that will correct multiple bit errors. (13)	BTL 3	Applying
10	(i). Write about the limited usefulness of software error models? (5) (ii). Explain how the clocks are synchronized if the times are close to each other. (8)	BTL 4	Analyzing
11	(i) Compare independent failure and correlated failure. (3) (ii) Examine the process of completely connected zero propagation system. (10)	BTL 4	Analyzing
12	Summarize the concepts of impact of faults and Loss of synchrony in fault tolerant systems. (13)	BTL 4	Analyzing
13	Write about reliability models for hardware redundancy. (13)	BTL 4	Analyzing
14	Outline the More general model assuming that the failure process and fault latency are exponential and Poisson distributed. (13)	BTL 3	Applying
15	Describe the real time system and discuss the structure of real time systems. (13)	BTL 2	Understanding
16	Write in detail about System reliability and Mean Time To Failure(MTTF) (13)	BTL 4	Analyzing
17	List the characteristics of task assignment /scheduling and Multiprocessor schedule. (13)	BTL1	Remembering
PART – C			
1	Explain the mathematical concepts of Identical Linear Reward functions in Uniprocessor scheduling. (15)	BTL 4	Analyzing
2	Describe the completely connected zero propagation time system in hardware fault tolerant synchronization. (15)	BTL 2	Understanding
3	Outline the utilization bound for the RM algorithm and explain in detail. (15)	BTL 3	Applying
4	Summarize with necessary illustrations explain the following redundancy in fault tolerant systems. (i) Hardware Redundancy (5) (ii) Software Redundancy (5) (iii) Information Redundancy (5)	BTL 2	Understanding
5	Write about system reliability preliminaries in detail. (15)	BTL1	Remembering

UNIT V PROCESSES AND OPERATING SYSTEMS

Introduction – Multiple tasks and multiple processes – Multirate systems- Preemptive real-time operating systems- Priority based scheduling- Interprocess communication mechanisms – Evaluating operating system performance- power optimization strategies for processes – Example Real time operating systems-POSIX-Windows CE. - Distributed embedded systems – MPSoCs and shared memory multiprocessors. – Design Example - Audio player, Engine control unit – Video accelerator.

PART – A

Q.No	Questions	BT Level	Competence
1.	Mention the networks for distributed embedded systems.	BTL1	Remembering
2.	Define the term time quantum.	BTL1	Remembering
3.	List the major function of POSIX RTOS.	BTL1	Remembering
4.	What is Semaphore?	BTL1	Remembering
5.	State the needs of CPU accelerator in embedded systems.	BTL1	Remembering
6.	Outline the advantages and limitations of Priority based process scheduling.	BTL1	Remembering
7.	Summarize the essential criteria's of rate monolithic scheduling.	BTL2	Understanding
8.	Explain priority inversion briefly.	BTL2	Understanding
9.	Enumerate the various scheduling states of a process.	BTL2	Understanding
10.	Write examples of blocking and Non-blocking inter process Communication	BTL2	Understanding
11.	Draw the block diagram of Distributed embedded systems	BTL3	Applying
12.	Identify the principle of multi rate embedded system by quoting three Examples	BTL3	Applying
13.	Mention the two different styles used for inter process communication.	BTL3	Applying
14.	Compare between a process and thread.	BTL4	Analyzing
15.	Differentiate between initiation time and completion time	BTL4	Analyzing
16.	Explain the multi-processing systems.	BTL4	Analyzing
17.	Determine the communication among processes which runs at different rates.	BTL3	Applying
18.	Summarize the important characteristics of Multitasking.	BTL2	Understanding
19.	Write about hard-real-time operating system with an example.	BTL1	Remembering
20.	Compile the organization of scheduling policy.	BTL3	Applying
21.	Write short notes on Distributed embedded systems.	BTL1	Remembering
22.	What are the advantages of Shared memory multiprocessors?	BTL3	Applying
23.	Why Power optimization strategies are required?	BTL4	Analyzing
24.	What is MPSoC in embedded system?	BTL2	Understanding
PART – B			
1.	Enumerate the context switch mechanism for moving the CPU from one executing process to another. (13)	BTL1	Remembering

2.	State how the Kernel determines the order of the processes which has to be executed. (13)	BTL2	Understanding
3.	(i). Enumerate why an automobile engine requires multi rate control.(4) (ii) Describe the performance of the Earliest – Deadline – First scheduling with suitable example. (9)	BTL1	Remembering
4.	Describe the real time operating system called POSIX in detail. (13)	BTL1	Remembering
5.	Explain about Power optimization strategies in embedded system. (13)	BTL2	Understanding
6.	(i) Mention in detail about Shared Resources. (7) (ii) Explain about Windows CE with a neat diagram. (6)	BTL1	Remembering
7.	(i) Write in detail about multitasking and multiprocessing. (4) (ii) Illustrate process state and scheduling. (9)	BTL2	Understanding
8.	Infer in detail about the Characteristics of distributed embedded System. (13)	BTL2	Understanding
9.	Explain the architecture of Distributed Embedded System with neat sketch. (13)	BTL3	Applying
10.	(i) Outline the services of operating system in handling multiple tasks and multiple processes. (7) (ii) Identify the features of preemptive execution with the help of a Sequence diagram. (6)	BTL2	Understanding
11.	(i) Explain in detail about power optimization strategies for CPU operation. (7) (ii) Identify how the Predictive shut down technique proved itself as more sophisticated. (6)	BTL3	Applying
12.	With necessary diagrams explain about Audio Player design. (13)	BTL3	Applying
13.	(i) Outline about priority-based scheduling in detail. (7) (ii) With the help of an example, explain how the knowledge of data dependencies can help to use the CPU more efficiently. (6)	BTL4	Analyzing
14.	(i) Summarize the preemptive real time operating systems in detail. (7) (ii) Analyze the special characteristics of Processes and Internet with the help of a suitable diagram. (6)	BTL4	Analyzing
15.	Explain the concepts of Multiprocessor System-On-Chip (MPSoC) and Shared memory multiprocessor are used in embedded applications. (13)	BTL4	Analyzing
16.	Explain the principle, merits and its limitations of inter-process communication mechanisms. (13)		
17.	(i) Justify this statement with the help of an example. 'The timing requirements on a set of process can strongly influence the type of appropriate scheduling'. (7) (ii) Write about a critical section using semaphores in operating system. (6)		
PART C			
1	Explain about Multiple tasks and multiple processes with suitable examples. (15)	BTL3	Applying

2	Explain the working of Engine control unit in detail. i). Theory of operations and requirements (4) ii). Specification (4) iii). System Architecture (3) iv). Component designing and testing (2) v). System integration and testing. (2)	BTL2	Understanding
3	Outline in detail how shared memory and message passing mechanisms are used for interprocess communication. (15)	BTL1	Remembering
4	With necessary illustrations explain about EDF algorithm for scheduling three process with hyper period 60. (15)	BTL4	Analyzing
5	What is the purpose of Priority based scheduling. Discuss in detail with appropriate diagrams.	BTL2	Understanding