SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF

ELECTRONICS AND INSTRUMENTATION ENGINEERING

QUESTION BANK

IV SEMESTER

1907402– DIGITAL LOGIC CIRCUITS

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UNIT I - NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES			
Review of number systems, binary codes, error detection and correction codes (Parity and Hamming code)- Digital Logic Families, comparison of RTL, DTL, TTL, ECL and MOS families -operation, characteristics of digital logic family.			
PART – A			
S. No	**Questions**	**BT Level**	**Competence**
1.	Solve A (A+B).	**BTL 3**	**Apply**
2.	Point out the gray code for the binary $(10101101)_2$ and $(1010111000)_2$.	**BTL 4**	**Analyze**
3.	Analyze the octal equivalent of $(377)_{10}$.	**BTL 4**	**Analyze**
4.	If $(123)_5 = (A3)_7$, then what is the value of A?	**BTL 6**	**Create**
5.	Write down the truth table of XOR gate.	**BTL 5**	**Evaluate**
6.	Convert $(115)_{10}$ to hexadecimal numbers.	**BTL 2**	**Understand**
7.	State the associative property of Boolean algebra.	**BTL 1**	**Remember**
8.	Express the value of b if $\sqrt{41}_b=5$.	**BTL 2**	**Understand**
9.	Apply DE Morgan's theorem and simplify the Boolean expression ((A'B)' +(AB'))'	**BTL 3**	**Apply**
10.	Explain briefly about parity codes. Mention 2 examples.	**BTL 4**	**Analyze**
11.	Using DE Morgan's theorem, find (a) $\overline{A+B+C}$ (b) $\overline{A(B+C)}$	**BTL 5**	**Evaluate**
12.	Convert 143_{10} into its binary equivalent.	**BTL 3**	**Apply**
13.	Interpret OR gate and AND gate using NAND gates.	**BTL 2**	**Understand**
14.	Convert $(627)_8$ to binary.	**BTL 2**	**Understand**
15.	Simplify (x+y)(x+y') to a minimum number of literals.	**BTL 3**	**Apply**
16.	Classify the different types of number system.	**BTL 4**	**Analyze**
17.	Transform the given binary number to hexadecimal $(111.110110)_2$.	**BTL 5**	**Evaluate**
18.	Tabulate the propagation delay and power dissipation characteristics of ECL and CMOS.	**BTL 1**	**Remember**
19.	Discuss briefly about unit distance code. Give an example.	**BTL 2**	**Understand**
20.	Define fan-in and fan-out.	**BTL 1**	**Remember**
21.	What is a grey code and mention its advantages?	**BTL 1**	**Remember**
22.	List the important CMOS characteristics.	**BTL 1**	**Remember**
23.	Draw the CMOS logic circuit for Inverter and NAND gate.	**BTL 6**	**Create**
24.	Draw the DTL based NAND gate.	**BTL 1**	**Remember**
PART B			
1	Explain in detail about error detecting and error correcting code. **(13)**	**BTL 2**	**Understand**
2.	**(i)** Rewrite the expression A+BC in standard product of sum form. **(7)**	**BTL 6**	**Create**
	(ii) Modify $(11001011.01101)_2$ into its equivalent octal and		

		hexadecimal code. **(6)**		
3.	Describe with an aid of circuit diagram the operation of 2 input RTL NAND gate and list out its advantages. **(13)**		**BTL 2**	**Understand**
4.	Evaluate: $(ABCD.1234)_{16}$ = $(?)_{10}$ **(7)** = $(?)_2$ **(6)**		**BTL 5**	**Evaluate**
5.	**(i)**	Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Examine the method of detecting the error using any one error detecting code. **(7)**	**BLT 3**	**Apply**
	(ii)	Explain in detail the generation of hamming code for 4-bit data. **(6)**		
6.	Encode the binary word 1001101 into even parity Hamming code. **(13)**		**BTL 3**	**Apply**
7.	Write short notes on the following: **(i)** RTL **(7)** **(ii)** DTL **(6)**		**BTL 3**	**Apply**
8.	Describe the procedure to get the Hamming code for any binary word with an example. **(13)**		**BTL 1**	**Remember**
9.	**(i)**	A 12 bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. Identify the original 8 bit data word that was written into memory if the 12 bit word read out is as **(8)** (a) 101110010100 (b) 111111110100	**BTL 1**	**Remember**
	(ii)	Describe in detail about weighted and non-weighted binary codes with examples. **(5)**		
10.	Give the CMOS logic circuit for Universal gate and explain its operation. **(13)**		**BTL 2**	**Understand**
11.	Explain NOR and OR gate construction using ECL. Also point out the characteristics of ECL family. **(13)**		**BTL 1**	**Remember**
12.	**(i)**	Examine about the formation of inverter using CMOS and its operation. **(6)**	**BTL 1**	**Remember**
	(ii)	Explain the structure and working principle of TTL based Totem-pole output configuration. **(7)**		
13.	Draw the MOS logic circuit for NOT gate and explain its operation. **(13)**		**BTL 4**	**Analyze**
14.	Assume a 3-input AND gate with output F and a 3-input OR gate with G output. Show the signals of the outputs F and G as functions of the three inputs ABC. Use all 8 possible combinations of inputs ABC. **(13)**		**BTL 4**	**Analyze**
15.	Draw the circuit diagram of TTL NAND gate and explain its working with the help of a truth table. **(13)**		**BLT 3**	**Apply**

16.	Draw the logic circuit of 2 input DTL NAND gate .Explain its operation with the help of equivalent circuit diagram. **(13)**		**BTL 2**	**Understand**
17.	Convert the following decimal numbers to binary, octal and hexadecimal. **(i)** $(455)_{10}$ **(6)** **(ii)** $(256.22)_{10}$ **(7)**		**BTL 4**	**Analyze**
	PART C			
1.	**(i)**	Deduce $FACE_{16}$ in its binary, octal and decimal equivalent. **(6)**	**BTL 5**	**Evaluate**
	(ii)	Assess the data bits 1101 in a 7-bit even parity Hamming code. **(9)**		
2.	Modify 1010111011101100_2 into its octal, decimal and hexadecimal equivalent. **(15)**		**BTL 5**	**Evaluate**
3.	Design a CMOS inverter and explain its operation. Comment on its characteristics such as Fan-in, Fan-out, Power dissipation, Propagation delay and Noise margin. Compare its advantages over other logic families. **(15)**		**BTL 6**	**Create**
4.	A digital system has 3 bits A, B and C as input. The output Y is 1 when two adjacent bits or 3 equal to 1. **(i)** Develop the k-map for Y and minimize. **(8)** **(ii)** Design the reduced function using NAND gates. **(7)**		**BTL 6**	**Create**
5.	Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any error detecting code. **(15)**		**BTL 6**	**Create**

UNIT II – COMBINATIONAL CIRCUITS			
Combinational logic – representation of logic functions-SOP and POS forms, K-map representations-minimization using K maps – simplification and implementation of combinational logic – multiplexers and demultiplexers – code converters, adders, subtractors, Encoders and Decoders.			
PART – A			
S.No	**Questions**	**BT Level**	**Competence**
1.	What is a K-map?	**BTL 2**	**Understand**
2.	Convert the given expression in canonical SOP form $Y = AC + AB + BC$	**BTL 3**	**Apply**
3.	List out some of the combinational circuits.	**BTL 4**	**Analyze**
4.	Write the POS representation of the following SOP function: $f(x,y,z) = \sum m(0,1,3,5,7)$	**BTL 5**	**Evaluate**
5.	If $A \oplus B = C$, then formulate $A \oplus B \oplus C = 0$.	**BTL 6**	**Create**
6.	Evaluate the function $F(x, y, z) = \sum m(0, 3, 4, 6, 7)$.	**BTL 5**	**Evaluate**

7.	Predict the simplest form of the expression: *Z=AB+AB'. (A'C')'*	**BTL 2**	**Understand**
8.	Point out the design procedure for combinational circuits.	**BTL 4**	**Analyze**
9.	Given *F=B'+A'B+A'C'*. Identify the redundant term using K-Map.	**BTL 2**	**Understand**
10.	Name the gates that are called universal gates. Give the reason.	**BTL 1**	**Remember**
11.	Design a Half Subtractor.	**BTL 6**	**Create**
12.	Show the truth table of 2:1 MUX.	**BTL 3**	**Apply**
13.	Compare decoder and demultiplexer.	**BTL 1**	**Remember**
14.	Draw a logic diagram of a 4 line to 1 line multiplexer.	**BTL 2**	**Understand**
15.	Write the POS form of the SOP expression. *f (x,y,z) = x'yz + xyz' + xy'z*	**BTL 4**	**Analyze**
16.	Define the function of select inputs in MUX.	**BTL 1**	**Remember**
17.	Implement the following function using suitable multiplexer. F(x, y, z)=∑m(0, 2, 5, 7)	**BTL 5**	**Evaluate**
18.	Define half adder and full adder.	**BTL 1**	**Remember**
19.	Differentiate between MUX and DE-MUX.	**BTL 4**	**Analyze**
20.	Determine the exact number of half adders and full adders required for performing the addition of two binary numbers of 5 bits length each.	**BTL 3**	**Apply**
21.	Give one application each for Multiplexer and Decoder.	**BTL 1**	**Remember**
22.	Design a half adder using basic gate.	**BTL 3**	**Apply**
23.	Give the logical expression for sum output and carry output of a full adder.	**BTL 2**	**Understand**
24.	Label the code used for error detection. Name two applications of code convertors.	**BTL 1**	**Remember**

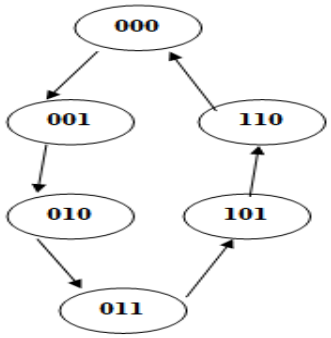
PART B

1.	Examine how to minimize the function: F(A, B, C, D)=∑m(0,4,6,8,9,10,12) +∑d(2,13) and implement it using only NOR gates. **(13)**		**BTL 1**	**Remember**
2.	**(i)**	Interpret the logical expression using K-map in SOP and POS form : F (A, B, C, D) =∑m (0, 2, 3, 6, 7) + d (8, 10, 11, 15). **(8)**	**BTL 2**	**Understand**
	(ii)	Simplify the function F=xy+x'y'z'+x'yz'. **(5)**		
3.	**(i)**	Identify the minimal SOP form for the following function. F(A,B,C,D)=∑m(0,1,3,5,6,8,9,14,26,28,31) +∑d(4,13). **(8)**	**BTL 1**	**Remember**
	(ii)	List the advantages and disadvantages of minimization of Boolean Function using K-Map. **(5)**		
4.	Given the following expression: F= A'C+A'B+AB'C+BC **(i)** Express it in n sum of minterms**.** **(6)**		**BTL 5**	**Evaluate**

	(ii) Find the minimal sum of products expression. **(7)**			
5.	Interpret a full adder circuit using logic gates. **(13)**		**BTL 1**	**Remember**
6.	Express the Boolean function using K-map and implement it using only NAND gates. F (A, B, C, D) =∑m (0, 8, 11, 12, 15) +∑d (1, 2, 4, 7, 10, 14). Give the essential and non-essential prime implicants. **(13)**		**BTL 2**	**Understand**
7.	**(i)**	Plot the logical expression : ABCD + AB'C'D' + AB'C + AB on a 4 variable K-map; obtain the simplified expression from the map. **(7)**	**BTL 3**	**Apply**
	(ii)	Express the function Y = A + B'C in canonical SOP and canonical POS form. **(6)**		
8.	Realize the following Boolean expression using a suitable multiplexer F (A,B,C,D) = ∑(0, 1, 3, 5, 7, 9, 11, 14, 15) **(13)**		**BTL 2**	**Understand**
9.	Describe a 4-bit Binary to gray code converter and implement it using logic gates. **(13)**		**BTL 1**	**Remember**
10.	Draw the logic diagram of a 2-to-4 decoder using NOR gates only. Include an enable input. **(13)**		**BTL 4**	**Analyze**
11.	Analyze a code converter for Gray to Binary code conversion. **(13)**		**BTL 4**	**Analyze**
12.	**(i)**	Design a 4 bit BCD to Excess-3 code converter. **(8)**	**BTL 6**	**Create**
	(ii)	Draw the logic diagram of 1 to 4 line demultiplexer and discuss on it. **(5)**		
13.	Design a 3 x 8 decoder using 2 x 4 decoders and explain its operation as a minterm generator. **(13)**		**BTL 3**	**Apply**
14.	Deduce the following function using K-map: **(13)** F(A,B,C,D)= πM(0,2,3,8,9,12,13,15)		**BTL 3**	**Apply**
15.	Describe the combinational circuit which has single data input, three selection lines and 8 data outputs. Verify with truth table and logic diagram. **(13)**		**BTL 2**	**Understand**
16.	Implement the Boolean function using 4 : 1 multiplexer F (A, B, C) = ∑(1, 3, 6, 7) **(13)**		**BTL 3**	**Apply**
17.	Analyze and describe the following in detail **(i)** Performs subtraction on 2 binary inputs and produce two binary outputs as a difference and a borrow. **(6)** **(ii)** Performs subtraction on 3 binary inputs and produce output as a difference and a carry bit. **(7)**		**BTL 4**	**Analyze**
PART C				
1.	Realize the given Boolean function using two 4 : 1 MUX F (A, B, C, D) = ∑ m (0, 1, 2, 4, 6, 9, 12, 14) **(15)**		**BLT-5**	**Evaluate**
2.	**(i)**	Simplify the following function using Karnaugh Map.	**BTL 6**	**Create**

		F(W,X,Y,Z)=∑m(0,1,3,9,10,12,13,14)+ ∑d(2,5,6,11). **(7)**		
	(ii)	Generalize about the concepts of implicant, prime implicant, essential and non-essential prime implicant. Develop the K-map for the following function and test for all the possible solutions for the given function. F(A,B,C,D) = ∑m (0,1,4,5,13,14,15) **(8)**		
3.	Design a suitable multiplexer which has 3 selection lines, eight input lines and one output. Verify with truth table and logic diagram. **(15)**		**BTL 6**	**Create**
4.	**(i)**	Implement the following Boolean function using suitable multiplexer F (A, B, C) =∑m (1, 3, 5, 6). **(5)**	**BTL 5**	**Evaluate**
	(ii)	Assess a full adder using two half adders and an OR gate**.** **(10)**		
5.	Design a combinational logic circuit with three input variable A,B,C that will produce a output as 1 whenever the variable A or C , both A and C are logic 1. **(15)**		**BLT-5**	**Evaluate**

UNIT III - SYNCHRONOUS SEQUENTIAL CIRCUITS			
Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters - asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits – Moore and Melay models- Counters, state diagram; state reduction; state assignment.			
PART – A			
S.No	**Questions**	**BT Level**	**Competence**
1.	Construct the characteristic table of SR Flip Flop.	**BTL 6**	**Create**
2.	Give the characteristic equation and characteristic table of a T- flip-flop	**BTL 2**	**Understand**
3.	Draw the schematic of D flip flop.	**BTL 4**	**Analyze**
4.	Show how a RS FF can be built using NAND gates.	**BTL 3**	**Apply**
5.	What is Excitation table?	**BTL 1**	**Remember**
6.	Summarize the drawbacks of JK FF.	**BTL 5**	**Evaluate**
7.	Give the excitation table for T Flip Flop.	**BTL 2**	**Understand**
8.	Point out few applications of flip flop.	**BTL 4**	**Analyze**
9.	Distinguish between synchronous sequential circuits and asynchronous sequential circuits.	**BTL 3**	**Apply**
10.	Determine the characteristic equation of JK FF.	**BTL 5**	**Evaluate**
11.	Describe edge and level triggered FF.	**BTL 2**	**Understand**

12.	What is FSM state? List its two basic types.	**BTL 4**	**Analyze**
13.	List the applications of shift register.	**BTL 1**	**Remember**
14.	Classify sequential circuits.	**BTL 3**	**Apply**
15.	Write the benefits of state reduction.	**BTL 1**	**Remember**
16.	Define incompletely specified sequential circuit.	**BTL 1**	**Remember**
17.	Generalize the differences between combinational and sequential circuits.	**BTL 6**	**Create**
18.	Define Flip flop.	**BTL 1**	**Remember**
19.	Comment about ripple counter.	**BTL 2**	**Understand**
20.	Write the role of master clock generator in synchronous circuits.	**BTL 1**	**Remember**
21.	List the different types of flipflop.	**BTL 2**	**Understand**
22.	Compare Melay and Moore Circuit.	**BTL 3**	**Apply**
23.	How the race around condition can be avoided in JK flipflop?	**BTL 4**	**Analyze**
24.	Find the number of flip-flop needed to realize mod-16 counter.	**BTL 5**	**Evaluate**
	PART B		
1.	Draw and explain the operation of a Master-Slave JK flip flop. **(13)**	**BTL 2**	**Understand**
2.	Design a counter or the following state diagram. **(13)** 	**BTL 4**	**Analyze**
3.	Solve the following state equations to obtain a sequential circuit. **(13)** **A (t+1) =C⊕D; B (t+1) = A;** **C (t+1)= B; D (t+1)=C;**	**BTL 3**	**Apply**
4.	Explain the operation, state diagram and characteristics of a T-Flip flop. **(13)**	**BTL 4**	**Analyze**
5.	**(i)** Design a 2-bit synchronous sequential down counter.**(6)**	**BTL 1**	**Remember**
	(ii) Explain the operation of 3-bit shift register of any type. **(7)**		
6.	Identify a sequence detector that produces an output '1' whenever the non-overlapping sequence 101101 is detected. **(13)**	**BTL 1**	**Remember**
7.	**(i)** Analyze the circuit of a SR flip flop and realize SR flip flop using D flip flop. **(6)**	**BTL 1**	**Remember**

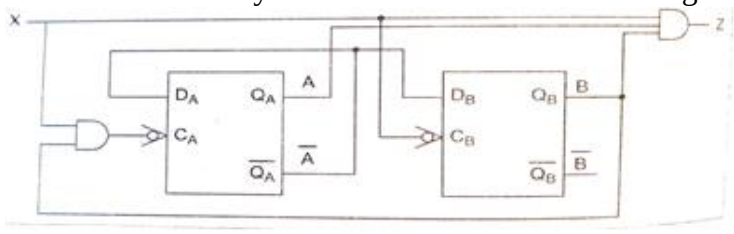
	(ii)	Explain a synchronous sequential circuit that goes through the count sequence 1,3,4,5 repeatedly. Use T flip flops for your design. **(7)**		
8.	Show the state transition diagram of a sequence detector circuit that detects '1010' from input data stream using Moore model. **(13)**		**BTL 3**	**Apply**
9.	**(i)**	Deduce a MOD-3 synchronous counter using JK flip flop. **(7)**	**BTL 5**	**Evaluate**
	(ii)	Evaluate a sequence detector to detect the sequence 101 using JK flip flop. **(6)**		
10.	Discuss about a 3 bit (MOD 8) Synchronous UP/Down counter with neat state diagram, state table, excitation table, K-map simplification and its circuit diagram. **(13)**		**BTL 2**	**Understand**
11.	Write a detailed note about shift registers with its types. **(13)**		**BTL 1**	**Remember**
12.	**(i)**	What is meant by state diagram? Define how state assignment is important in a sequential circuit design. Describe with a suitable example. **(7)**	**BTL 1**	**Remember**
13.	**(ii)**	Implement D and T FFs using JK flip flop. Tabulate the characteristics equation of the three flip flops. **(6)**		
14.	A sequential circuit with two D flip flops A and B, input X and output Y is specified by the following next state and output equations: **A (t+1) = AX+BX; B (t+1) = A'X; Y= (A+B) X'.** **(i)** Draw the logic diagram. **(4)** **(ii)** Construct the state table. **(5)** **(iii)** Draw the state diagram. **(4)**		**BTL 6**	**Create**
15.	Realize the logic diagram of D-FF using NAND gates and explain. **(13)**		**BTL 4**	**Analyze**
16.	Write down the characteristic equation and explain the operation of JK flip flop. **(13)**		**BTL 2**	**Understand**
17.	Assess the truth table of clocked SR flip flop with logic diagram. **(13)**		**BTL 3**	**Apply**
PART C				
1.	Design a sequential logic circuit that goes through the following sequence 0, 2, 4, 6, 8, 10, 12, 14 repeatedly. Use D flip-flops for the design. **(15)**		**BTL 5**	**Evaluate**
2.	Formulate a flip flop using NAND gates in which clock signal is directly connected to the JK flip flop and it is connected through inverter to the SR flip flop. Explain with neat block diagrams, timing diagram and logic diagrams. **(15)**		**BLT-5**	**Evaluate**
3.	Evaluate a Mealy state diagram that will detect a serial input sequence of 10110. The detection of the required bit pattern can occur in a longer data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause an output Z to be asserted high. **(15)**		**BTL 5**	**Evaluate**
4.	Design and implement MOD-12 Synchronous Down Counter using T Flip flop. **(15)**		**BLT-6**	**Create**

5.	**(i)**	Design and explain the working of a synchronous MOD-5 counter. **(8)**	**BTL 6**	**Create**
	(ii)	Design a T flip flop using JK flip flop. **(7)**		

UNIT IV- ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABLE LOGIC DEVICES			
Asynchronous sequential logic circuits-Transition table, flow table-race conditions, hazards &errors in digital circuits; analysis of asynchronous sequential logic circuits-introduction to Programmable Logic Devices: PROM – PLA –PAL, GAL and its implementation, CPLD-FPGA.			
PART – A			
S.No	**Questions**	**BT Level**	**Competence**
1.	Differentiate synchronous and asynchronous sequential circuits.	**BTL 2**	**Understand**
2.	Summarize the advantages and disadvantages of asynchronous sequential circuits.	**BTL 5**	**Evaluate**
3.	What happens to the information stored in a memory location after it has been read and write operation?	**BTL 3**	**Apply**
4.	Formulate the relationship between fundamental mode and pulse mode circuit.	**BTL 6**	**Create**
5.	Explain the purpose of primitive flow table.	**BTL 4**	**Analyze**
6.	Distinguish between stable and unstable state.	**BTL 4**	**Analyze**
7.	What do you mean by race around condition in a flip-flop?	**BTL 1**	**Remember**
8.	Illustrate the concept of critical race. Why should it be avoided?	**BTL 3**	**Apply**
9.	Explain about non-critical race. Mention its cause.	**BTL 5**	**Evaluate**
10.	Define Static -1- Hazard.	**BTL 2**	**Understand**
11.	State the difference between static 0 and static 1 hazard.	**BTL 4**	**Analyze**
12.	How to detect and eliminate hazards from an asynchronous network.	**BTL 2**	**Understand**
13.	What is meant by fusible link? List the types of fuse technologies used in PROM.	**BTL 1**	**Remember**
14.	Design a hazard free circuit to implement the following function. F (A, B, C, D) = ∑m (1,3,4,5,6,7,9,11,15)	**BTL 6**	**Create**
15.	Draw the structure of PAL.	**BTL 1**	**Remember**
16.	Mention the types of Hazards in logic circuits.	**BTL 3**	**Apply**
17.	Define PLA. How it differs from PROM?	**BTL 1**	**Remember**
18.	List the applications of PLA.	**BTL 1**	**Remember**

19.	List the types of PLD.	**BTL 1**	**Remember**
20.	Draw the block diagram of asynchronous sequential circuits.	**BTL 2**	**Understand**
21.	What is Static-0- hazard	**BTL 2**	**Understand**
22.	Differentiate between Programmable Logic Array and Programming Array Logic.	**BTL 3**	**Apply**
23.	Draw the block diagram of PLA	**BTL 4**	**Analyze**
24.	Evaluate the function $F_1=\sum$ (0, 1, 2, 5, 7) and $F_2=\sum$ (1, 2, 4, 6) using PROM.	**BTL 5**	**Evaluate**
	PART B		
1.	**(i)** List out the steps involved in the design procedure of an asynchronous sequential circuit. **(5)**	**BTL 1**	**Remember**
	(ii) When do you get the critical and non-critical race? How will you obtain race free conditions? **(8)**		
2.	Design an asynchronous sequential circuit (with detailed steps involved) that has 2 inputs x_1 and x_2 and one output z. The circuit is required to give an output z=1 when x_1 =1, x_2 =1 and x_1 =1 being first. **(13)**	**BTL 6**	**Create**
3.	**(i)** What is hazard? Explain hazards in digital circuits. **(7)**	**BTL 1**	**Remember**
	(ii) Implement the following logic and analyse for the pressure of any hazard f=x1x2 + x'1x3. If hazard is present briefly explain the type of hazard and design a hazard-free circuit. **(6)**		
4.	**A**n asynchronous sequential circuit is described by the following excitation and output function, $Y=x_1 x_2 +(x_1+x_{2)}y$ Z= y **(i)** Predict the logic diagram of the circuit. **(3)** **(ii)** Interpret the transition table and the output map. **(7)** **(iii)**Obtain its flow table. **(3)**	**BTL 2**	**Understand**
5.	Deduce an asynchronous network that has two inputs x_1 and x_2 and one output z. The circuit is required to give an output whenever the input sequence (0, 0), (0, 1), (1, 1) received but only in that order. **(13)**	**BTL 5**	**Evaluate**
6.	Describe the operation of SR latch using universal gates. **(13)**	**BTL 1**	**Remember**
7.	Using PROM, examine the following expression. **(13)** $F_1(A,B,C)= \sum$ (0, 1, 3, 5, 7) $F_2(A,B,C)=\sum$ (1, 2, 5, 6)	**BTL 4**	**Analyze**
8.	Analyze a circuit with primary inputs A and B to give an output Z equal to 1 when A becomes 1 if B is already 1. Once Z=1 it will remain so until A goes to 0. Draw the total state diagram, primitive flow table for designing this circuit. **(13)**	**BTL 4**	**Analyze**
9.	Describe about the following programmable logic devices: **(i)** PLA **(7)** **(ii)** PAL **(6)**	**BTL 1**	**Remember**

10.	**(i)**	Express the following function using PLA. F (W, X, Y, Z) = π (0, 3, 5, 7, 12, 15) + d (2, 9). **(6)**	**BTL 2**	**Understand**
	(ii)	Explain the structure of CPLD with the help of a block diagram. **(7)**		
11.	**(i)**	What are static-0 and static-1 hazards? Show the removal of hazards using hazard covers in K-map. **(7)**	**BTL 3**	**Apply**
	(ii)	Examine cycles and races in asynchronous sequential circuits. **(6)**		
12.	For the given Boolean function, sketch the hazard free circuit. F(A,B,C,D) = ∑m(1,3,6,7,13,15). **(13)**		**BTL 3**	**Apply**
13.	Analyze a BCD to Excess-3 code converter and implement using suitable PLA. **(13)**		**BTL 4**	**Analyze**
14.	Consider an asynchronous sequential circuit described by $Y= x_1 x'_2 + (x_1 + x'_2) y$; Z=Y, where Y and Z are excitation and output functions respectively. **(i)** Give the logic diagram of the circuit. **(3)** **(ii)** Interpret the transition table and output map. **(7)** **(iii)**Obtain its flow table. **(3)**		**BTL 2**	**Understand**
15.	Give the hazard free realization for the following Boolean function. **(i)** F(A,B,C,D) = $\sum m$ (0, 1, 5, 6, 7, 9, 11) **(6)** **(ii)** F(W,X,Y,Z) = $\sum m$ (0, 2, 6, 7, 8, 10, 12) **(7)**		**BTL 3**	**Apply**
16.	Write concise notes in detail about **(i)** Hazards **(6)** **(ii)** Dynamic Hazards **(7)**		**BLT-1**	**Remember**
17.	Solve the following function using PAL and PLA. F(X, Y, Z) = ∑m (0,1,3,4,6,7) **(13)**		**BTL 3**	**Apply**
PART C				
1.	A combinational logic circuit is generalized by the following function F_1(A,B,C) = ∑m (0,1,6,7), F_2(A,B,C)= ∑m (2,3,5,7). Assess the circuit with a PAL having three inputs, product terms and two outputs. **(15)**		**BTL 5**	**Evaluate**
2.	Design an asynchronous sequential circuit with two inputs x1 and x2 and one output Z. Initially, both inputs are equal to zero. When x1 or x2 becomes 1, the output Z becomes 1. When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state. **(15)**		**BTL 6**	**Create**
3.	Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions. F_1(A,B,C)= ∑ (0, 1, 2, 4) F_2(A,B,C)=∑ (0, 5, 6, 7) **(15)**		**BTL 5**	**Evaluate**
4.	Design an asynchronous sequential circuit that has two internal states and one output. The excitation and output function describing the circuit are as follows:		**BTL 6**	**Create**

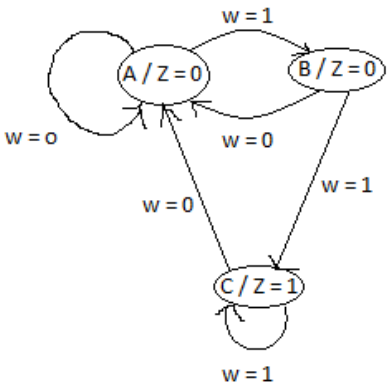
	$Y_1=x_1 x_2 +x_1y_2 +x_2y_1$ $Y_2=x_2+x_1y_1y_2 +x_1y_1$ $Z= x_2+y_1$ **(i)** Predict the logic diagram of the circuit. **(4)** **(ii)** Interpret the transition table and the output map. **(7)** **(iii)** Obtain its flow table. **(4)**		
5.	Consider the asynchronous sequential circuit driven by the pulse shown below. Analyse the circuit and draw the timing diagram.  **(15)**	**BLT-6**	**Create**

UNIT V- VHDL			
RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages –Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip-flops, FSM, Multiplexers /Demultiplexers).			
PART – A			
S.No	**Questions**	**BT Level**	**Competence**
1.	List the languages that are combined together to get VHDL language.	**BTL 1**	**Remember**
2.	State the need for VHDL. List out the operators available in VHDL.	**BTL 1**	**Remember**
3.	Name the modeling techniques available in HDL.	**BTL 1**	**Remember**
4.	What are the languages that are combined together to get VHDL language?	**BTL 1**	**Remember**
5.	Illustrate about variable class.	**BTL 3**	**Apply**
6.	Define data flow modeling in VHDL. Give its basic mechanism.	**BTL 1**	**Remember**
7.	Classify the different types of test bench.	**BTL 3**	**Apply**
8.	Write the VHDL code for a 2X1 multiplexer using behavioural modelling.	**BTL 5**	**Evaluate**
9.	Interpret the VHDL code for a logic gate which gives high output only when both the inputs are high.	**BTL 2**	**Understand**
10.	Give the syntax for package declaration and package body in VHDL.	**BTL 2**	**Understand**
11.	Write the VHDL behavioural model for D flip-flop.	**BTL 5**	**Evaluate**
12.	Give the HDL code for half adder.	**BTL 2**	**Understand**

13.	Describe the VHDL code for AND gate.	**BTL 2**	**Understand**
14.	Differentiate between a signal and variable.	**BTL 4**	**Analyze**
15.	Define modularity.	**BTL 1**	**Remember**
16.	Write a VHDL program for an EX-NOR gate using behavioural coding.	**BTL 6**	**Create**
17.	Explain 'block' statement in VHDL with an example.	**BTL 4**	**Analyze**
18.	Design a 2 bit counter in VHDL.	**BTL 6**	**Create**
19.	Illustrate 'case' statement in VHDL.	**BTL 3**	**Apply**
20.	Differentiate between function and procedure in VHDL.	**BTL 4**	**Analyze**
21.	What is HDL?	**BTL 2**	**Understand**
22.	Examine logic synthesis and simulation.	**BTL 3**	**Apply**
23.	Analyze the operator precedence of Verilog HDL.	**BTL 4**	**Analyze**
24.	Write the VHDL code for a half subtractor using any model.	**BTL 5**	**Evaluate**

PART-B

1.	Write the VHDL code for MOD-6 counter using JK flip flops. **(13)**		**BTL 1**	**Remember**
2.	Explain in detail about the various programming constructs used in VHDL for designing a logic circuit. **(13)**		**BTL 4**	**Analyze**
3.	Describe the modeling techniques available in HDL. Give the VHDL code to realize a full adder using Behavioural modeling. **(13)**		**BTL 2**	**Understand**
4.	List the different data objects available in VHDL and model a 3-bit comparator using Structural modeling. **(13)**		**BTL 1**	**Remember**
5.	Summarize in detail the concept of structural modeling in VHDL with an example of full adder. **(13)**		**BTL 2**	**Understand**
6.	What are the components in VHDL? Show step by step how a NOR gate component can be created and added in the library. **(13)**		**BTL1**	**Remember**
7.	**(i)**	Explain the various operations supported by VHDL. **(7)**	**BTL1**	**Remember**
	(ii)	Write the VHDL code to realize a decade counter with behavioral modeling. **(6)**		
8.	Analyze a full adder and half subtractor in data flow modeling using VHDL. Explain in detail. **(13)**		**BTL 4**	**Analyze**
9.	**(i)**	Define VHDL Package. List the types and explain in detail. **(6)**	**BTL 1**	**Remember**
	(ii)	Write a VHDL program for 1x4 De-Mux using dataflow modeling. **(7)**		

10.	Explain in detail the design procedure for register transfer language. **(13)**		**BTL 4**	**Analyze**
11.	**(i)**	Construct a VHDL module for a JK flip flop. **(7)**	**BTL 3**	**Apply**
	(ii)	Illustrate how arithmetic and logic operations are expressed using RTL. **(6)**		
12.	**(i)**	Generalize the terms functions and subprograms with suitable examples. **(5)**	**BTL 6**	**Create**
	(ii)	Develop the VHDL code to realize a 4-bit parallel binary adder with structural modeling. **(8)**		
13.	Explain briefly about VHDL test benches. **(6)**		**BTL 5**	**Evaluate**
14.	Design a 4 x 4 array multiplier and write the VHDL code to realize it using structural modeling. **(13)**		**BTL 3**	**Apply**
15.	Enumerate in detail about Hardware description language (HDL) which is used to describe the structure and behaviour of electronic digital circuits. **(13)**		**BTL 2**	**Understand**
16.	Explain in detail about Operators in Verilog HDL. Write a Verilog code for half adder circuit. **(13)**		**BTL 3**	**Apply**
17.	Describe the VHDL coding for 8 x 1 Multiplexer. **(13)**		**BTL 3**	**Apply**
	PART C			
1.	Create a VHDL module listing for a 16:1 MUX that is based on the assign statement. Use a 4-bit select word (S_3, S_2, S_1, and S_0) to map the selected input P_i (i=0, 1….15) to the output**.** **(15)**		**BTL 6**	**Create**
2.	Assess the VHDL code for Binary UP/DOWN counter using JK flip flops. **(15)**		**BTL 5**	**Evaluate**
3.	Compare the VHDL code for full subtractor in structural modeling and data flow modeling. **(15)**		**BTL 5**	**Evaluate**
4.	Write the VHDL code for the given state diagram, using behavioural modeling. Design it using one-hot state assignment and implement it using PAL. **(15)** 		**BTL 6**	**Create**
5.	Test the VHDL code for half subtractor using structural modelling. **(15)**		**BTL 5**	**Evaluate**