SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)
SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VIII SEMESTER
1906004 ELECTRONICS PACKAGING AND TESTING
Regulation – 2019

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SUBJECT : 1906004 Electronics Packaging and Testing

SEM / YEAR: VIII/ IV year B.E. ECE

	UNIT - I: OVERVIEW OF ELECTRONIC SYSTEMS PACKAGING			
	Functions of an Electronic Package, Packaging Hierarchy, IC packaging: MEMS packaging, consumer electronics packaging, medical electronics packaging, Trends, Challenges, Driving Forces on Packaging Technology, Materials for Microelectronic packaging, Packaging Material Properties, Ceramics, Polymers, and Metals in Packaging, Material for high density interconnect substrates..			
	PART – A (2 marks)			
Q. No	Questions	CO	BT Level	Competence
1	What are the primary functions of an electronic package?	CO1	BTL 1	Remembering
2	Write about the concept of packaging hierarchy in electronic systems.	CO1	BTL 1	Remembering
3	Differentiate between IC packaging and MEMS packaging.	CO1	BTL 2	Understanding
4	How does packaging impact consumer electronics in terms of performance and durability?	CO1	BTL 1	Remembering
5	List the critical aspects of packaging in medical electronics.	CO1	BTL 1	Remembering
6	What are the current trends and major challenges faced in electronic packaging?	CO1	BTL 1	Remembering
7	Identify the key driving forces influencing advancements in packaging technology.	CO1	BTL 1	Remembering
8	Name the main categories of materials used in microelectronic packaging.	CO1	BTL 2	Understanding
9	What properties are crucial in selecting packaging materials?	CO1	BTL 2	Understanding
10	Illustrate the role of ceramics in electronic packaging.	CO1	BTL 2	Understanding
11	How are polymers utilized in electronic packaging?	CO1	BTL 1	Remembering
12	Mention the significance of metals in electronic packaging.	CO1	BTL 1	Remembering
13	What are the specific material requirements for high-density interconnect substrates?	CO1	BTL 2	Understanding
14	Summarize the working principle of flip-chip technology in IC packaging.	CO1	BTL 1	Remembering
15	What is wafer-level packaging, and what advantages does it offer?	CO1	BTL 1	Remembering
16	Interpret the concept of 3D packaging in microelectronics.	CO1	BTL 1	Remembering
17	Why is hermetic sealing essential in certain electronic packages?	CO1	BTL 1	Remembering
18	Analyze the environmental considerations associated with	CO1	BTL 2	Understanding

	electronic packaging.			
19	What are the key reliability tests conducted on electronic packages?	CO1	BTL 2	Understanding
20	Name two emerging technologies shaping the future of electronic packaging.	CO1	BTL 2	Understanding
21	Why is the dielectric constant crucial in substrate materials?	CO1	BTL 2	Understanding
22	What are the specific challenges encountered in MEMS packaging compared to traditional IC packaging?	CO1	BTL 2	Understanding
23	Explain the significance of thermal management in electronic packaging.	CO1	BTL 2	Understanding
24	Why is material selection critical for biocompatibility in medical electronics packaging?	CO1	BTL 2	Understanding
	PART- B (13 marks)			
1	Define the primary functions served by an electronic package and describe its hierarchy.	CO1	BTL 3	Applying
2	Explain how hermetic sealing plays a critical role in safeguarding sensitive electronic components.	CO1	BTL 3	Applying
3	Identify the key reliability tests conducted on electronic packages.	CO1	BTL 3	Applying
4	Examine the significance of material selection in medical electronics packaging for biocompatibility.	CO1	BTL 3	Applying
5	Describe the significance of packaging hierarchy in the context of electronic systems.	CO1	BTL 4	Analyzing
6	Compare and contrast IC packaging with MEMS packaging, highlighting their distinctive features and applications.	CO1	BTL 4	Analyzing
7	Explore the role of materials like metals, ceramics, and polymers in electronic packaging, emphasizing their specific contributions.	CO1	BTL 4	Analyzing
8	What is the role of packaging in MEMS products?	CO1	BTL 4	Analyzing
9	Illustrate how materials like ceramics and polymers are practically utilized in electronic packaging.	CO1	BTL 3	Applying
10	Design a hypothetical high-density interconnect substrate, specifying material requirements and their rationale.	CO1	BTL 3	Applying
11	Formulate a future-oriented packaging strategy for emerging technologies, integrating embedded packaging techniques and novel materials.	CO1	BTL 3	Applying
12	Apply the concept of 3D packaging to a specific electronic device, outlining potential advantages and challenges.	CO1	BTL 3	Applying
13	How does packaging contribute to the functionality and protection of electronic components used in medical devices?	CO1	BTL 4	Analyzing
14	Investigate the material properties crucial for selecting appropriate packaging materials, emphasizing their roles in electronic packaging.	CO1	BTL 4	Analyzing

15	Develop a comprehensive plan for effective thermal management in electronic packaging, considering diverse environmental conditions.	CO1	BTL 4	Analyzing
16	How does packaging design cater to the specific demands of consumer electronics, particularly in achieving ultra-portability while accommodating the unique characteristics of these products?	CO1	BTL 4	Analyzing
17	Analyze the impact of packaging on the durability and performance of consumer electronics, citing specific examples.	CO1	BTL 4	Analyzing
	PART – C (15 marks)			
1	Describe the Mobile phone system technology with a neat block diagram?	CO1	BTL 3	Applying
2	Explain the role and significance of ceramics, polymers, and metals in microelectronic packaging.	CO1	BTL 3	Applying
3	Discuss the essential material requirements for high-density interconnect substrates in electronics packaging.	CO1	BTL 3	Applying
4	Compare and contrast IC packaging and MEMS packaging, highlighting their distinctive characteristics in electronics packaging.	CO1	BTL 4	Analyzing
5	Analyze the contemporary challenges encountered in consumer electronics packaging and how technological advancements influence this field.	CO1	BTL 4	Analyzing

	UNIT - II: ELECTRICAL ISSSUES IN PACKAGING			
	Electrical Issues of Systems Packaging, Signal Distribution, Power Distribution, Electromagnetic Interference, Transmission Lines, Clock Distribution, Noise Sources, Digital and RF Issues. Design Process Electrical Design: Interconnect Capacitance, Resistance and Inductance fundamentals; Packaging roadmaps - Hybrid circuits - Resistive, Capacitive and Inductive parasitic.			
	PART- A (2 marks)			
Q. No	Questions	CO	BT Level	Competence
1.	Define the concept of signal distribution in electronics packaging.	CO2	BTL 1	Remembering
2.	List the primary sources of noise affecting electronic systems.	CO2	BTL 1	Remembering
3.	Recall the fundamental characteristics of transmission lines in electronics packaging.	CO2	BTL 1	Remembering
4.	State the main aspects of power distribution in systems packaging.	CO2	BTL 1	Remembering
5.	Outline the key issues related to electromagnetic interference (EMI) in packaging.	CO2	BTL 1	Remembering
6.	Enumerate the key aspects of clock distribution challenges in electronic systems.	CO2	BTL 1	Remembering
7.	How interconnect capacitance influences electrical design in packaging?	CO2	BTL 2	Understanding
8.	Outline the fundamentals of resistance in the context of electronics packaging.	CO2	BTL 2	Understanding
9.	Elucidate the significance of inductance in electrical design within	CO2	BTL 2	Understanding

	packaging systems.			
10.	Interpret the concept of packaging roadmaps and their relevance in electronics.	CO2	BTL 2	Understanding
11.	Discuss the role of hybrid circuits in addressing resistive, capacitive, and inductive parasitics.	CO2	BTL 2	Understanding
12.	Write a note on digital and RF issues encountered in electronic packaging.	CO2	BTL 2	Understanding
13.	Discuss strategies to mitigate electromagnetic interference (EMI) in packaging applications.	CO2	BTL 1	Remembering
14.	Apply the concepts of transmission lines to resolve signal integrity issues in electronics packaging.	CO2	BTL 1	Remembering
15.	Summarize the plan to optimize power distribution for enhanced system performance.	CO2	BTL 1	Remembering
16.	Mention the methods to minimize noise sources affecting electronic systems within packaging.	CO2	BTL 1	Remembering
17.	Illustrate the design approach to address interconnect capacitance challenges in packaging.	CO2	BTL 1	Remembering
18.	Devise a strategy to manage clock distribution challenges in electronic packaging.	CO2	BTL 1	Remembering
19.	Analyze the impact of parasitic elements (resistive, capacitive, inductive) on packaging design and functionality.	CO2	BTL 2	Understanding
20.	Assess the trade-offs between signal distribution methods in electronics packaging.	CO2	BTL 2	Understanding
21.	How do the different approaches address electromagnetic interference (EMI) in packaging.	CO2	BTL 2	Understanding
22.	Elaborate in short the effectiveness of transmission line solutions in reducing signal degradation in packaging.	CO2	BTL 2	Understanding
23.	Intrepret the challenges posed by digital versus RF issues in electronics packaging.	CO2	BTL 2	Understanding
24.	Investigate the role of electrical design in influencing packaging roadmaps for emerging technologies.	CO2	BTL 2	Understanding
	PART – B (13 marks)			
1.	Evaluate the fundamentals of electrical packaging design?	CO2	BTL 3	Applying
2.	Summarize the fundamentals of transmission lines in electronic packaging.	CO2	BTL 3	Applying
3.	Apply the key characteristics of clock distribution challenges in electronic systems.	CO2	BTL 3	Applying
4.	Recall the primary sources of noise affecting electronic systems within packaging.	CO2	BTL 3	Applying
5.	Explain the electrical anatomy of systems packaging?	CO2	BTL 4	Analyzing
6.	Describe how resistive, capacitive, and inductive parasitic elements impact hybrid circuits in packaging.	CO2	BTL 4	Analyzing

7.	Elaborate on the significance of signal distribution in devices with respect to systems packaging?	CO2	BTL 4	Analyzing
8.	Elucidate the role of packaging roadmaps in guiding design processes for electronic systems.	CO2	BTL 4	Analyzing
9.	Summarize the effective strategies to mitigate electromagnetic interference (EMI) within packaging applications.	CO2	BTL 4	Analyzing
10.	Elaborate the optimization of power distribution for enhanced system performance.	CO2	BTL 3	Applying
11.	Explain the comprehensive design approach to address interconnect capacitance challenges in electronic packaging.	CO2	BTL 3	Applying
12.	Devise a strategic plan to manage clock distribution challenges effectively in electronic packaging.	CO2	BTL 3	Applying
13.	Enumerate the electrical design procedure of the package.	CO2	BTL 4	Analyzing
14.	Analyze the inductive effects in packaging industry.	CO2	BTL 4	Analyzing
15.	Compare and contrast the challenges posed by digital and RF issues in electronics packaging.	CO2	BTL 4	Analyzing
16.	Assess various noise sources affecting electronic systems within packaging and their implications.	CO2	BTL 4	Analyzing
17.	Categorize the approaches to minimize electromagnetic interference (EMI) in packaging applications.	CO2	BTL 4	Analyzing
	PART – C (15 marks)			
1.	Consider a package that has a power supply inductance of 10pH and has to support the switching of 1000 on-chip circuits. This circuit draw 10A of current in time 0.25ns. Calculate the power supply noise voltage. Devise a method to reduce the power supply noise voltage to 200mV.	CO2	BTL 4	Analyzing
2.	Elaborate on the role of transmission lines in mitigating signal degradation within electronic packaging.	CO2	BTL 4	Analyzing
3.	Evaluate the effectiveness of strategies used to manage electromagnetic interference (EMI) in packaging.	CO2	BTL 3	Applying
4.	Explain the significance of signal distribution in the context of electrical issues encountered in packaging.	CO2	BTL 3	Applying
5.	Define the fundamental concept of 'Electromagnetic Interference' and its relevance to packaging electronics.	CO2	BTL 3	Applying

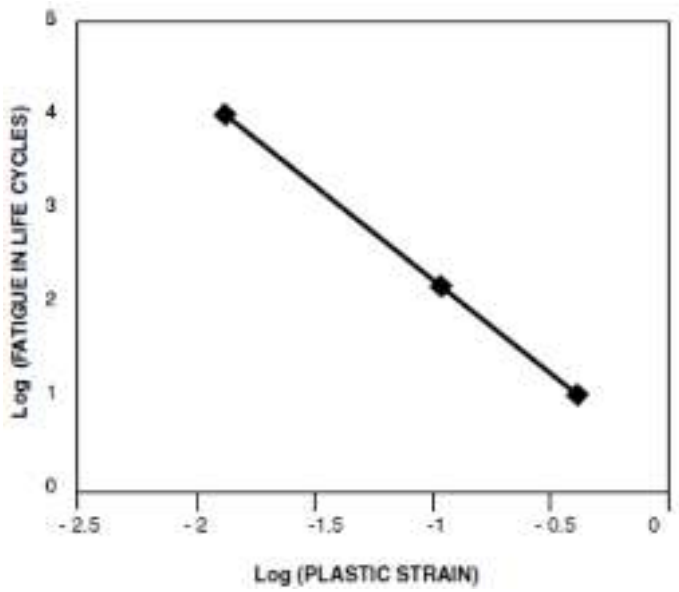
	UNIT - III: CHIP PACKAGES			
	IC Assembly - Purpose, Requirements, Technologies, Wire bonding, Tape Automated Bonding, Flip Chip, Wafer Level Packaging, reliability, wafer level burn – in and test. Single chip packaging: functions, types, materials processes, properties, characteristics, trends. Multi chip packaging: types, design, comparison, trends. System in - package (SIP); Passives: discrete, integrated, and embedded.			
	PART A (2 marks)			
Q. No	Questions	CO	BT Level	Competence
1.	Define IC Assembly and its primary purpose in chip packaging.	CO3	BTL 1	Remembering
2.	Write about the technologies used in IC Assembly.	CO3	BTL 1	Remembering
3.	Recall the various bonding methods employed in chip packaging.	CO3	BTL 1	Remembering
4.	What are the characteristics of wafer-level burn-in and test in chip packaging?	CO3	BTL 1	Remembering
5.	List the functions of single-chip packaging.	CO3	BTL 1	Remembering
6.	What are the key properties associated with materials used in single-chip packaging?	CO3	BTL 1	Remembering
7.	Interpret the requirements for IC Assembly in chip packaging.	CO3	BTL 2	Understanding
8.	Name the types and processes involved in single-chip packaging.	CO3	BTL 2	Understanding
9.	Elaborate on the design variations in multi-chip packaging.	CO3	BTL 2	Understanding
10.	Understand the differences between integrated and embedded passives in chip packaging.	CO3	BTL 2	Understanding
11.	How do wafer-level packaging and tape automated bonding differ in chip packaging?	CO3	BTL 2	Understanding
12.	How do materials and processes influence the characteristics of single-chip packaging?	CO3	BTL 2	Understanding
13.	Apply the principles of wire bonding in a chip packaging scenario.	CO3	BTL 1	Remembering
14.	Summarize the plan for reliable wafer-level packaging in chip production.	CO3	BTL 1	Remembering
15.	Outline the chip packaging strategy utilizing flip-chip technology.	CO3	BTL 1	Remembering
16.	Mention the methods to enhance the reliability of single-chip packaging.	CO3	BTL 1	Remembering
17.	How would you implement integrated passives in a system-in-package (SIP)?	CO3	BTL 2	Understanding
18.	Apply the knowledge of materials and trends to create an innovative chip packaging solution.	CO3	BTL 2	Understanding
19.	Analyze the advantages and disadvantages of tape automated bonding in chip packaging.	CO3	BTL 2	Understanding
20.	Compare and contrast the design aspects of single-chip and multi-chip packaging.	CO3	BTL 2	Understanding
21.	Inspect the reliability concerns associated with wafer-level burn-in and test in chip packaging.	CO3	BTL 1	Remembering

22.	Assess the impact of different bonding methods on chip packaging reliability.	CO3	BTL 1	Remembering
23.	Examine the role of passives (discrete, integrated, embedded) in chip packaging.	CO3	BTL 2	Understanding
24.	Analyze the evolving trends in chip packaging and their potential implications.	CO3	BTL 2	Understanding
	PART – B (13 marks)			
1.	What is the primary requirements of IC Assembly in chip packaging?	CO3	BTL 3	Applying
2.	Describe the Failure mechanisms, its accelerating factors, and design for reliability?	CO3	BTL 3	Applying
3.	Describe a bonding method used specifically in wafer-level packaging.	CO3	BTL 3	Applying
4.	(i)What is Single chip IC packaging and list out its functions? (7) (ii)Mention the types of Single Chip IC Packages? (6)	CO3	BTL 3	Applying
5.	Discuss the distinct functions associated with multichip model?	CO3	BTL 4	Analyzing
6.	Compare the materials and processes used in different types of single-chip packaging.	CO3	BTL 4	Analyzing
7.	Outline the design considerations for multi-chip packaging and discuss their impact.	CO3	BTL 4	Analyzing
8.	Differentiate between discrete and integrated passives in chip packaging.	CO3	BTL 4	Analyzing
9.	How does tape automated bonding differ from flip-chip technology in chip packaging?	CO3	BTL 4	Analyzing
10.	Develop a reliability plan specifically for wafer-level packaging during chip production.	CO3	BTL 3	Applying
11.	Suggest strategies to enhance bonding method reliability in chip packaging.	CO3	BTL 3	Applying
12.	Explain the concept of wire bonding and the process involved in packaging? State its advantages and disadvantages?	CO3	BTL 3	Applying
13.	Analyze the feasibility of implementing system-in-package (SIP) solutions for chip packaging.	CO3	BTL 4	Analyzing
14.	Evaluate the impact of embedded passives on chip packaging advancements.	CO3	BTL 4	Analyzing
15.	Explore the foreseeable trends in chip packaging and their anticipated technological influences.	CO3	BTL 4	Analyzing
16.	Evaluate the challenges associated with ensuring the reliability of flip-chip technology in chip packaging.	CO3	BTL 4	Analyzing
17.	Compare the advantages and disadvantages of single-chip versus multi-chip packaging in the context of chip technologies.	CO3	BTL 4	Analyzing

	PART-C (15 marks)			
1	Define the primary purpose of IC Assembly in chip packaging.	CO3	BTL 3	Applying
2	Explain the IC assembly technologies with illustrative diagrams.	CO3	BTL 4	Analyzing
3	Apply the principles of wire bonding in a chip packaging scenario.	CO3	BTL 3	Applying
4	Analyze the evolving trends in multi-chip packaging and their potential impact on chip technologies.	CO3	BTL 4	Analyzing
5	Assess the reliability concerns associated with flip-chip technology in single-chip packaging.	CO3	BTL 4	Analyzing

	UNIT IV PCB, SURFACE MOUNT TECHNOLOGY AND THERMAL CONSIDERATIONS			
	Printed Circuit Board: Anatomy, CAD tools for PCB design, Standard fabrication, Micro via Boards. Board Assembly: Surface Mount Technology, Through Hole Technology, Process Control and Design challenges. Thermal Management, Heat transfer fundamentals, Thermal conductivity and resistance, Conduction, convection and radiation – Cooling requirements.			
	PART A (2 marks)			
Q. No	Questions	CO	BT Level	Competence
1.	Define Printed Circuit Board (PCB) and list its basic anatomy.	CO4	BTL 1	Remembering
2.	List the commonly used CAD tools for PCB design.	CO4	BTL 1	Remembering
3.	Recall the standard fabrication processes involved in PCB manufacturing.	CO4	BTL 1	Remembering
4.	Identify the features of Micro via Boards.	CO4	BTL 1	Remembering
5.	Write the differences between Surface Mount Technology and Through Hole Technology in board assembly.	CO4	BTL 1	Remembering
6.	Point out the challenges in process control encountered in board assembly.	CO4	BTL 1	Remembering
7.	Interpret the fundamentals of heat transfer in thermal management.	CO4	BTL 2	Understanding
8.	Outline the concepts of thermal conductivity and resistance in relation to PCBs.	CO4	BTL 2	Understanding
9.	What are the cooling requirements in the context of conduction, convection, and radiation.	CO4	BTL 2	Understanding
10.	How do CAD tools impact PCB design challenges?	CO4	BTL 2	Understanding
11.	Mention the advantages of Micro via Boards in comparison to standard PCBs.	CO4	BTL 2	Understanding
12.	Apply the principles of Surface Mount Technology in a board assembly scenario.	CO4	BTL 2	Understanding
13.	Develop a process control plan to mitigate challenges in Through Hole Technology.	CO4	BTL 1	Remembering
14.	Propose a thermal management strategy for a PCB considering heat transfer fundamentals.	CO4	BTL 1	Remembering
15.	Evaluate the suitability of different cooling methods for specific PCB designs.	CO4	BTL 1	Remembering

16.	Analyze the impact of design challenges on PCB fabrication and assembly.	CO4	BTL 1	Remembering
17.	Summarize the efficiency of CAD tools in addressing design challenges in PCB manufacturing.	CO4	BTL 1	Remembering
18.	Compare the thermal conductivity of various materials used in PCBs.	CO4	BTL 1	Remembering
19.	Evaluate the reliability issues associated with Micro via Boards.	CO4	BTL 2	Understanding
20.	Examine the trade-offs between Surface Mount Technology and Through Hole Technology in board assembly.	CO4	BTL 2	Understanding
21.	Analyze the influence of heat transfer principles on PCB performance and longevity.	CO4	BTL 2	Understanding
22.	Critique the limitations of standard PCBs concerning miniaturization and complex designs.	CO4	BTL 2	Understanding
23.	Assess the impact of thermal management on overall PCB functionality.	CO4	BTL 2	Understanding
24.	Evaluate the role of process control in minimizing defects in PCB fabrication and assembly.	CO4	BTL 2	Understanding
	PART – B (13 marks)			
1.	Describe the types of Printed Circuit Board (PCB)?	CO4	BTL 3	Applying
2.	List and explain the three CAD tools commonly used for PCB design.	CO4	BTL 3	Applying
3.	Explain the role of thermal conductivity in PCBs.	CO4	BTL 3	Applying
4.	Define the concept of process control in PCB manufacturing.	CO4	BTL 3	Applying
5.	What are the fundamental parameters of Printed Wiring Board and explain in detail?	CO4	BTL 4	Analyzing
6.	Compare and contrast Surface Mount Technology and Through Hole Technology in PCB assembly.	CO4	BTL 4	Analyzing
7.	Explain the principles of heat transfer and their relevance to thermal management in PCBs.	CO4	BTL 4	Analyzing
8.	Describe the process control measures adopted to address design flaws during PCB fabrication.	CO4	BTL 4	Analyzing
9.	Explain the plan to implement Surface Mount Technology in a PCB assembly line.	CO4	BTL 3	Applying
10.	Illustrate the methods to enhance thermal conductivity in a PCB design.	CO4	BTL 3	Applying
11.	Design a process control strategy for Micro via Boards fabrication.	CO4	BTL 3	Applying
12.	Devise a process flow for fabricating a double-sided through-hole connected PWB.	CO4	BTL 3	Applying

13.	In a low-cycle fatigue test of a solder joint, the logarithmic fatigue cycle as a function of logarithmic plastic strain is given by Figure below.  Assume that the solder joints obey the Coffin-Manson frequency-modified equation. Determine the constants Θ and η such that the frequency is equal to 0.3 s^{-1} and K=0?	CO4	BTL 4	Analyzing
14.	Analyze the relationship between PCB layout complexity and its impact on heat dissipation efficiency.	CO4	BTL 4	Analyzing
15.	Evaluate the effectiveness of various process control techniques in minimizing PCB manufacturing errors.	CO4	BTL 4	Analyzing
16.	Compare and contrast the thermal management capabilities between Surface Mount Technology and Through Hole Technology in PCBs.	CO4	BTL 4	Analyzing
17.	Assume that a Si-chip with a thermal expansion of coefficient of 2.6 ppm/ ℃ assembled with eutectic soldering flip chip technique on an FR-4 board with a thermal expansion of coefficient of 16 ppm/℃. The stand-off height after soldering is 50μm. The chip edge length is 20 mm and the temperature varies from -40 to +125℃. Calculate the total shear strain during the temperature cycling in this interval for the solder joint. Assume the ideal case where all the deformation is taken up by the solder joint.	CO4	BTL 4	Analyzing
	PART-C (15 marks)			
1	Describe the chart comparing the Key packaging materials, processes and its properties.	CO4	BTL 3	Applying
2	Explain the role of thermal conductivity in managing heat dissipation in PCBs.	CO4	BTL 4	Analyzing

3	Devise a strategy to optimize cooling requirements for a specific PCB design scenario.	CO4	BTL 3	Applying
4	Analyze the effectiveness of Surface Mount Technology versus Through Hole Technology in PCB assembly.	CO4	BTL 4	Analyzing
5	Evaluate the impact of Micro via Boards on reducing PCB size and enhancing circuit density.	CO4	BTL 4	Analyzing

	UNIT V TESTING			
	Reliability, Basic concepts, Environmental interactions. Thermal mismatch and fatigue – failures – thermo mechanically induced –electrically induced – chemically induced. Electrical Testing: System level electrical testing, Interconnection tests, Active Circuit Testing, Design for Testability.DSP based Analog and Mixed Signal Testing, Fault Modelling.			
	PART A (2 marks)			
Q.No	Questions	CO	BT Level	Competence
1.	Define reliability in electronic testing.	CO5	BTL 1	Remembering
2.	Define Defect, Error and fault.	CO5	BTL 1	Remembering
3.	Recall types of failures due to thermal mismatch.	CO5	BTL 1	Remembering
4.	List environmentally induced failures.	CO5	BTL 1	Remembering
5.	What are the thermo-mechanically induced failures?	CO5	BTL 1	Remembering
6.	Outline the fault modeling in testing.	CO5	BTL 1	Remembering
7.	Interpret the design for testability in electronic testing.	CO5	BTL 2	Understanding
8.	What is Fault equivalence?	CO5	BTL 2	Understanding
9.	Discuss DSP-based testing in analog and mixed-signal circuits.	CO5	BTL 2	Understanding
10.	Analyze thermal mismatch's impact on electronic component degradation during testing.	CO5	BTL 2	Understanding
11.	Discuss chemically induced failures in components.	CO5	BTL 2	Understanding
12.	Develop a plan for design for testability in a complex circuit.	CO5	BTL 2	Understanding
13.	What are the assumptions made to characterize a single stuck at fault?	CO5	BTL 1	Remembering
14.	Categorize the methods to enhance reliability in systems prone to environmental interactions.	CO5	BTL 1	Remembering
15.	Apply interconnection tests to identify potential failures.	CO5	BTL 1	Remembering
16.	What is DFT?	CO5	BTL 1	Remembering
17.	Devise a chip packaging strategy using flip-chip technology.	CO5	BTL 1	Remembering
18.	Assess advantages and limitations of system-level electrical testing.	CO5	BTL 1	Remembering

19.	Evaluate active circuit testing in ensuring reliability.	CO5	BTL 2	Understanding
20.	Compare the effectiveness of active circuit and system-level electrical testing.	CO5	BTL 2	Understanding
21.	Analyze electrically induced failures' impact on system reliability.	CO5	BTL 2	Understanding
22.	Evaluate electronic testing's role in ensuring overall system reliability.	CO5	BTL 2	Understanding
23.	Examine fault modeling's impact on testing cost-effectiveness.	CO5	BTL 2	Understanding
24.	Investigate the influence of thermal considerations on system reliability in electronic testing.	CO5	BTL 2	Understanding
	PART-B (13 marks)			
1.	Define thermo-mechanical-induced failures in electronic testing and explain in detail.	CO5	BTL 3	Applying
2.	List the categories and explain the environmental interactions typically tested in reliability evaluations.	CO5	BTL 3	Applying
3.	Identify the primary objectives of system-level electrical testing in electronic components.	CO5	BTL 3	Applying
4.	Mention the types of faults considered in fault modeling within electronic testing and explain any 4 in detail.	CO5	BTL 3	Applying
5.	Explain the impact of thermal mismatch on the reliability of electronic systems.	CO5	BTL 4	Analyzing
6.	Describe the significance of Design for Testability (DFT) in electronic testing.	CO5	BTL 4	Analyzing
7.	Elaborate on the process involved in interconnection tests in electronic devices.	CO5	BTL 4	Analyzing
8.	Understand the concept and need for active circuit testing in electronic systems.	CO5	BTL 4	Analyzing
9.	Devise a strategy to minimize chemically induced failures in electronic testing scenarios.	CO5	BTL 4	Analyzing
10.	Summarize the methods to mitigate thermal fatigue-induced failures in electronic components.	CO5	BTL 3	Applying
11.	Enumerate a test plan for system-level electrical testing in a mixed-signal VLSI circuit.	CO5	BTL 3	Applying
12.	Apply fault modeling techniques to identify potential issues in a digital memory VLSI circuit.	CO5	BTL 3	Applying
13.	Analyze the impact of electrical testing methods on the reliability of VLSI circuits.	CO5	BTL 4	Analyzing
14.	Evaluate the occurrence of single stuck at faults for a NAND based two input XOR operation?	CO5	BTL 4	Analyzing

15.	Assess the implications of thermal mismatch and fatigue on digital and mixed-signal VLSI circuits.	CO5	BTL 4	Analyzing
16.	Inspect the role of environmental stress testing in identifying electronic system vulnerabilities.	CO5	BTL 4	Analyzing
17.	Examine the implications of thermo-mechanical-induced failures on long-term reliability in electronic devices.	CO5	BTL 4	Analyzing
	PART – C (15 marks)			
1.	Explain the concept of thermal mismatch-induced failures in electronic components.	CO5	BTL 3	Applying
2.	Apply the principles of system-level electrical testing in the context of electronic reliability evaluation.	CO5	BTL 4	Analyzing
3.	Analyze the impact of chemically induced failures on electronic components during environmental stress testing.	CO5	BTL 3	Applying
4.	Analyze the significance of fault modeling in identifying potential issues within digital memory VLSI circuits.	CO5	BTL 4	Analyzing
5.	Examine the role of design for testability (DFT) in ensuring efficient electronic testing methods.	CO5	BTL 4	Analyzing