SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VI SEMESTER

1906005– VLSI Design

Regulation – 2019

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SUBJECT : 1906005 - VLSI Design

SEM / YEAR: VI / III

UNIT I - INTRODUCTION TO MOS TRANSISTOR				
MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, Non ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.				
PART - A				
Q. No	**Questions**	**CO**	**BTL**	**Competence**
1.	What are the functions of gate terminal in MOS transistor?	CO1	BTL1	Remembering
2.	Why nMOS devices conduct strong zero and weak one?	CO1	BTL1	Remembering
3.	How do you calculate gate capacitance of a MOSFET?	CO1	BTL1	Remembering
4.	Differentiate enhancement and depletion mode devices.	CO1	BTL2	Understanding
5.	Draw the 3-input NOR gate using CMOS logic with truth table.	CO1	BTL1	Understanding
6.	Draw the structure of MOS transistor.	CO1	BTL2	Understanding
7.	Sketch the transmission gate or pass gate.	CO1	BTL2	Understanding
8.	List out the set of design rules for layouts with two metal layers.	CO1	BTL1	Remembering
9.	What is stick diagram?	CO1	BTL1	Remembering
10.	Name the different operating modes of transistor and its current.	CO1	BTL1	Remembering
11.	Write the equation for describing the channel length modulation effect in nMOS transistor.	CO1	BTL2	Understanding
12.	List the Non ideal I-V effects of MOS transistor.	CO1	BTL1	Remembering
13.	Draw a CMOS inverter circuit.	CO1	BTL2	Understanding
14.	Why pMOS transistors are wider than nMOS transistors?	CO1	BTL2	Understanding
15.	Draw a RC ladder for Elmore delay with its propagation delay time, tpd.	CO1	BTL2	Understanding
16.	Define body effect and write the threshold equation including the body effect.	CO1	BTL1	Remembering
17.	Outline the features of logical effort of a gate.	CO1	BTL2	Understanding
18.	What is meant by Parasitic delay of a gate?	CO1	BTL1	Remembering
19.	Compare constant field scaling and constant voltage scaling.	CO1	BTL2	Understanding

20.	Formulate the various critical parameters of Transistor scaling.		CO1	BTL2	Understanding
21.	Define Threshold Voltage for a MOSFET		CO1	BTL2	Understanding
22.	What is body effect in MOSFETs		CO1	BTL2	Understanding
23.	What are the advantages of CMOS over NMOS		CO1	BTL1	Remembering
24.	Determine whether an NMOS transistor with a threshold voltage of 0.7V is operating in the saturation region if VGS = 2V and VDS = 3V.		CO1	BTL2	Understanding
	PART – B				
1.	Explain the operation of NMOS enhancement transistor with necessary diagram.	(13)	CO1	BTL3	Applying
2.	Explain about the modes of operation in MOS transistor with neat diagram.	(13)	CO1	BTL3	Applying
3.	Describe the equation for source to drain current in the three regions of operation of a MOS transistor.	(13)	CO1	BTL3	Applying
4.	Discuss about the Non ideal I-V effects of MOS transistors with neat diagram.	(13)	CO1	BTL4	Analyzing
5.	Explain in detail about Long-Channel I-V Charterstics of MOS transistor.	(13)	CO1	BTL4	Analyzing
6.	Summarize about stick diagram and rules with an example.	(13)	CO1	BTL4	Analyzing
7.	Describe the second order effects in MOS transistor with neat diagram.	(13)	CO1	BTL4	Analyzing
8.	Explain in detail about the DC transfer characteristics of CMOS inverter.	(13)	CO1	BTL3	Applying
9.	Write about the following MOS model with necessary equations. (i) Simple MOS capacitance model. (ii) Detailed MOS gate capacitance and diffusion capacitance model.	 (7) (6)	CO1	BTL4	Analyzing
10.	Analyze about the impact of RC Delay model and Elmore delay model in CMOS design.	(13)	CO1	BTL4	Analyzing
11.	Describe in detail about various regions of current versus input characteristics of CMOS inverter.	(13)	CO1	BTL4	Analyzing
12.	Write short notes on: (i) Transistor scaling (ii) Interconnect scaling.	(7) (6)	CO1	BTL4	Analyzing
13.	Elaborate about the CV characteristics of MOS transistor along with neat sketches.	(13)	CO1	BTL4	Analyzing

14.	Design a symbolic diagram and stick diagram for 2 input NAND gate.	(13)	CO1	BTL3	Applying
15.	Design a symbolic diagram and stick diagram for 2 input NOR gate.	(13)	CO1	BTL3	Applying
16.	Explain the operation of PMOS enhancement transistor with necessary diagram.	(13)	CO1	BTL3	Applying
17.	An NMOS transistor has a nominal threshold voltage of 0.16V. Determine the shift in threshold voltage caused by body effect using the following data. The NMOS transistor is operating at a temperature of 300ºK with the following parameters: gate oxide thickness (t_{ox}) = 0.2 * 10^{-5} cm, relative permittivity of gate oxide (ε_{ox}) = 3.9, relative permittivity of silicon (ε_{si}) = 11.7, substrate bias voltage = 2.5V, intrinsic electron concentration (N_i) = 1.5 * $10^{10}/cm^3$, impurity concentration in substrate (N_A) = 3 * 10^{16} $/cm^3$. Given Boltzmann's constant = 1.38 * 10^{-23} J/ºK, electron charge = 1.6 * 10^{-19} Columb and permittivity of free space = 8.85 * 10^{-14} F/cm.	(13)	CO1	BTL3	Applying
	PART – C				
1.	Explain in detail about Layout design rules and design for CMOS inverter with neat layout design rules.	(15)	CO1	BTL3	Applying
2.	**(i)** Consider an NMOS having electron mobility of μ_n =540 cm^2/V–Sec. Calculate the process trans conductance for the gate oxide thickness of 12 nm and 8 nm. **(ii)** An nMOS transistor has the following parameters: gate oxide thickness= 10nm, relative permittivity of gate oxide=3.9, electron mobility= 520 cm^2/V-sec, threshold voltage= 0.7 V, permittivity of free space= 8.85 x 10^{-14} F/cm and (W/L) =8. Calculate the drain current when (V_{GS} = 2V and V_{DS} =1.2 V) and also compute the gate oxide capacitance per unit area. Note that W and L refer to the width and length of the channel respectively.	(7) (8)	CO1	BTL3	Applying
3.	For a resistive load inverter circuit with V_{DD} = 5V, K_n' = 20µA/V^2, V_{to} = 0.8V, R_L = 200kΩ and W/L = 2. Calculate the critical voltages on the voltage transfer characteristics and find the noise margins of the circuit.	(15)	CO1	BTL4	Analyzing
4.	Discuss on the characteristics and working of the following with neat diagram, (i) Pass transistors (ii) Transmission gate.	(7) (8)	CO1	BTL4	Analyzing

5.	Explain the following delay models: (i) RC delay model (ii) Linear and Parasitic delay model (iii) Logical effort and delay in logic gate		CO1	BTL4	Analyzing

UNIT II – COMBINATIONAL MOS LOGIC CIRCUITS

Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. **Power:** Dynamic Power, Static Power, Low Power Architecture.

PART – A

Q. No	Questions	CO	BTL	Competence
1.	Write about static CMOS circuits.	CO2	BTL1	Remembering
2.	What is meant by bubble pushing?	CO2	BTL1	Remembering
3.	How will you calculate the logical effort in HI-skew inverter?	CO2	BTL2	Understanding
4.	Write short note about the Multiple threshold voltages for CMOS.	CO2	BTL1	Remembering
5.	What is the importance of pseudo-nMOS logic gates?	CO2	BTL2	Understanding
6.	Sketch the symmetric 2-input NOR gate with its truth table.	CO2	BTL2	Understanding
7.	Draw the schematic of Source follower Pull-up logic.	CO2	BTL2	Understanding
8.	Plot the recharge and evaluation modes of dynamic gates timing diagram.	CO2	BTL2	Understanding
9.	Draw the footed Inverter.	CO2	BTL2	Understanding
10.	Compare the static CMOS, Pseudo-nMOS inverters.	CO2	BTL2	Understanding
11.	What is the advantage of the Multiple Output Domino Logic (MODL)?	CO2	BTL1	Remembering
12.	Design a 2-input NAND gate with its truth table.	CO2	BTL2	Understanding
13.	Define Keeper circuit.	CO2	BTL1	Remembering
14.	Outline about Dual-rail Domino Logic.	CO2	BTL2	Understanding
15.	Why CMOS gates are very much power-efficient?	CO2	BTL2	Understanding
16.	How to calculate the power dissipation in CMOS circuits?	CO2	BTL1	Remembering
17.	Write the static dissipation equation in CMOS inverter.	CO2	BTL2	Understanding
18.	Mention the methods used for dynamic power reduction.	CO2	BTL1	Remembering
19.	How to calculate the average dynamic power dissipation?	CO2	BTL1	Remembering
20.	Justify that CPL is an improvement of CVSL.	CO2	BTL1	Remembering
21.	List the drawbacks of ratioed logic.	CO2	BTL2	Understanding
22.	Why single phase dynamic logic structure cannot be cascaded? Justify	CO2	BTL1	Remembering
23.	What is the influence of voltage scaling on power and delay?	CO2	BTL1	Remembering
24.	What is mean by PDP?	CO2	BTL2	Understanding

PART – B

1.	Explain in detail about static CMOS logic (or) complementary CMOS logic.	(13)	CO2	BTL4	Analyzing

2.	Illustrate the following circuits in detail. (i) Pseudo-nMOS, (ii) Ganged CMOS.	(8) (5)	CO2	BTL4	Analyzing
3.	Classify the various Ratioed circuits for CMOS circuits and explain in detail.	(13)	CO2	BTL3	Applying
4.	Assess the design of Differential Cascode Voltage Switch with Pass Gate (DCVSPG).	(13)	CO2	BTL4	Analyzing
5.	Explain in detail about the working of Cascode Voltage Switch Logic (CVSL) with neat diagram.	(13)	CO2	BTL3	Applying
6.	Discuss the structure and working of pass transistor logic with neat diagram.	(13)	CO2	BTL3	Applying
7.	Demonstrate about the structure and working of CMOS with transmission gates.	(13)	CO2	BTL3	Applying
8.	Summarize about the working of Complementary pass transistor logic (CPL) with neat diagram.	(13)	CO2	BTL4	Analyzing
9.	Explain in detail about the working of Differential pass transistor logic (DPL) with neat diagram.	(13)	CO2	BTL4	Analyzing
10.	Describe the properties and operation of dynamic CMOS logic with neat diagram.	(13)	CO2	BTL4	Analyzing
11.	Examine about the cascading of 2 dynamic gates with neat diagram.	(13)	CO2	BTL4	Analyzing
12.	Describe the basic principle of operation of Domino logic with neat diagrams.	(13)	CO2	BTL4	Analyzing
13.	Classify the types of power dissipation and derive the equation each parameter.	(13)	CO2	BTL4	Analyzing
14.	Discuss the following power dissipation techniques and its impact in CMOS inverter circuits. (i) Static dissipation, (ii) Dynamic dissipation.	(7) (6)	CO2	BTL4	Analyzing
15.	Design a CMOS compound gate(or) static gate for the Boolean expression $F = \overline{DE + A \bullet (B + C)}$	(13)	CO2	BTL3	Applying
16.	Implement the Boolean function using CMOS logic gates $Z = \overline{AB + AC + BD}$	(13)	CO2	BTL3	Applying
17.	Explain the Dual Rail Domino Logic families with necessary diagrams.	(13)	CO2	BTL4	Analyzing
	PART – C				
1.	Compare the circuit families in a tabular form.	(13)	CO2	BTL4	Analyzing
2.	(i) Draw the CMOS logic circuit for the Boolean expression $Z = \overline{(A+B)(A+C)(B+D)}$ (ii) Realize the function $F = (A+B+C)D$ using static CMOS logic.	(7) (8)	CO2	BTL3	Applying

3.	Explain the following static CMOS logic. (i) Bubble pushing. (ii) Compound gates. (iii)Skewed gates.	(5) (5) (5)	CO2	BTL4	Analyzing
4.	Explain in detail about circuit pitfalls with neat diagram.	(15)	CO2	BTL3	Applying
5.	What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS?	(15)	CO2	BTL4	Analyzing

UNIT III - SEQUENTIAL CIRCUIT DESIGN

Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. **Timing Issues:** Timing Classification of Digital System, Synchronous Design.

PART – A

Q. No	Questions	CO	BTL	Competence
1.	Define Bistability principle.	CO3	BTL1	Remembering
2.	State the approaches used to accomplish the bistable circuit.	CO3	BTL1	Remembering
3.	List the modes of operation of low voltage static latches.	CO3	BTL2	Understanding
4.	Outline the timing properties of Master-slave registers.	CO3	BTL1	Remembering
5.	Outline the working of dynamic positive edge-triggered register when Clk = 0.	CO3	BTL1	Remembering
6.	Implement a Multiplexer-based nMOS latch.	CO3	BTL2	Understanding
7.	Write the operation of C^2MOS register.	CO3	BTL2	Understanding
8.	Write about True Single-Phase Clocked Register (TSPCR).	CO3	BTL2	Understanding
9.	State the role of transistor sizing in TSPC Edge-Triggered Register.	CO3	BTL1	Remembering
10.	Mention the advantages of pipelined operation.	CO3	BTL1	Remembering
11.	What is meant by sense-amplifier based registers?	CO3	BTL2	Understanding
12.	Sketch the circuit of latch-based pipeline using C^2MOS latches.	CO3	BTL1	Remembering
13.	State the operation modes for NORA logic style.	CO3	BTL1	Remembering
14.	List out the timing parameters of the sequential circuit in synchronous design.	CO3	BTL1	Remembering
15.	Assess the properties of Schmitt trigger.	CO3	BTL2	Understanding
16.	Analyse the importance of voltage-controlled oscillator based on current-starved inverters.	CO3	BTL2	Understanding
17.	List the applications of Schmitt trigger.	CO3	BTL2	Understanding
18.	Point out the use of address transition detection (ATD) circuit.	CO3	BTL2	Understanding
19.	Enumerate the scenarios of positive and negative clock skew.	CO3	BTL2	Understanding
20.	Sketch the sense amplifiers based CMOS circuit.	CO3	BTL2	Understanding
21.	What is the difference between latches and flip flops based designs?	CO3	BTL1	Remembering
22.	What are synchronizers?	CO3	BTL2	Understanding

23.	Define max delay failure in sequential circuits.		CO3	BTL1	Remembering
24.	Define min delay failure in sequential circuits.		CO3	BTL1	Remembering
	PART-B				
1.	Explain in detail about static latches and registers.	(13)	CO3	BTL3	Applying
2.	State Bistability principle and explain in detail about the two different approaches used in this.	(13)	CO3	BTL4	Analyzing
3.	Summarize about Multiplexer-Based Latches with neat diagram.	(13)	CO3	BTL4	Analyzing
4.	Elaborate about the concept of static RS flip flops with truth table.	(13)	CO3	BTL4	Analyzing
5.	Explain in detail about dynamic latches and registers.	(13)	CO3	BTL4	Analyzing
6.	Discuss in detail about dynamic transmission gate edge triggered registers.	(13)	CO3	BTL3	Applying
7.	Explain about True Single-Phase Clocked (TSPC) latches.	(13)	CO3	BTL3	Applying
8.	Examine about the operation of TSPC positive Edge-Triggered Register (TSPCR).	(13)	CO3	BTL3	Applying
9.	Elaborate about the working of dual edge register with neat diagram.	(13)	CO3	BTL3	Applying
10.	Illustrate the following Alternative Register styles. (i) Pulse Registers. (ii) Sense-Amplifier-Based Registers.	 (7) (6)	CO3	BTL3	Applying
11.	Explain the concept of timing issues and pipelining in sequential circuits. (13)	(13)	CO3	BTL3	Applying
12.	(i) Write about Schmitt trigger and its properties. (ii) Describe Schmitt trigger and its CMOS implementation with neat diagram.	(4) (9)	CO3	BTL4	Analyzing
13.	With necessary diagram, explain the Monostable sequential circuits.	(13)	CO3	BTL4	Analyzing
14.	Evaluate the various sources of skew and jitter and explain it.	(13)	CO3	BTL3	Applying
15.	Explain the operation of Astable Circuits with a neat diagram.	(13)	CO3	BTL3	Applying
16.	Derive the equation for Max – Delay Constraints for sequential circuits.	(13)	CO3	BTL4	Analyzing
17.	Derive the equation for Min – Delay Constraints for sequential circuits.	(13)	CO3	BTL4	Analyzing
	PART-C				
1.	Draw and explain about Master-Slave Edge-Triggered register with its timing properties and Non-ideal clock signals.	(15)	CO3	BTL3	Applying
2.	Design a C^2MOS Register with CLK-$\overline{CLK}$ clocking	(15)	CO3	BTL3	Applying

	approach.				
3.	Analyse the basics of synchronous timing, clock skew, clock jitter and combined impact of skew and jitter.	(15)	CO3	BTL4	Analyzing
4.	Explain in detail about the synchronous pipelining approaches to optimize sequential circuits.	(15)	CO3	BTL4	Analyzing
5.	Write in detail about the asynchronous pipelining to optimize sequential circuit.	(15)	CO3	BTL3	Applying

UNIT IV - DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed trade-offs, Case Study: Design as a trade-off.

Designing Memory and Array structures: Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry.

PART-A

Q. No	Questions	CO	BTL	Competence
1.	Obtain the critical path delay of 4 bit ripple carry adder,	CO4	BTL2	Understanding
2.	Write about carry propagation delay and its effect in circuits.	CO4	BTL2	Understanding
3.	List out the components of Data path.	CO4	BTL1	Remembering
4.	Why is barrel Shifters very useful in the designing of arithmetic circuits?	CO4	BTL2	Understanding
5.	Deduce a partial product selection table using modified 3-bit booth's recoding multiplication.	CO4	BTL2	Understanding
6.	What is one time programmable memories?	CO4	BTL1	Remembering
7.	Draw the structure of 6- transistor SRAM cell.	CO4	BTL1	Remembering
8.	Mention the advantages and disadvantages of full adder design using static CMOS.	CO4	BTL1	Remembering
9.	Outline the concept of Dynamic voltage scaling and list its advantages.	CO4	BTL1	Remembering
10.	Define Clock gating.	CO4	BTL1	Remembering
11.	Draw the schematic for Sleep transistors used on both supply and ground.	CO4	BTL1	Remembering
12.	Identify the need for VTCMOS.	CO4	BTL2	Understanding
13.	Mention the applications of CAM.	CO4	BTL2	Understanding
14.	Assess about the inverting property of full adder.	CO4	BTL2	Understanding
15.	How to design a column multiplexer with separate decoder circuit?	CO4	BTL2	Understanding
16.	Write the full adders output in terms of propagate and generate.	CO4	BTL2	Understanding
17.	Mention the power optimization techniques for latency and throughput constrained design.	CO4	BTL1	Remembering
18.	Write the charge-share equation for DRAM.	CO4	BTL1	Remembering

19.	Design a one transistor DRAM cell.		CO4	BTL2	Understanding
20.	State the Concept of large SRAMs.		CO4	BTL2	Understanding
21.	What is meant by bit sliced data path organisation?		CO4	BTL2	Understanding
22.	Which factors determine the performance of a programmable shifter?		CO4	BTL2	Understanding
23.	Determine the propagation delay of a n – bit carry select adder		CO4	BTL2	Understanding
24.	What is ripple carry adder?		CO4	BTL1	Remembering
PART-B					
1.	Discuss the data paths in digital processor architectures.	(13)	CO4	BTL4	Analyzing
2.	(i)Explain the operation of a basic 4 bit binary adder. (ii)Describe the different approaches of improving the speed of the adder.	(10) (3)	CO4	BTL3	Applying
3.	Describe the working of ripple carry adder and derive the expression for worst case delay.	(13)	CO4	BTL3	Applying
4.	Describe the operation and working of 4-bit Brent-kung Adder.	(13)	CO4	BTL3	Applying
5.	Write short notes on Static CMOS adders.	(13)	CO4	BTL4	Analyzing
6.	Explain the operation of Carry Bypass adders with neat diagram.	(13)	CO4	BTL4	Analyzing
7.	Discuss in detail about carry select adder with neat diagram.	(13)	CO4	BTL3	Applying
8.	Write the equations governing the design of carry skip adder and explain its working.	(13)	CO4	BTL3	Applying
9.	Construct 4 X 4 array type multiplier and find its critical path delay.	(13)	CO4	BTL4	Analyzing
10.	Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier.	(13)	CO4	BTL3	Applying
11.	Illustrate the working of 4x4 carry save multiplier with neat diagram.	(13)	CO4	BTL4	Analyzing
12.	Explain the working of power and speed trade-offs with suitable case study.	(13)	CO4	BTL3	Applying
13.	Examine the working of Multi-ported SRAM and Register file CMOS logic circuit.	(13)	CO4	BTL3	Applying
14.	Explain about the DRAM sub array and open bit lines architecture.	(13)	CO4	BTL4	Analyzing
15.	What is mirror adder? List its characteristics, advantages and disadvantages.	(13)	CO4	BTL4	Analyzing
16.	Describe the Manchester carry chain adder with a neat diagram and supporting equations.	(13)	CO4	BTL4	Analyzing

17.	Describe the operation of Carry Select Adder with a block diagram.	(13)	CO4	BTL3	Applying
PART-C					
1.	Elaborate about 4 input and 4 output barrel shift adder using NMOS logic.	(15)	CO4	BTL4	Analyzing
2.	Derive the necessary expressions of a 4-bit carry look ahead adder and realize the carry out expressions using dynamic CMOS logic.	(15)	CO4	BTL3	Applying
3.	Analyse the operation of booth multiplication with suitable examples.	(15)	CO4	BTL4	Analyzing
4.	Draw and explain the architecture of large memory array with sub array memory circuitry.	(15)	CO4	BTL3	Applying
5.	Write short notes on (i) Linear carry select adder. (ii) Square root carry select adder.	(8) (7)	CO4	BTL4	Analyzing

UNIT V - IMPLEMENTATION STRATEGIES AND TESTING				
FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. ASIC design flow, Need for Testing, Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan				
PART-A				
Q. No	**Questions**	**CO**	**BT Level**	**Competence**
1.	What is meant by FPGA?	CO5	BTL 1	Remembering
2.	Point out the common techniques of adhoc testing.	CO5	BTL 1	Remembering
3.	List out the different approaches of Design for testability.	CO5	BTL 1	Remembering
4.	Analyze the relationship between full customs and semi-customs ASIC's with an example.	CO5	BTL 2	Understanding
5.	Mention the types of stuck-at faults.	CO5	BTL 2	Understanding
6.	Write a note on short circuit and open circuit faults.	CO5	BTL 2	Understanding
7.	State the features of boundary scan method.	CO5	BTL 1	Remembering
8.	Differentiate between observability and controllability.	CO5	BTL 2	Understanding
9.	Write about ATPG design scan.	CO5	BTL 1	Remembering
10.	Define Fuse based FPGA.	CO5	BTL 1	Remembering
11.	Define Antifuse.	CO5	BTL 1	Remembering
12.	Identify different types of ASIC Design Methodology.	CO5	BTL 2	Understanding
13.	Draw the block diagram of test data register.	CO5	BTL 2	Understanding
14.	List the advantages and disadvantages of ASIC.	CO5	BTL 2	Understanding
15.	Summarize the functions of Programmable Interconnect points in FPGA.	CO5	BTL 2	Understanding
16.	Summarize the advantages and disadvantages of FPGA compared to ASIC.	CO5	BTL 2	Understanding
17.	Distinguish between standard cell-based ASICs and full custom ASIC.	CO5	BTL 1	Remembering

18.	Examine the Test Access Port connection details.		CO5	BTL 1	Remembering
19.	Outline the steps for CMOS circuit IDDQ test.		CO5	BTL 2	Understanding
20.	Write about various ways of routing procedure.		CO5	BTL 1	Remembering
21.	What is the impact of Moore's Law on the Semiconductor Industry?		CO5	BTL 1	Remembering
22.	State the features of full custom design		CO5	BTL 1	Remembering
23.	What is DFT?		CO5	BTL 2	Understanding
24.	What are the types of faults detected by IDDQ testing.		CO5	BTL 1	Remembering
PART-B					
1.	Define an ASIC? Explain different types of ASIC's.	(13)	CO5	BTL3	Applying
2.	Describe the various types of adhoc testing techniques with neat diagram.	(13)	CO5	BTL4	Analyzing
3.	Explain the ASIC design flow with a neat diagram	(13)	CO5	BTL3	Applying
4.	Illustrate the concepts of short circuit and open circuit fault.	(13)	CO5	BTL3	Applying
5.	Explain the architecture of parallel scan testing method.	(13)	CO5	BTL4	Analyzing
6.	Examine the boundary scan architectures and explain how to test the circuit board level and system level.	(13)	CO5	BTL4	Analyzing
7.	Describe briefly about the BIST block structure along its components.	(13)	CO5	BTL4	Analyzing
8.	Discuss the types of FPGA routing techniques.	(13)	CO5	BTL3	Applying
9.	Write the goals and objectives of following terms a) Floor planning b) Placement c) Routing	(13)	CO5	BTL4	Analyzing
10.	Examine Antifuse, SRAM, EPROM and EEPROM technologies with respect to erasing mechanism.	(13)	CO5	BTL4	Analyzing
11.	Draw and explain the building blocks of FPGA.	(13)	CO5	BTL3	Applying
12.	Draw the block diagram of BILBO\BIST and explain each unit operation.	(13)	CO5	BTL3	Applying
13.	Evaluate the steps involved in design for manufacturability to increase the yield of optimized circuit.	(13)	CO5	BTL3	Applying
14.	Write short notes on TAP controller of Boundary Scan Technique.	(13)	CO5	BTL3	Applying
15.	Illustrate the basic types of programmable elements of FPGA.	(13)	CO5	BTL3	Applying
16.	Write short notes on the following terms a) Design Rule Checks (DRC) b) Electrical Rules Checks (ERC) c) Layout versus Schematic (LVS)	(13)	CO5	BTL3	Applying
17.	Describe an instruction register of Boundary Scan.	(13)	CO5	BTL4	Analyzing
PART-C					
1.	Explain the ASIC design flow with a neat diagram and	(15)	CO5	BTL3	Applying

	write the difference between custom IC and standard IC				
2.	Draw and explain the building blocks of FPGA with different fusing technologies.	(15)	CO5	BTL4	Analyzing
3.	(i) Explain about building block architecture of TAP. (ii) Write short notes on routing procedures involved in FPGA interconnect.	(10) (5)	CO5	BTL4	Analyzing
4.	Discuss in detail about different types of scan design method and explain with neat diagram.	(15)	CO5	BTL3	Applying
5.	Describe about the Boundary Scan in detail with supporting diagrams.	(15)	CO5	BTL4	Analyzing