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SRM VALLIAMMAI ENGINEERING COLLEGE

SRM NAGAR, KATTANKULATHUR – 603203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LAB MANUAL

EC3466- LINEAR IC AND PCB DESIGN LABORATORY

IV SEMESTER ECE

(REGULATION 2023)

Academic Year: 2024-2025 (Even Semester)

Prepared by,

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EC3466	LINEAR IC AND PCB DESIGN LABORATORY	L	T	P	C
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LIST OF EXPERIMENTS:

OP-AMP BASED EXPERIMENTS: DESIGN AND TESTING OF

1. Inverting, Non-inverting Amplifier using Op-Amp.
2. Integrator and Differentiator using Op-Amp.
3. Instrumentation amplifier using Op-Amp.
4. Active low-pass and High-pass Filters using Op-Amp.
5. Bistable multivibrators and Schmitt Trigger using Op-Amp.
6. Astable and monostable multivibrators using NE555 Timer.
7. PLL characteristics

PCB DESIGN EXPERIMENTS USING OrCAD TOOL

8. Introduction to PCB Design, Fabrication & Assembly Process and Transmission lines, crosstalk, and its effects using OrCAD.
9. Using OrCAD tool, Practice the Basic RC Circuit with following PCB Design steps.
    - Schematic Design: Familiarization of the Schematic Editor, Schematic creation, Annotation, Netlist generation
    - Layout Design: Familiarization of Footprint Editor, Mapping of components, Creation of PCB layout Schematic
    - Create new schematic components

      Create new component footprints.
10. Design and fabricate a PCB for Regulated power supply with filter and regulation sections.

TOTAL: 45 Periods

LAB REQUIREMENT FOR A BATCH OF 30 STUDENTS:

S.NO	EQUIPMENTS	QUANTITY
1.	70MHz DSO with built in 4-bit pattern generator and 50 MHz AFG	15 Nos
2.	Programmable Triple o/p Power Supplies (0 –30V/ 3A) (0-30V/3A) (0-5V/3A)	15 Nos
3.	Digital Multimeter	15 Nos
4.	Digital LCR Meter	2 Nos
5.	Standalone desktops PC	15 Nos
6.	Transistor/MOSFET (BJT-NPN-PNP and NMOS/PMOS)	50 Nos
7.	IC Tester	5 Nos
8.	Copper cladded base board	15 Nos
9.	Hand Drilling machine	15 Nos
10.	Soldering guns	15 Nos
11.	Assorted electronic components for making circuits	50 Nos
12.	OrCAD/ allegro/Altium or equivalent software	15 Users
13.	Copper solvent	as required

EC3466 LINEAR IC AND PCB DESIGN LABORATORY

Cycle – 1

1 Inverting, Non-inverting Amplifier using Op-Amp.

2 Integrator and Differentiator using Op-Amp.

3 Instrumentation amplifier using Op-Amp.

4 Active low-pass and High-pass Filters using Op-Amp.

5 Bistable multivibrators and Schmitt Trigger using Op-Amp.

Cycle – 2

6 Astable and monostable multivibrators using NE555 Timer.

7 PLL characteristics

8 Introduction to PCB Design, Fabrication & Assembly Process and Transmission lines, crosstalk, and its effects using OrCAD.

9 Using OrCAD tool, Practice the Basic RC Circuit with following PCB Design steps.

Schematic Design: Familiarization of the Schematic Editor, Schematic creation, Annotation, Netlist generation

Layout Design: Familiarization of Footprint Editor, Mapping of components, Creation of PCB layout Schematic

Create new schematic components Create new

component footprints.

10 Design and fabricate a PCB for Regulated power supply with filter and regulation sections.

ADDITIONAL EXPERIMENTS:

11 Phase shift and Wien bridge oscillators using op-amp.

12 Design a voltage divider circuit with SPICE simulator.

Exp 1. INVERTING AND NON-INVERTING AMPLIFIERS USING OP-AMP.

1(a) INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the inverting input terminal through R_1 and the non- inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

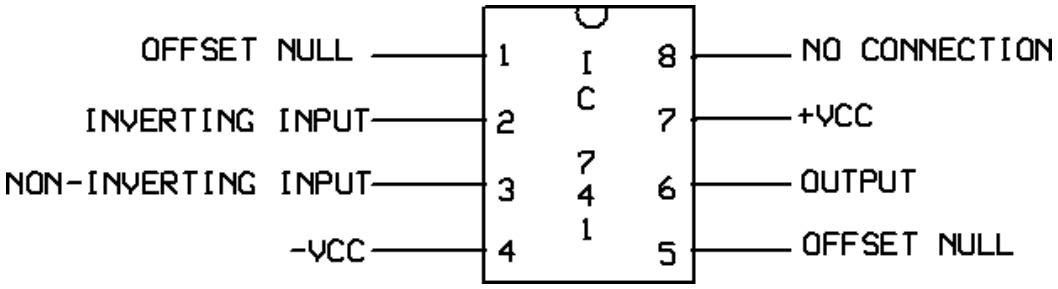
$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

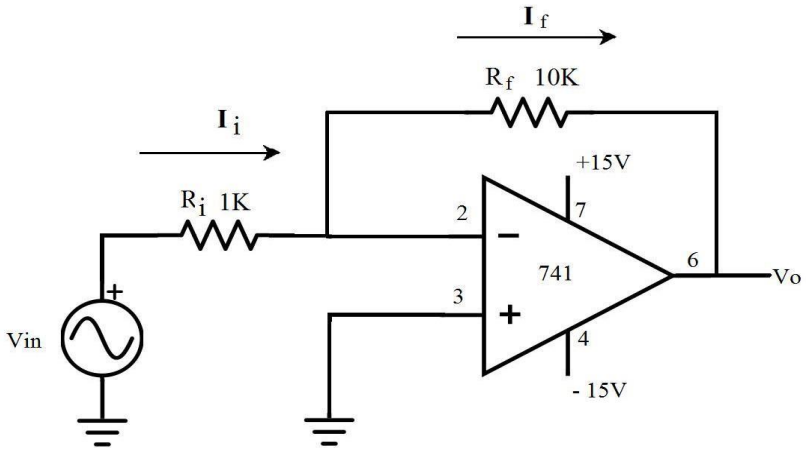
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{CC}$ and $- V_{CC}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



DESIGN:

Gain of an inverting amplifier $Av = V_o/V_{in} = - R_f / R_i$

The required gain = 10, That is

$Av = -(Rf/ Ri = 10$

Let $Ri = 1K\Omega$, Then $Rf = 10K\Omega$

Observations:

Vin = 1 Vpp

Vo=?

Gain, Av = Vo/Vin =?

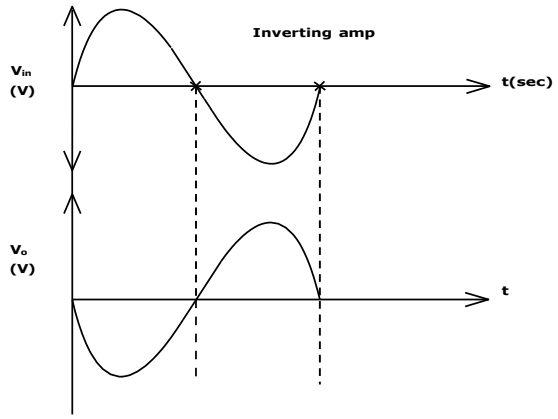
Observed phase difference between the input and the output on the CRO =?

Calculation:

OBSERVATIONS:

S.No	Parameters	Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

MODEL GRAPH:



VIVA QUESTIONS:

1. What is an op-amp?
2. What is an inverting amplifier?
3. What is the difference between inverting and non-inverting amplifier?
4. Define CMRR.
5. Write the equation for gain of an inverting amplifier.

RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn**.**

1(b) NON - INVERTING AMPLIFIER

AIM:

To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

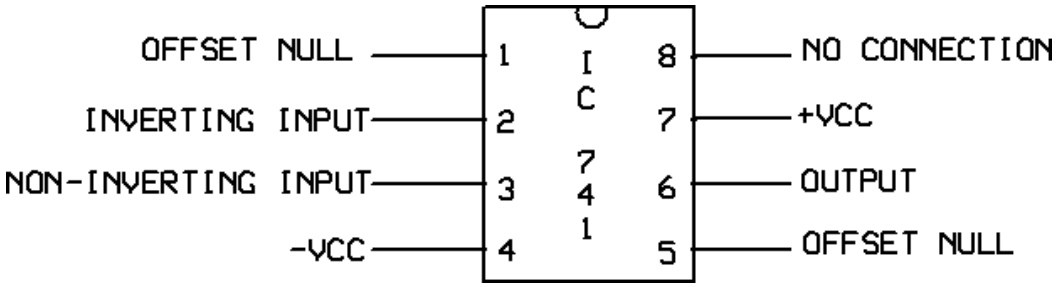
$$V_o = A_{CL}\ V_i$$

Here the output voltage is in phase with the input signal.

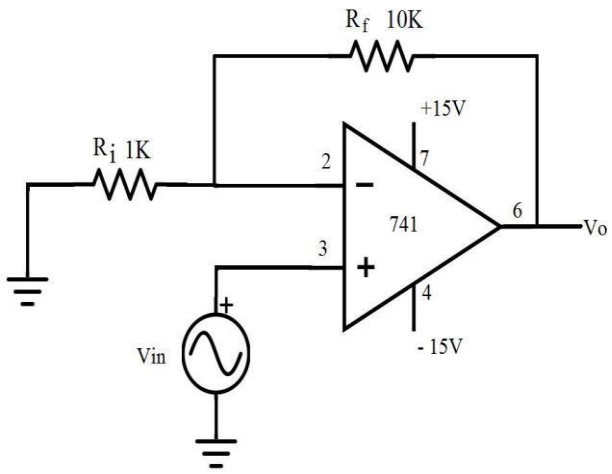
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{CC}$ and $- V_{CC}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



DESIGN:

Gain of an inverting amplifier $Av=V_o/V_{in} = 1+(R_f/ R_i)$,

Let the required gain be 11,

Therefore $Av= 1+R_f/ R_i= 11$

$R_f/ R_i = 10$

Take $R_i= 1K\Omega$, Then $R_f = 10K\Omega$

Vin = 1Vpp

Vo = ?

Gain Av = Vo/Vin =?

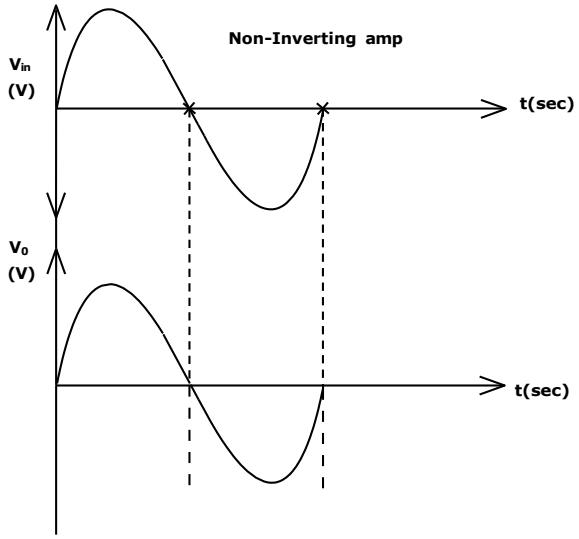
Observed phase difference between the input and the output on the CRO =?

CALCULATION:

OBSERVATIONS:

S.No	Parameters	Input	Output
1.	Amplitude (No. of div x Volts per div)		
2.	Time period (No. of div x Time per div)		

MODEL GRAPH:



VIVA QUESTIONS:

1. What is an op-amp?
2. What is an non- inverting amplifier?
3. What is the difference between inverting and non-inverting amplifier?
4. Define CMRR.
5. Write the equation for gain of a non- inverting amplifier.

RESULT:

The design and testing of the non-inverting amplifier are done and the input and output waveforms were drawn.

Exp 2. INTEGRATOR AND DIFFERENTIATOR AMPLIFIERS USING OP-AMP.

2(a) INTEGRATOR

AIM:

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

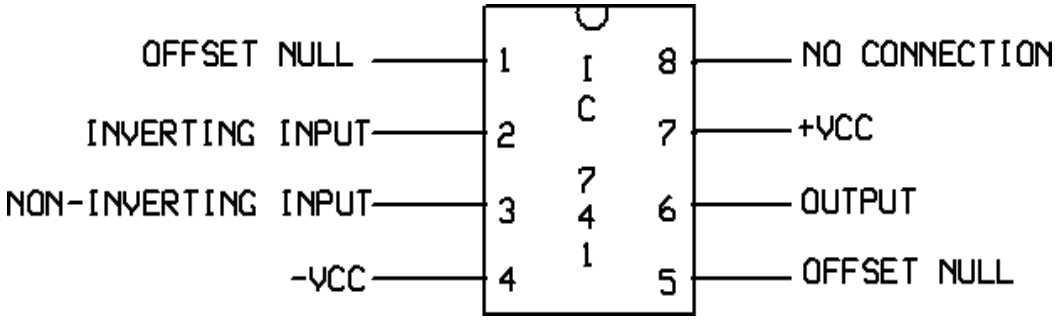
A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as,

$$V_o = - (1/R_f C_1) \int V_i \, dt$$

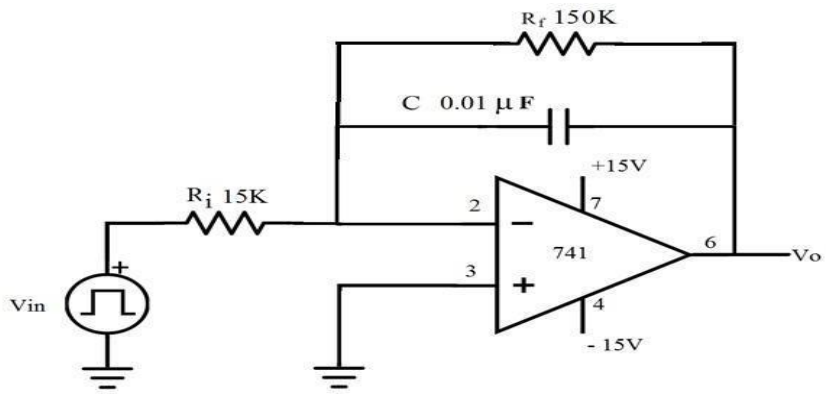
Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is, $T \geq R_f C_f$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



DESIGN:

Given f =1 KHz So T = 1/f = 1ms

Design equation is $T = 2\pi R_i C$

Let $C = 0.01\mu F$

Then $R_i = 15K\Omega$

Take $R_f = 10R_i = 150K\Omega$

[To obtain the output of an Integrator circuit with component values $R_1C_f = 0.1ms$, $R_f = 10\ R_1$ and $C_f = 0.01\ \mu F$ and also if 1 V peak square wave at 1000Hz is applied as input.]

We know the frequency at which the gain is 0 dB, fb = 1 / (2π R1 Cf) Therefore fb =

Since fb = 10 fa, and also the gain limiting frequency fa = 1 / (2π Rf Cf) We get, R1 = and hence Rf =

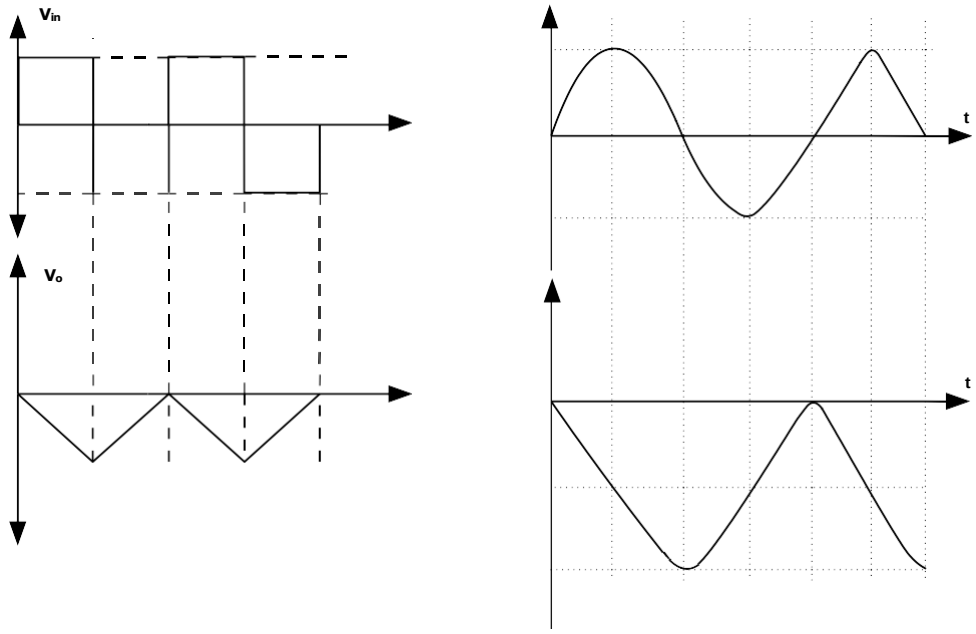
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No	Parameters	Amplitude	Time period
1.	Sine wave input Cosine wave output		
2.	Square wave input Spike wave output		

MODEL GRAPH:



CALCULATION:

RESULT:

The design of the Integrator circuit was done and the input and output waveforms were obtained**.**

2(b) DIFFERENTIATOR

AIM:

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 - 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

THEORY:

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. The expression for the output voltage is given as,

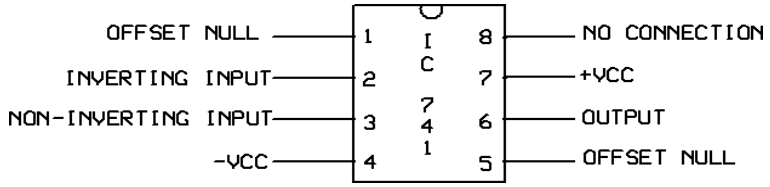
$$V_o = - R_f C_1 (dV i /dt)$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op- amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

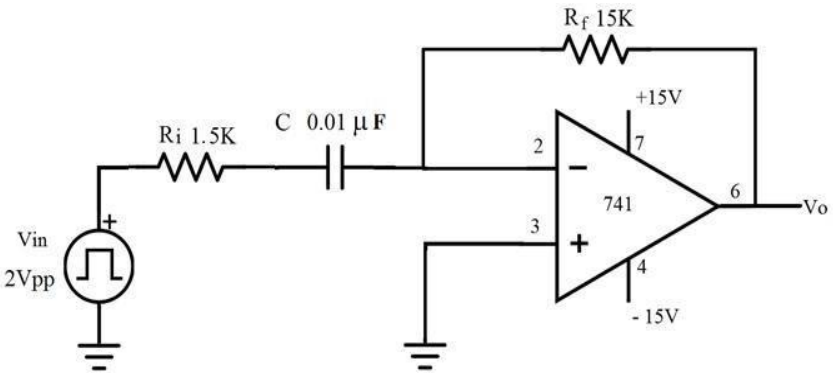
1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ μF, calculate the value of R_f.
2. Choose $f_b = 20 f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f C_f$.

The differentiator is most commonly used in wave shaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF DIFFERENTIATOR:



DESIGN:

Given f = 1 KHz So T = 1/f = 1ms

Design equation is $T = 2\pi R_f C$

Let C = 0.01µF

Then R_f = 15KΩ

Let Ri = Rf/10 = 1.5KΩ

[To design a differentiator circuit to differentiate an input signal that varies in frequency from 10 Hz to about 1 KHz. If a sine wave of 1 V peak at 1000Hz is applied to the differentiator, draw its output waveform.]

Given, f_a = 1 KHz

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$ Let us assume C_1 = 0.1 µF; then R_f = _____

Since $f_b = 20 f_a$, f_b = 20 KHz

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$ Hence R_1 = ___

Also, since $R_1C_1 = R_f C_f$; Cf = _____

Given V_p = 1 V and f = 1000 Hz, the input voltage is $V_i = V_p \sin \omega t$ We know $\omega = 2\pi f$

Hence,

$Vo = - R_f C_1 (dVi/dt)$

$= - 0.94 \cos \omega t$

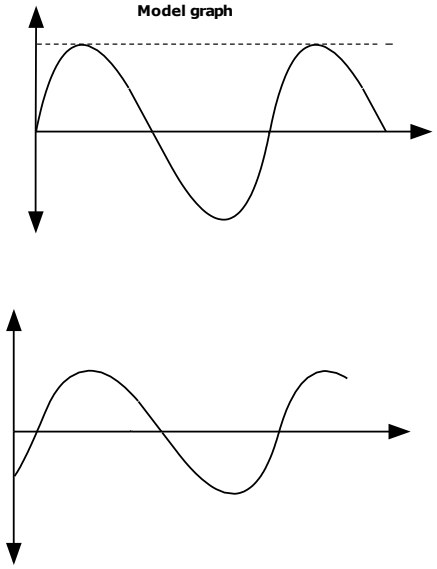
PROCEDURE:

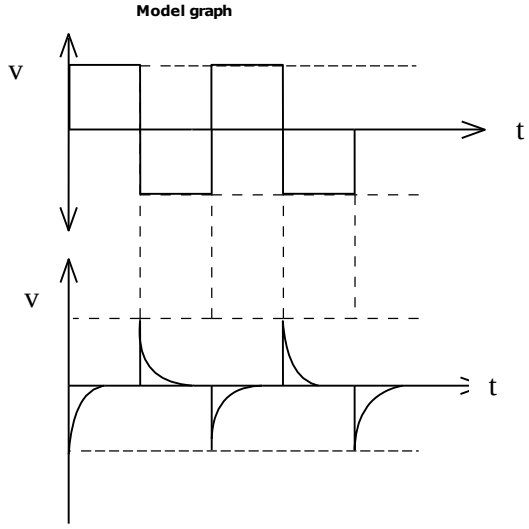
1. Connections are given as per the circuit diagram.
2. + V_{CC} and - V_{CC} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

OBSERVATIONS:

S.No	Parameters	Amplitude	Time period
1.	Sine wave input Cosine wave output		
2.	Square wave input Spike wave output		

MODEL GRAPH:





CALCULATION:

VIVA QUESTIONS.

1. Define an integrator.
2. State the applications of an integrator.
3. What is a differentiator?
4. What are the steps to design a differentiator?
5. What are the steps to design an integrator?

RESULT:

The design of the Differentiator circuit was done and the input and output waveforms were obtained.

Exp 3. INSTRUMENTATION AMPLIFIER USING OP-AMP.

AIM:

To design a instrumentation Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

THEORY:

An **instrumentation** (or **instrumentational**) **amplifier** is a type of differential amplifier that has been outfitted with input buffers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment.
Additional characteristics include very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. Instrumentation amplifiers are used where great accuracy and stability of the circuit both short- and long-term are required.

The most commonly used instrumentation amplifier circuit is shown in the figure. The gain of the circuit is

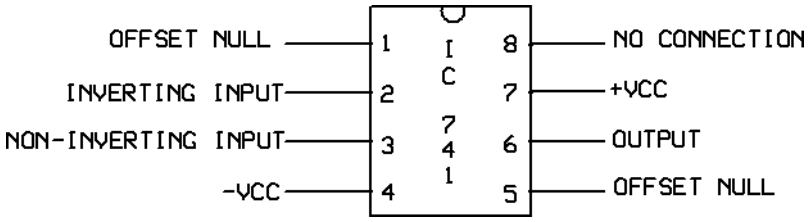
$$\frac{V_{\text{out}}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{\text{gain}}}\right)\frac{R_3}{R_2}$$

The rightmost amplifier, along with the resistors labelled R_2 and R_3 is just the standard differential amplifier circuit, with gain = R_3 / R_2 and differential input resistance = $2 \cdot R_2$. The two amplifiers on the left are the buffers. With R_{gain} removed (open circuited), they are simple unity gain buffers; the circuit will work in that state, with gain simply equal to R_3 / R_2 and high input impedance because of the buffers. The buffer gain could be increased by putting resistors between the buffer inverting inputs and ground to shunt away some of the negative feedback; however, the single resistor R_{gain} between the two inverting inputs is a much more elegant method: it increases the differential-mode gain of the buffer pair while leaving the common-mode gain equal to 1.

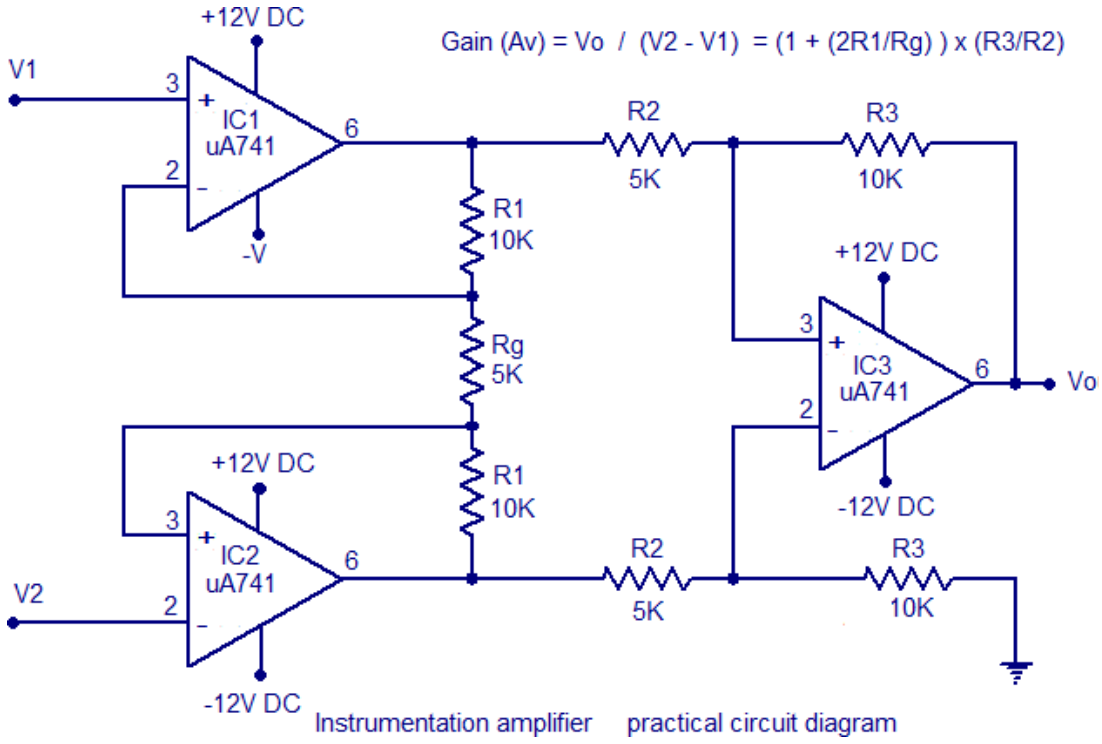
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + Vcc and - Vcc supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INSTRUMENTATION AMPLIFIER:



OBSERVATIONS:

S.No	Parameters	Amplitude	Time period
1.	Input		
2	Output		

VIVA QUESTIONS:

1. What are the features of instrumentation amplifier?
2. What are the applications of instrumentation amplifier?
3. What is an instrumentation amplifier?
4. Write the expression for output voltage.
5. What is the use of transducer in an instrumentation amplifier?

RESULT:

The design and testing of the instrumentation amplifier are done and the input and output waveforms were drawn.

Exp 4. ACTIVE LOWPASS, HIGHPASS AND BANDPASS FILTERS USING OP-AMP

Aim:

To design and test the frequency response of a second order LPF, HPF and BPF.

Components Required:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Resistors		
3.	Capacitor	O.01□f, O.05□f	2 each
4.	CRO		1
5.	Power Supply	± 15V	1
6.	Probe		2
7.	Bread Board		1

Theory:

LPF:

A LPF allows only low frequency signals up to a certain break-point f_H to pass through, while suppressing high frequency components. The range of frequency from 0 to higher cut off frequency f_H is called pass band and the range of frequencies beyond f_H is called stop band.

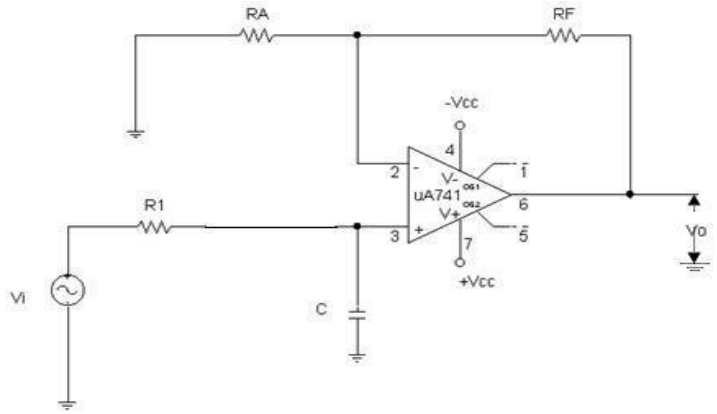
The following steps are used for the design of active LPF.

1. The value of high cut off frequency f_H is chosen.
2. The value of capacitor C is selected such that its value is ≤1μF.
3. By knowing the values of f_H and C, the value of R can be calculated using

$$f_H = \frac{1}{2\pi RC}$$

4. Finally, the values of R_1 and R_f are selected depending on the designed pass band gain by using, $A = 1 + \left(\frac{R_f}{R_1}\right)$

Circuit Diagram:



Design:

Second order:

Given frequency, f_H = 2 KHz and gain =2

Let C=0.01μf

The frequency, $f_H = {}^{1}\Big/_{2\pi\sqrt{(2\times10^{3})(0.01\times10^{-6})}}$

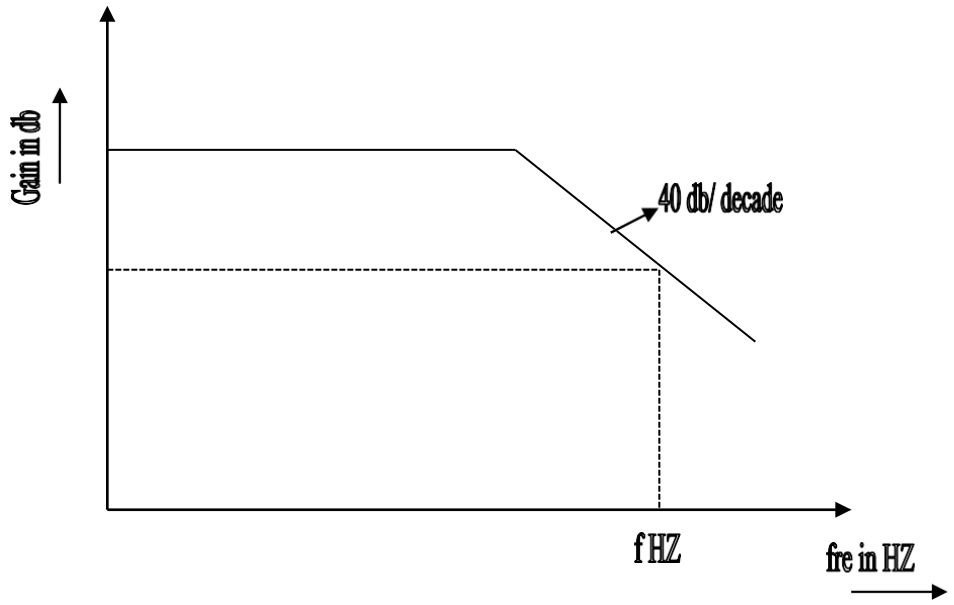
Set, $R_2 = R_3 = R$ and $C_2 = C_3 = C$ and $f_H = \frac{1}{2\pi RC}$

Tabulation:

First order LPF **Vin=1V**

S.No	Frequency (Hz)	O/p voltage(v)	Gain=Vo/Vin	Gain=20log (Vo/Vin)

Model graph:

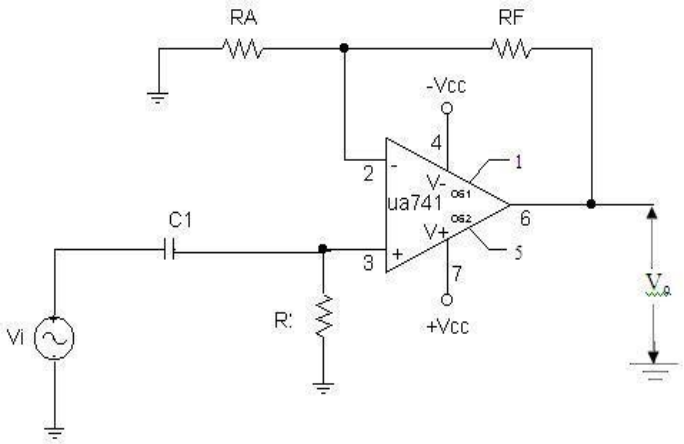


High Pass Filter:

Theory:

The high pass filter is the complement of the low pass filter. Thus, the high pass filter can be obtained by interchanging R and C in the circuit of low pass configuration. A high pass filter allows only frequencies above a certain bread point to pass through and at terminates the low frequency components. The range of frequencies beyond its lower cut off frequency f_L is called stop band.

Circuit Diagram:



Design:

$f_L = 2\ KHz, C = 0.01\mu F, \qquad Gain, A_v = 2$

$$f_L = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$$

Set, $R_2 = R_3 = R$

$C_2 = C_3 = C$

$$R_2 = R_3 = \frac{1}{2\pi fLC} = 7.95\ k\Omega$$

$$A = 1 + \left(\frac{R_f}{R_1}\right) = 2$$

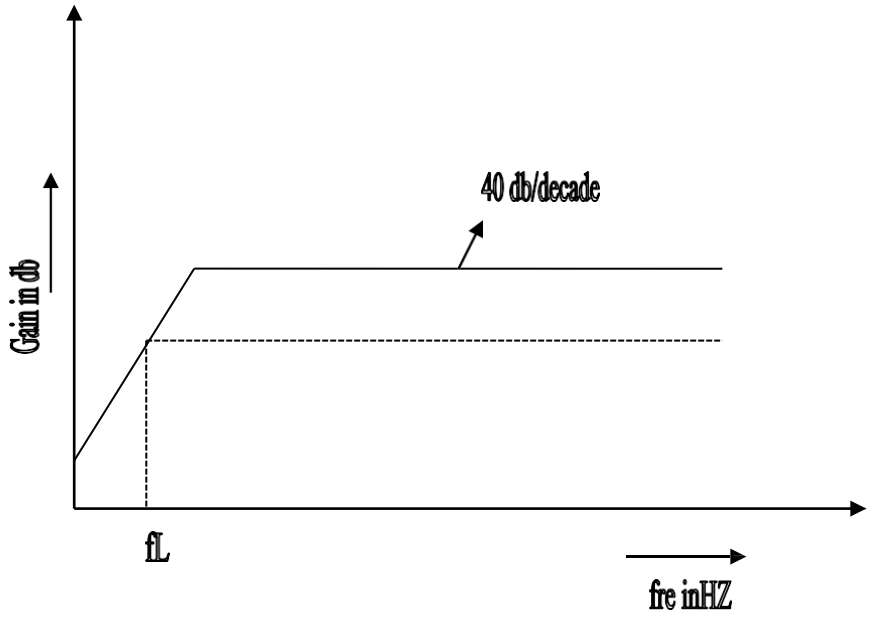
$R_f = R_1 = 10\ k\Omega$ (given)

Observation:

Vin=1V

S.No	Frequency (Hz)	O/p voltage(v)	Gain=Vo/Vin	Gain=20log(Vo/Vin)

Model graph:



Procedure:

LPF:

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the filter channels 1 and 2 of the CRO are connected.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. The correct polarity is checked.
6. The above steps are repeated for second order filter.

HPF:

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the filter channels 1 and 2 of the CRO are connected.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. The correct polarity is checked.
6. The above steps are repeated for second order filter.

Theory:

BPF:

The BPF is the combination of high and low pass filters and this allows a specified range of frequencies to pass through. It has two stop bands in range of frequencies between 0 to f_L and beyond f_H. The band b/w f_L and f_H is called pass band. Hence its bandwidth is (f_L-f_H). This filter has a maximum gain at the resonant frequency (f_r) which is defined as,

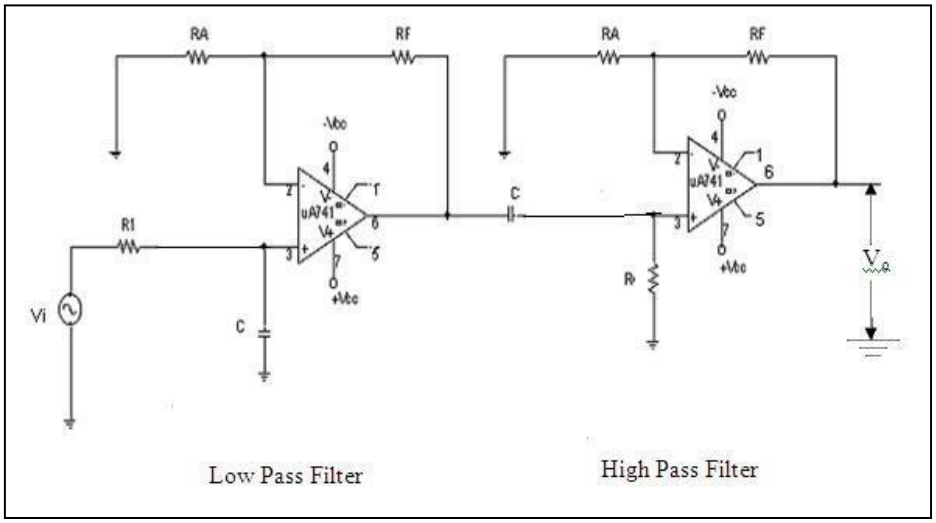
$$f_r = \sqrt{f_H f_L}$$

The figure of merit (or) quality factor Q is given by,

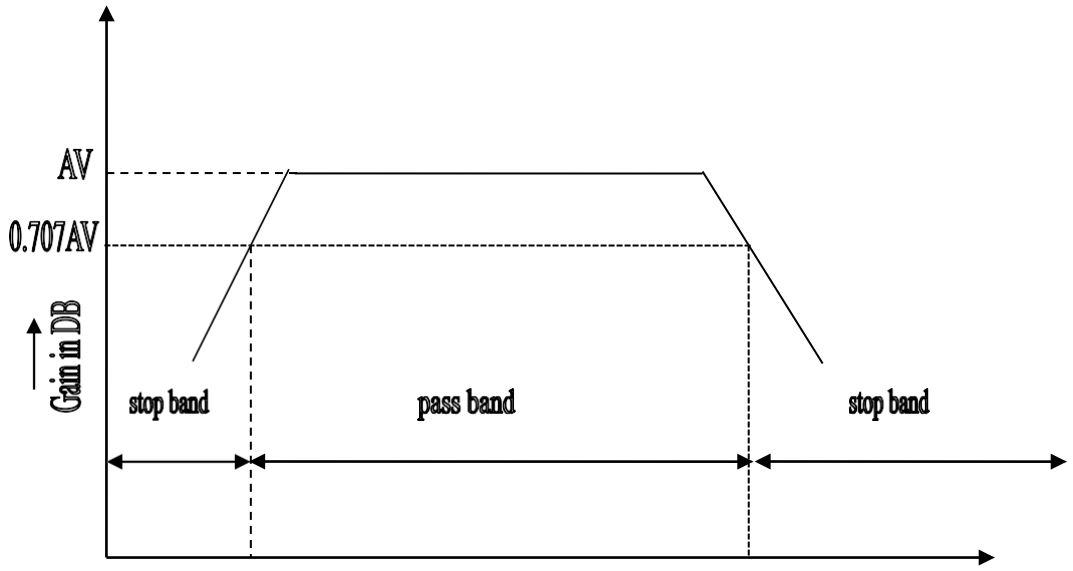
Circuit Diagram and Model graph: BPF

$$Q = \frac{f_r}{f_H - f_L} = \frac{f_r}{BW}$$

Circuit Diagram:



MODEL GRAPH:



TABULATION:

S.No	Frequency (Hz)	Vo(volts)	Gain=20log (Vo/Vin)

Procedure:

BPF:

1. The input signal is connected to the circuit from the signal generator.
2. The input and output signals are connected to the filter.
3. The suitable voltage is selected.
4. The correct polarity is checked.
5. The steps are repeated.

Result:

Thus, the frequency response of second order LPF, HPF and BSF filter was designed and tested.

Exp 5. BISTABLE MULTIVIBRATOR SCHMITT TRIGGER USING OP-AMP.

5(a): BISTABLE MULTIVIBRATOR

AIM: To verify the stable states of Bistable Multivibrator and observe the base & Collector waveforms.

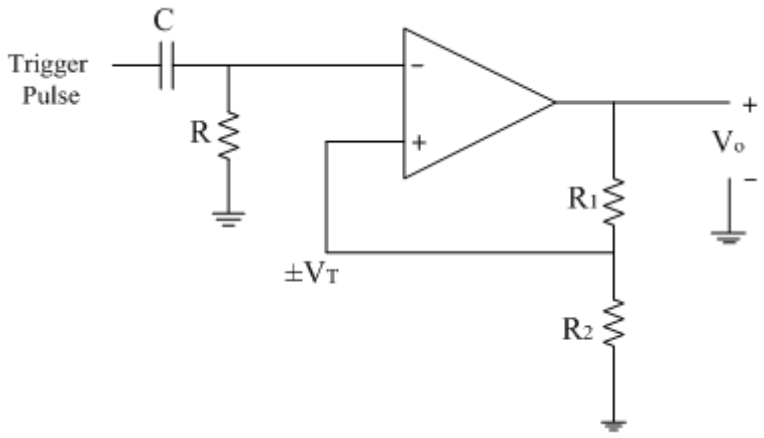
APPARATUS:

S.No	Items	Range	Quantity
1	Dual Regulated D.C Power supply	0–30 Volts	1
2	Diode	BY127	3
3	Resistors	15KΩ, 2.2 KΩ, 560Ω	Each 2
4	Capacitors	0.01μf	1
5	Capacitors	10pf	2
6	Transistors	2N2222	2
7	Signal Generator	-	1
8	CRO	-	1
9	Bread Board & Connecting wires	-	1 Set

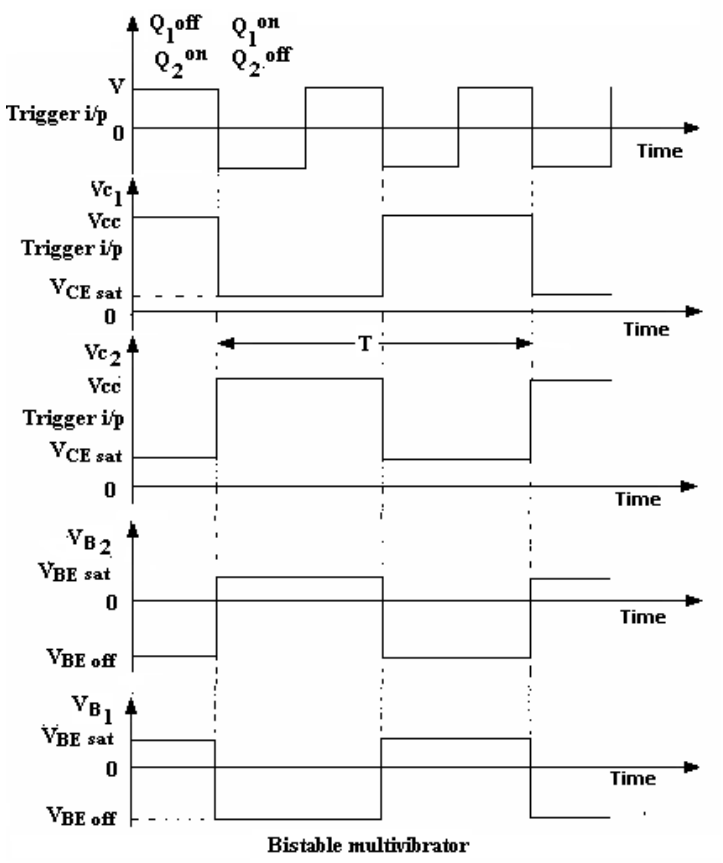
PROCEDURE:

1. Connections are made as shown in Fig.
2. Switch on the D.C power supply and set the voltages to +6 V & -6V.
3. In the absence of steering diodes & Commutating capacitors, Verify the stable state of Multivibrator
4. After getting the stable state, connect the steering diodes and commutating capacitors
5. Apply trigger input of 5V p-p square wave at 1KHz from the function Generator.
6. Observe the waveforms at the collector and base of both the transistors.
7. Plot the waveforms on graph sheet to the scale.

CIRCUIT DIAGRAM:



WAVEFORMS:



Bistable multivibrator

VIVA QUESTIONS:

1. Describe the principle of fixed-bias Binary?
2. What is a stable state?
3. What is the role of commutating capacitors in the Binary?
4. Explain the working of steering diode arrangement in the binary?
5. What are the different types of triggering?
6. What is the difference between symmetrical triggering and asymmetrical triggering?
7. What are the applications of Bistable Multivibrator?

RESULT:

Stable states of Bistable Multivibrator are verified and waveforms at the base & collector of the transistors are observed.

5(b): SCHMITT TRIGGER

AIM: To study the operation of Schmitt Trigger circuit and calculate it's lower & upper triggering points.

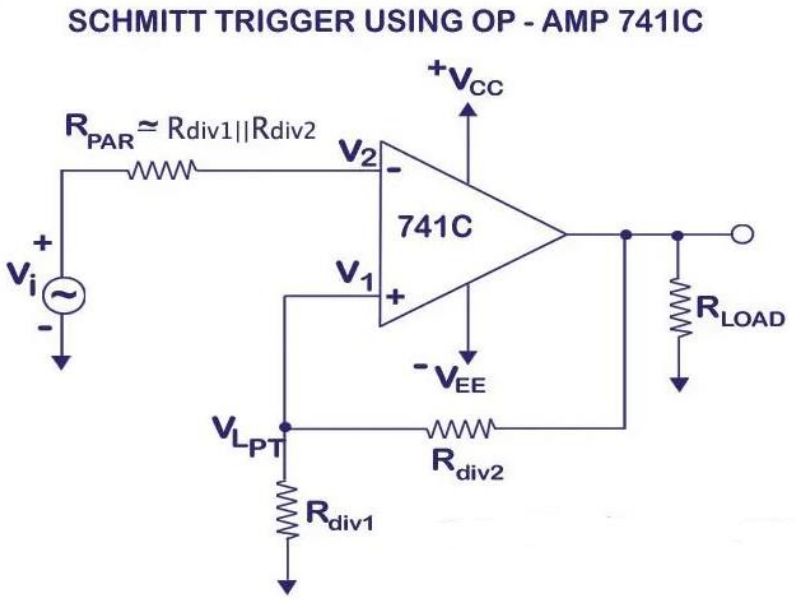
APPARATUS:

S.No	Items	Range	Quantity
1	Regulated D.C Power supply	(0–30) Volts	1
2	Resistors	2KΩ	2
3	Resistors	1KΩ, 5.6KΩ, 4KΩ, 4.7KΩ	Each 1
4	Transistors	SL100	2
5	Signal Generator	-	1
6	CRO	-	1
7	Bread Board & Connecting wires	-	1 Set

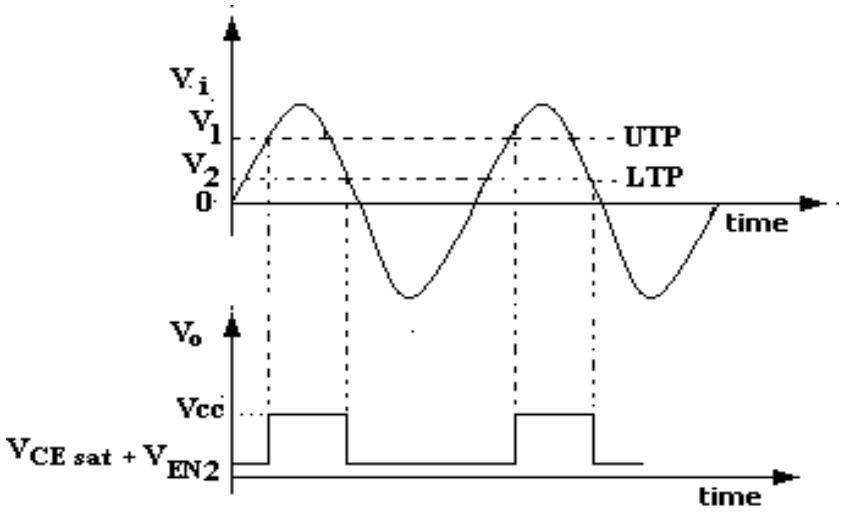
PROCEDURE:

1. Connections are made as shown in Fig.
2. Switch on the D.C power supply and set the voltage to +12 V.
3. Apply 12V p-p Sine wave at 1K Hz from the function Generator.
4. Observe the o/p square waveform on CRO.
5. Identify the amplitude of the I/p when the o/p rises suddenly, which is called UTP
6. Identify the amplitude of the I/p when the o/p falls suddenly, which is called LTP
7. Compare the identified UTP & LTP's with the theoretical values.
8. Plot the waveforms on graph sheet to the scale.

CIRCUIT DIAGRAM:



WAVEFORMS:



Schmitt Trigger

CALCULATIONS:

UTP ---- Upper triggering potential, LTP------ Lower triggering potential
UTP is defined as the I/P voltage at which transistor 'Q_1' begins to conduct LTP is defined as the I/P voltage at which transistor 'Q_2' resumes conduction. Let UTP = V_1 & LTP = V_2
From the ckt, Initially 'Q1' is OFF & 'Q_2' is

ON UTP = $V_1 = V_{BE1} + V_{EN2}$

W

here

$V_{EN2} = [(V_{CC} - V_{CEsat})\ Re] / (R_{C2} + Re)$, V_{BE1} is V_{Beoff}

When the I/P crosses UTP point, 'Q1' is ON & 'Q_2'

is OFF LTP = $V_2 = V_{BE1} + V_{EN1}$ Where

$V_{EN1} = [(V_{CC} - V_{CEsat})\ Re] / (R_{C1} + Re)$, V_{BE1} is V_{BEsat} Find the UTP & LTP of the ckt using above expressions.

VIVA QUESTIONS:

1. Define UTP & LTP?
2. What is the other name of a Schmitt Trigger circuit?
3. Explain the working of Schmitt Trigger circuit?
4. Explain Hysteresis with Schmitt Trigger?
5. What are the applications of Schmitt Trigger?

RESULT:

Square wave o/p of a Schmitt Trigger circuit is observed for a Sinusoidal input. UTP & LTP's are compared with the theoretical values.

EXP 6. ASTABLE AND MONOSTABLE MULTIVIBRATORS USING NE555 TIMER

6(a). ASTABLE MULTIVIBRATOR

Aim:

To design and test an Astable and Monostable Multivibrators using 555 timer with duty cycles ratio.

Apparatus Required:

S.No	Component	Range	Quantity
1.	555 TIMER		1
2.	Resistors	3.3K, 6.8k	1
3.	Capacitors	0.1 µ F, 0.01µ F	2
4.	Diode	In4001	1
5.	CRO		1
6.	Power supply	± 15 V	1
7.	Probe		2
8.	Bread Board		1

Astable Multivibrators using 555

Fig shows the 555-timer connected as an Astable Multivibrators. Initially, when the output is high. Capacitor C starts charging towards V_{cc} through R_A and R_B. As soon as capacitor voltage equals 2/3 VCC upper comparator (UC) triggers the flip flop and the output switches low. Now capacitor C starts discharging through R_B and transistor Q_1.

When the voltage across C equals 1/3 VCC lower comparator (LC), output triggers the flip- flop and the output goes high. Then the cycle repeats.

The capacitor is periodically charged and discharged between 2/3 VCC and 1/3 VCC respectively. The time during which the capacitor charges form 1/3 VCC to 2/3 VCC is equal to the time the output is high and is given by

$$T_c = 0.69(R_A+R_B)\,C \qquad (1)$$

Where R_A and R_B are in Ohms and C is in farads. Similarly, the time during which the capacitor discharges from 2/3 VCC to 1/3 VCC is equal to the time the output is low and is given by

$$T_d = 0.69\ R_B\ C \qquad (2)$$

The total period of the output waveform is

$$\mathbf{T = T_c + T_d = 0.69 (R_A + 2R_B) C} \qquad (3)$$

The frequency of oscillation

$$f_o = 1 / T = 1.45 / (R_A + 2R_B)C \qquad (4)$$

Eqn (4) shows that f_o is independent of supply voltage VCC

The duty cycle is the ratio of the time t_d during which the output is low to the total time period T. This definition is applicable to 555 Astable Multivibrators only; conventionally the duty cycle ratio is defined as the ratio as the time during which the output is high to the total time period.

$$\therefore \text{ Duty cycle} = t_d \, T \times 100$$

$$R_B + R_A + 2R_B \times 100 \qquad (5)$$

To obtain 50% duty cycle a diode should be connected across R_B and R_A must be a combination of a fixed resistor and a potentiometer. So that the potentiometer can be adjusted for the exact square waves.

DESIGN:

Design an Astable Multivibrators for a frequency of _____KHz with a duty cycle ratio of D = 50 %

$$\mathbf{fo = 1/T = 1.45 / (R_A + 2R_B)C}$$

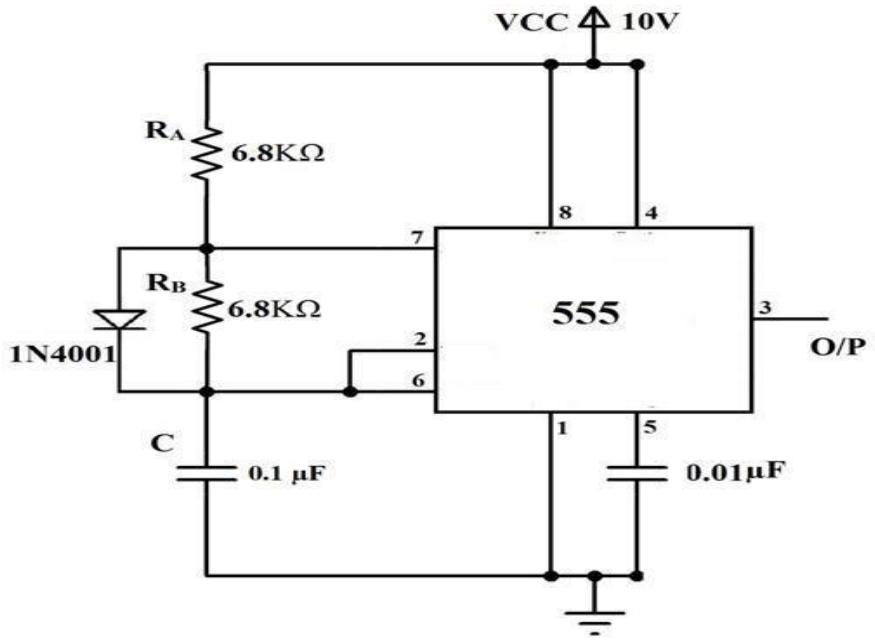
Choosing C = 1 μF; R_A =

560 D = R_B / R_A +2R_B=

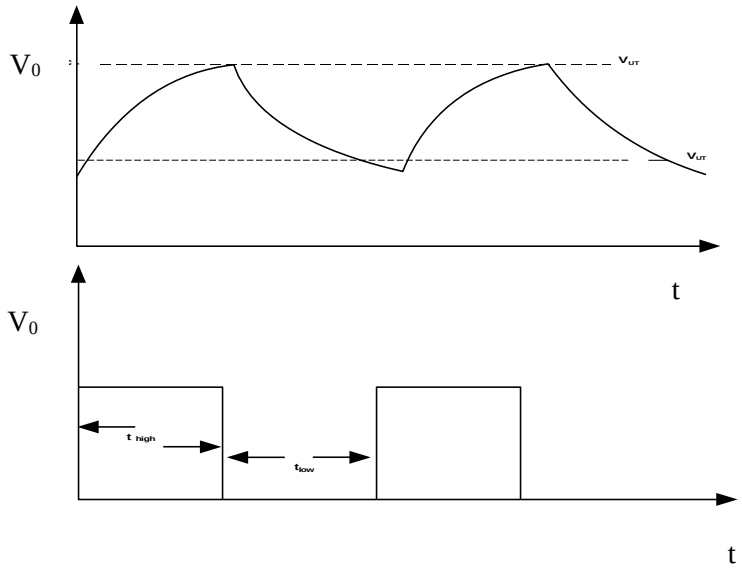
0.5 [50%]

R_B = _____

CIRCUIT DIAGRAM:



MODEL GRAPH:



TABULATION:

V_{cc} =

S. no	R_a	R_b	C	T_{on}		T_{off}		$T= T_{on} + T_{off}$		%Duty Cycle		Vopp (v) Squ	Vopp (v) Tri	1/3V_{cc}		2/3V_{cc}	
				Thero	Pract	Thero	Pract	Thero	Pract	Thero	Pract			Thero	Pract	Thero	Prac
1.																	
2.																	

PROCEDURE:

1. Rig-up the circuit of 555 Astable Multivibrators as shown in fig with the designed value of components.
2. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
3. Switch on the power supply to CRO and the circuit.
4. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings and frequency.
5. Switch off the power supply. Connect a diode across R_B as shown in dashed lines in

fig to make the Astable state with 50 % duty cycle ratio. Switch on the power supply.

Observe the output waveform. Draw to scale on a graph sheet.

VIVA QUESTIONS:

1. What is the other name of Astable Multivibrator?
2. Explain the working of Astable Multivibrator?
3. What is a quasi-stable state?
4. What are the applications of Astable Multivibrator?
5. Explain Hoe Astable Multivibrator can be used as a voltage to frequency converter?
6. For a symmetrical circuit how can you say that one transistor is on and one transistor if off?
7. Derive the equation for a time of an Astable Multivibrator?
8. Which type of biasing present in Astable Multivibrator?
9. How Astable Multivibrators acts as a free running oscillator?
10. Define time constant?

Result:

Thus, the Astable Multivibrators using 555 timer is designed and tested.

6(b) MONOSTABLE MULTIVIBRATOR

AIM: To study the operation of a Monostable Multivibrator using 555 IC

EQUIPMENTS & COMPONENTS:

1. C.R.O
2. Function generator
3. Multimeter
4. Bread board
5. ± 15 V variable power supply
6. 555 Timer IC
7. Resistors 10k
8. Capacitors 0.1μF,0.01μF(2)
9. Single stand wires

THEORY:

Monostable Multivibrators has one stable state and other is a quasi-stable state. The circuit is useful for generating single output pulse at adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components, resistor and a capacitor.

The stable state is the output low and quasi stable state is the output high. In the stable state transistor Q1 is 'on' and capacitor C is shorted out to ground. However upon application of a negative trigger pulse to pin2, Q1 is turned 'off' which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up towards V_{cc} through R_A. However when the voltage across C equal 2/3 VCC the upper comparator output switches form low to high which in turn drives the output to its low state via the output of the flip flop. At the same time the output of the flip flop turns Q1 'on' and hence C rapidly discharges through the transistor. The output remains low until a trigger is again applied. Then the cycle repeats.

The pulse width of the trigger input must be smaller than the expected pulse width of the output. The trigger pulse must be of negative going signal with amplitude larger than 1/3 VCC. The width of the output pulse is given by,

$$T = 1.1\ R_A C$$

DESIGN:

Given a pulse width of duration of 100 μs
Let C = 0.01 μ F;

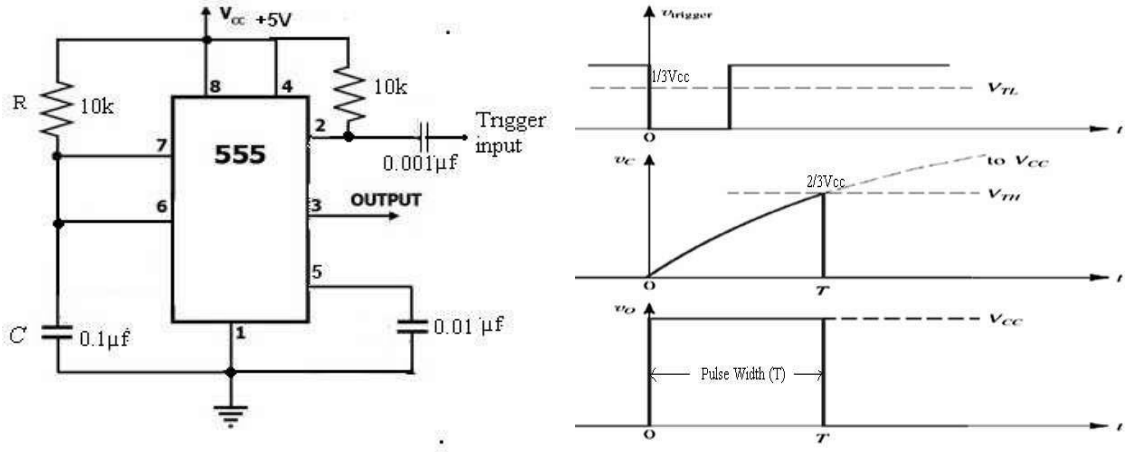
Frequency = _____KHz Here, $T = 1.1\ R_A C$

So, calculate R_A =

PROCEDURE:

1. Rig-up the circuit of 555 monostable Multivibrators as shown in fig with the designed value of components.
2. Connect the trigger input to pin 2 of 555 timer form the function generator.
3. Connect the CRO probes to pin 3 and 2 to display the output signal and the voltage across the timing capacitor. Set suitable voltage sensitively and time-base on the CRO.
4. Switch on the power supply to CRO and the circuit.
5. Observe the waveforms on the CRO and draw to scale on a graph sheet. Measure the voltage levels at which the capacitor starts charging and discharging, output high and low timings along with trigger pulse.

CIRCUIT DIAGRAM INPUT OUTPUT MODEL WAVEFORMS:



TABULATION:

Sl.no	Trigger input pulse Voltage	Resistor	capacitor	output voltage	Theoretical Time period	Practical Time period
1.						
2.						
3.						
4.						

VIVA QUESTIONS:

1. What are the features of 555 timer?
2. What are the applications of 555 timer?
3. Define duty cycle ratio.
4. What are the applications of monostable Multivibrators?
5. What is meant by quasi stable state?
6. What should be the amplitude of trigger pulse?

RESULT:

Thus, the Monostable Multivibrators using 555 timer is designed and tested.

Exp 7. PLL CHARACTERISTICS

AIM: To construct and study the operation of Phased Locked Loop (PLL) and its characteristics.

EQUIPMENTS & COMPONENTS:

S.NO	Components	Range	Quantity
1	IC 7490, 2N2222	-	1
2	Resistors	20kΩ, 2kΩ, 4.7kΩ, 10kΩ	1
3	Capacitors	0.001µF, 10µF	1 each
4	Function Generators	1Hz – 2 Hz	1
5	CRO	-	1
6	Dual Power supply	0 – 30V	1

FORMULA:

Free running frequency $f_o = 0.25/(R_T C_T)$

Lock in range $\Delta f_L = \pm 7.8\, f_0 / V$

Where, $V = +V_{CC} - (-V_{CC})$

Capture range, $\Delta f_c = \pm \left(\frac{\Delta f_L}{(2\pi)(3.6)(10^3)C} \right)^{1/2}$

PROCEDURE:

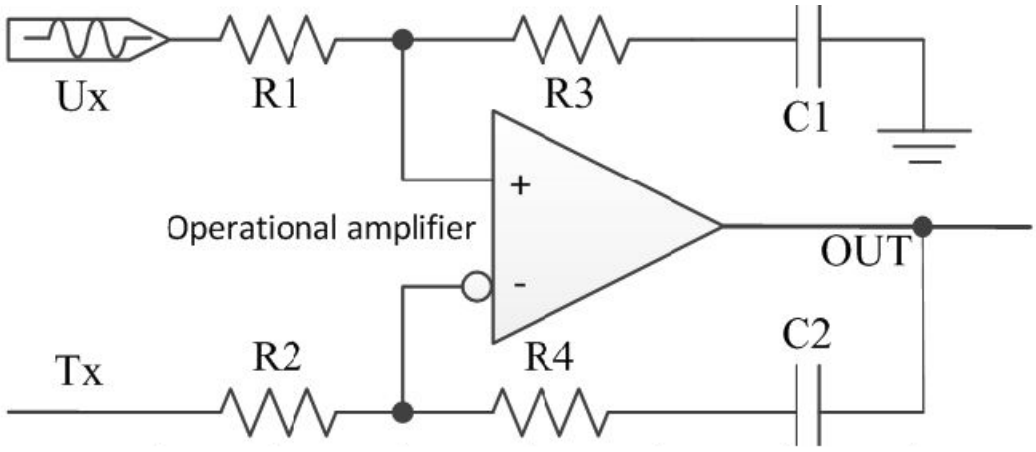
1. The connections are given as per the circuit diagram.
2. Measure the free running frequency of VCO at pin 4, with the input signal V_i set equal to zero. Compare it with the calculated value of $f_o = 0.25 / (R_T C_T)$.
3. Now apply the input signal of 1 V_{PP} square wave at a 1 KHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.
4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2.This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.

6. The lock range $\Delta f_L = (f_2 - f_4)$.Compare it with the theoretical value of Δf_L. The capture range is $\Delta f_c = (f_3 - f_1)$.Compare it with the theoretical value of capture range

THEORY:

The PLL consists of Phase detector, Low Pass Filter, Error Amplifier and VCO. The VCO is a free running Multivibrator operates at f_0 called free running frequency. The frequency deviation is directly proportional to the DC control voltage and hence it is called as VCO. If an input signal Vs. of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V0 of the VCO, if the two signals differs in frequency or phase an error voltage is generated, then the phase detector is a multiplier and produces $f_s \pm f_0$, the high frequency component fs+f0 is removed by LPF and the Low frequency component is amplified and applied as a control voltage to VCO. Vc shifts the VCO frequency to reduce the frequency difference between fs and f0, once this action starts the signals is in the capture range. The VCO continues to change the frequency till its output frequency is same as the input frequency then it is said to be a locked range.

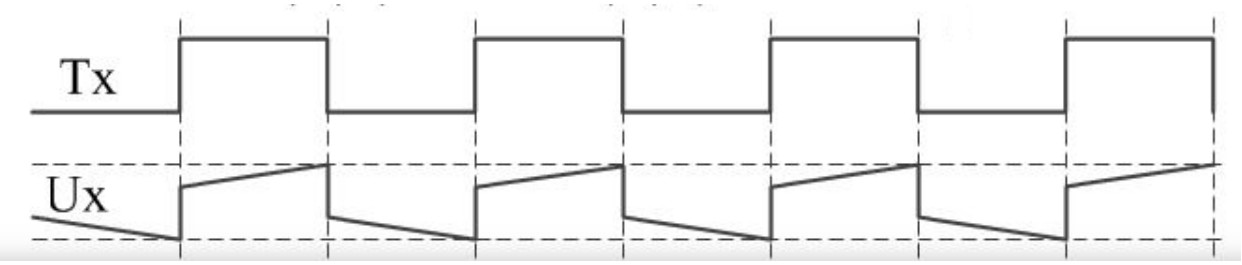
CIRCUIT DIAGRAM:



TABULATION:

S.No.	Input Frequency (kHz)	Output Frequency (kHz)

MODEL GRAPH:



RESULT:

Thus, the PLL is constructed and its characteristics are determined.

EXP 8. INTRODUCTION TO PCB DESIGN, FABRICATION & ASSEMBLY PROCESS AND TRANSMISSION LINES, CROSSTALK, AND ITS EFFECTS USING ORCAD

Printed Circuit Boards (PCBs) form the backbone of almost every electronic device. Understanding their design, fabrication, and assembly processes is critical for engineers and designers to produce reliable and high-performance electronics. This document provides an overview of these processes and discusses key considerations such as transmission lines, crosstalk, and their effects, especially in the context of design using OrCAD.

PCB Design Process

The PCB Design Process begins with defining the circuit requirements and ends with generating the files necessary for manufacturing. The steps include:

1. **Schematic Design**: The designer creates a schematic diagram, which serves as the blueprint of the circuit.
2. **Component Placement**: Components are placed on the PCB layout while considering functionality, thermal management, and signal integrity.
3. **Routing**: Interconnections are created between components using copper traces, adhering to electrical and manufacturing constraints.
4. **Design Rule Check (DRC)**: The design is validated against predefined rules to ensure manufacturability and performance.
5. **Gerber File Generation**: The design is exported into industry-standard Gerber files for fabrication.

PCB Fabrication Process

Fabrication transforms the digital design into a physical board. Key steps include:

1. **Substrate Preparation**: A Dielectric Substrate, such as FR4, is selected and prepared.
2. **Copper Lamination**: Copper layers are bonded to the substrate.
3. **Patterning**: The copper is etched to create traces based on the design.
4. **Drilling**: Holes for vias and through-hole components are drilled.
5. **Plating and Coating**: The board undergoes plating to improve conductivity and solderability.
6. **Solder Mask Application**: A protective layer is applied to prevent short circuits and oxidation.
7. **Silkscreen Printing**: Labels and component identifiers are added.

PCB Assembly Process

Assembly involves populating the fabricated board with components. The steps are:

1. **Solder Paste Application**: Solder Paste is applied to pads using a stencil.
2. **Component Placement**: Components are placed on the board, often using automated machines.
3. **Reflow Soldering**: The board passes through a reflow oven to solder surface-mount components.
4. **Inspection and Testing**: Automated Optical Inspection (AOI) and functional tests ensure quality and performance.

Transmission Lines and Crosstalk in PCB Design

Transmission Lines

In high-speed PCB designs, traces can act as transmission lines. Key factors affecting their performance include:

- **Impedance Matching**: Ensuring the trace impedance matches the source and load to prevent reflections.
- **Length Matching**: critical for differential pairs to ensure signal integrity.
- **Material Properties**: The dielectric constant and loss tangent of the substrate affect signal propagation.

Crosstalk

Crosstalk occurs when signals in one trace interfere with an adjacent trace, leading to noise and performance degradation.

- **Causes**:
    - Inductive and capacitive coupling between traces.
    - High-speed signals and improper spacing.
- **Mitigation**:
    - Increase spacing between traces.
    - Use ground planes and shielding.
    - Route critical signals on separate layers.

Using OrCAD for PCB Design

OrCAD is a powerful software tool for PCB design. Its features facilitate the entire process, including:

1. **Schematic Capture**: OrCAD Capture allows seamless schematic creation.

2. **PCB Layout**: OrCAD PCB Designer offers advanced routing and design rule checking.
3. **Simulation**: Tools for signal integrity analysis help identify and mitigate issues like reflections and crosstalk.
4. **Manufacturing Outputs**: OrCAD generates accurate Gerber files and Bill of Materials (BOM)

EXP 9. USING ORCAD TOOL, PRACTICE THE BASIC RC CIRCUIT. ACTIVE BANDPASS FILTER

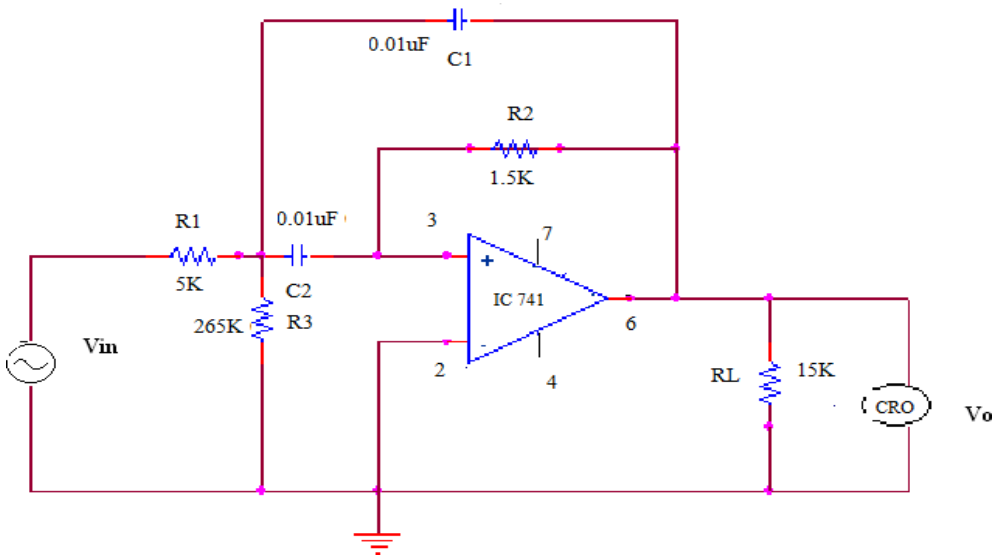
AIM:

To design and simulate a band pass filter using PSpice and to obtain the frequency response.

SOFTWARE REQUIRED:

System with PSpice software.

CIRCUIT DIAGRAM:



PROCEDURE:

General Steps for PCB design using Orcad:

1. Design circuit using schematic entry package (Capture).
2. Generate netlist for PCB package.
3. Import netlist into PCB package (Layout Plus).
4. Place components, route board.
5. Generate machining (Gerber) files for PCB plant.
6. View the PCB Layout.

Schematic Design:

1. Use Capture to enter the design (Refer SPICE Experiments). While creating new project, Select→ Schematic, here the component

library consist of more components than in PSPICE Library.

2. Connectors can be used for inputs, and outputs. Select Connector→ B2S for inputs and Outputs.
3. Select project in project window.
4. Check for any design rules violations. Tools → Design Rules Check. Any violation in electrical Rules, Unconnected Nets, Invalid References and Duplicate References will be checked. To view drc file, Outputs→ *.drc
5. Create Bill of materials. A file with details of components used, quantity and specifications will be generated. Tools → Bill of materials. To view bom file, Outputs→ *.bom
6. Create netlist. A file that is used in layout preparation is created. Tools → Create Netlist. Choose *Layout* tab → OK. A netlist file (.mnl extension) will be created.
7. Close Capture.

PCB Layout:

- Run Layout Plus. An ORCAD LAYOUT Window opens.
- Choose File→New. Another window, LAYOUT PLUS, opens.
- Select a "technology file" appropriate for the design.
- These are in Program

  C:\ Program Files\ Orcad\ Layout_Plus\ Data and select DEFAULT.TCH.

- Choose the created netlist file (.mnl extension).

If some of the components chosen from the Orcad Capture libraries did not have PCB footprints associated with them "*Cannot find footprint for...*" messages will be displayed. If this happens, choose "*link existing footprint to component*". Browse footprint libraries to find the required footprint. Eg: Capacitor→ TM- DISC, TM-CYLND, Jumper→J0, Diode→TM-DIODE, Resistor→TM-AXIAL, Connector → BCON100T etc.

Place Components:

1. Draw the border. Tool→Obstacle→Select tool. Draw the board outline.
2. Select thickness of different grids. Size is usually specified in mils (m), where 1 mil = 0.001 inch. Options→System Setting, Select Visible Grid→ 100, Detail Grid→ 25, Place Grid →25, Routing Grid→ 25, Via grid →10.
3. Select the origin. Tool→ Dimension→ Move Datum. Place the datum (A circle with a cross symbol) to one corner of outline. Origin will have the coordinate (X=0, Y=0).
4. Drag the components to inside the board outline. Tool→ Component→Select tool→ click on required component and drag it.
5. Right click to see some options, including rotate.

Choose Layers:

1. Select width of the net. View Spreadsheet →Net→Width→ Enter Min (Minimum) →25, Con (Connection)→50, Max (Maximum)→ 100. (All units in mils).
2. Select Route Spacing. View Spreadsheet→ Strategy →Route Spacing→ Set all to 12. (All units in mils)

3. Select layer to route. View Spreadsheet → Layers→ Layer Type.

4. Enable only the layers for routing, set other layers to unused (double click on the Layer Type→ select all to *unused routing*).

5. For a single sided board use only the "*bottom*" layer. Select layers needed then right click, select *properties*, then *set routing* to enable layers.

Routing:

1. To automatically route, select Auto→ auto route→board.

2. After an autoroute, board is completed.

3. Sometimes it is more appropriate to use manual routing. For

manual routing turn on *Edit Segment Mode* icon on top.

4. All tracks may not be routed after autoroute. Via can be added for connecting this track. Right click→ Add Via.

5. If any modification is required, unroute the board. Auto→ Unroute→ Board.

Generate Machining Files (Gerber files):

A Gerber file is a file that contains the information from Layout necessary for the prototyping machine to mill, drill and cut the PCB.

1. The machining files required to manufacture the PCB are generated by the "post processor". From *options* menu choose "*Post Process Settings*". In the spreadsheet, select the layers needed to manufacture. Post processor Settings→ Batch Enabled→ Properties→ First disable all, then enable BOT (BOTTOM), SMB (Solder Mask Bottom) and SMT (Solder Mask Top), SST (Silk Screen Top), AST (Assembly Top) and DRD (Drill Drawing).

2. Select Options → Gerber Settings → OK.

3. Choose Auto→ Run Post Processor to generate the files (.GTD file). The files generated by the post processor are the only ones needed for the PCB plant to make the board.

Viewing PCB Layout:

1. Open ORCAD LAYOUT window.
2. Open created GTD file. Tools→Gerb tool→Open→ Open created *.GTD file.
3. Select .BOT→Redraw, to view PCB bottom.

   .SMB→ Redraw, Solder mask bottom.

   .SMT→ Redraw, Solder mask Top.

   .SST→ Redraw, Silk Screen Top. \

Creating new footprint:

Footprint of all components may not be available in LAYOUT Library. New Libraries for required footprint can be created.

1. Open LAYOUT PLUS window.
2. Select Library manager. Tools→Library Manager.
3. We can create new footprint, or modify existing footprint. Select a footprint that looks similar to new requirement → Edit it→ Create

New Library → Change the name of footprint→Save footprint in new Library.

4. Component footprint can be selected from newly created library at the time of layout preparation.

Creating new part:

New parts can be created in ORCAD.

1. Open ORCAD capture. Create new schematic project. File→New→
2. Create a library of part symbols. File→New→Library. A new folder and a library file are created.
3. Save the library file. Right click library file→ Save As→Give name.
4. Now add part to the library. Right click library file → New Part. Enter part name.
5. A workspace for part creation opens. Using toolbar in the right side, create a new part.
6. Save the part and close the window.

PROCEDURE:

1. Open e-Sim.
2. Go to file option in the main menu and select new project.
3. Go to place part and select the components and place in the schematic window.
4. Add wires to all the components and specify the values of the components.
5. Go to Pspice in the main menu and check for errors in the netlist and set up the simulation profile by adding required traces.
6. Observe the output waveform

RESULT:

Thus, the Active Band pass second order filter circuit is simulated and the required frequency response graphs are plotted.

EXP 10. DESIGN AND FABRICATE A PCB FOR REGULATED POWER SUPPLY WITH FILTER AND REGULATION SECTIONS.

AIM:

- To create circuit schematic.
- To simulate line regulation of circuit.

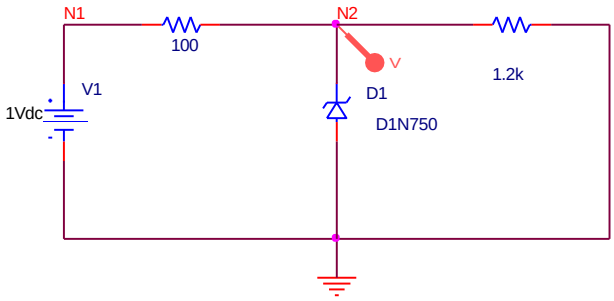
TOOL REQUIRED:

SPICE circuit simulator installed in a Personal Computer.

THEORY:

The function of a regulator is to provide a constant output voltage to a load connected in parallel with it, in spite of the ripples in the supply voltage or the variation in the load current. A Zener diode of break down voltage V_Z is reverse connected to an input voltage source V_1 across a load resistance R_2 and a series resistor R_1. The voltage across the Zener will remain steady at its break down voltage V_Z. Hence a regulated DC output voltage is obtained across R_2, whenever the input voltage remains within a minimum and maximum voltage.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Open the available SPICE simulation software. OrCAD →CAPTURE CIS.
2. Create a new project. Name the Project. Give location to save Project.
3. Place Parts from Libraries. Libraries→DIODE, Part→ D1N750.
4. Edit the values of Parts.
5. Place Ground. Connect the parts using Place Wire.
6. Simulate the circuit. Zener diode D1N750 has breakdown voltage, VB=4.7V. PSpice→New Simulation Profile. Analysis Type→DC Sweep, Name→V1, Sweep type→Linear, Start value→4V, End value→6V, Increment→1V.
7. Run the simulation.

* Data statements

D_D1 0 N2 D1N750

R_R1 N1 N2 100

R_R2 N2 0 1.2k

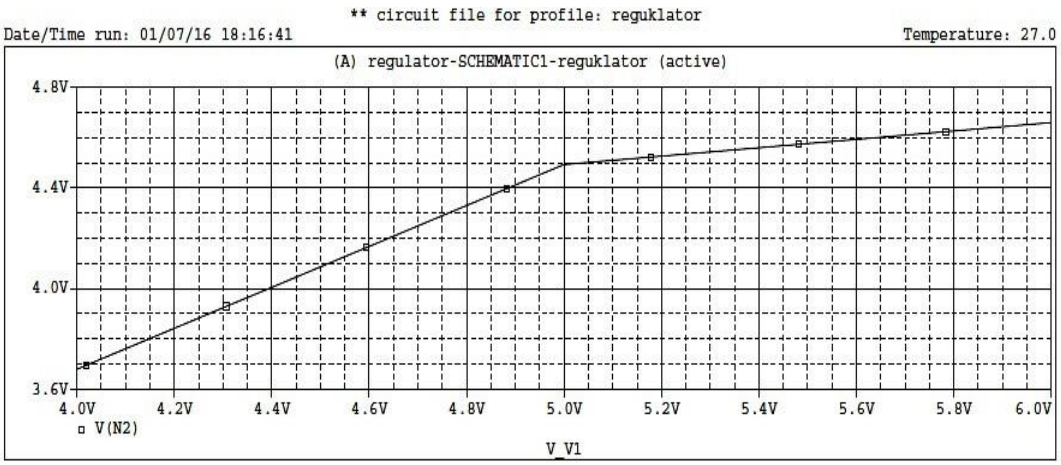
V_V1 N1 0 1Vdc

*Analysis directives:

.DC LIN V_V1 4 6 1

.PROBE

OBSERVATION:



RESULT:

Regulated power supply using Zener diode is setup and simulated using SPICE.

EXP 11. WIEN BRIDGE OSCILLATORS USING OP-AMP.

AIM:

To design the following sine wave oscillators

a) Wien Bridge Oscillator with the frequency of 1 KHz.
b) RC Phase shift oscillator with the frequency of 200 Hz.

COMPONENTS REQUIRED:

S.No	Components	Range	Quantity
1.	Op-amp	IC 741	1
2.	Dual trace supply	(0-30) V	1
3.	Function Generator	(0-2) MHz	1
4.	Resistors		
5.	Capacitors		
6	CRO	(0-30) MHz	1
7	Probes	--	--

Equations Related to the Experiments:

a) **Wien Bridge Oscillator**

Closed loop gain $A_v = (1+R_f/R_1) = 3$ Frequency of Oscillation $f_a = 1/(2\pi RC)$

DESIGN OF WIEN BRIDGE OSCILLATOR:

Gain required for sustained oscillation is $A_v = 1/\beta = 3$ (PASS BAND GAIN) (i.e.) $1+R_f/R_1 = 3$

$$\therefore R_f = 2R_1$$

Frequency of Oscillation $f_o = 1/2\pi R C$

Given $f_o = 1$ KHz Let

$C = 0.05\ \mu F$

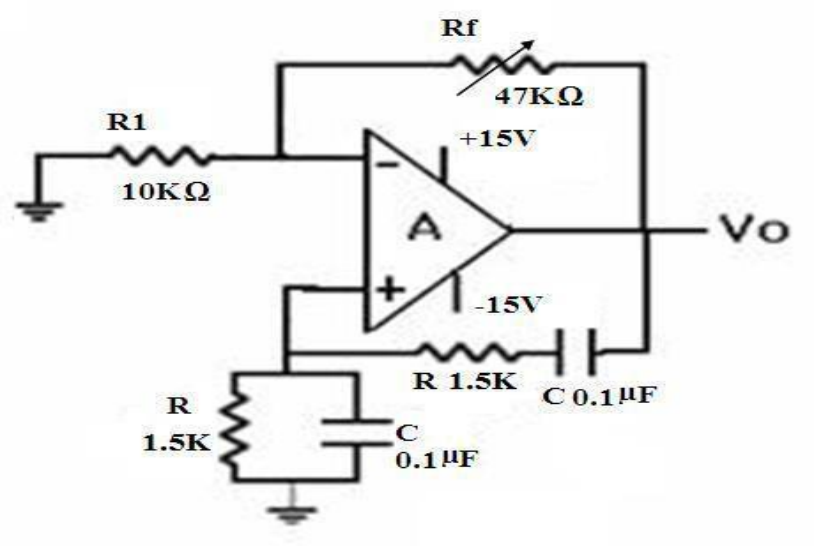
$\therefore R = 1/2\ \pi f_o C$

$R = 3.2\ K\Omega$

Let R1 = 10 KΩ

$\therefore$ Rf = 2 * 10 KΩ

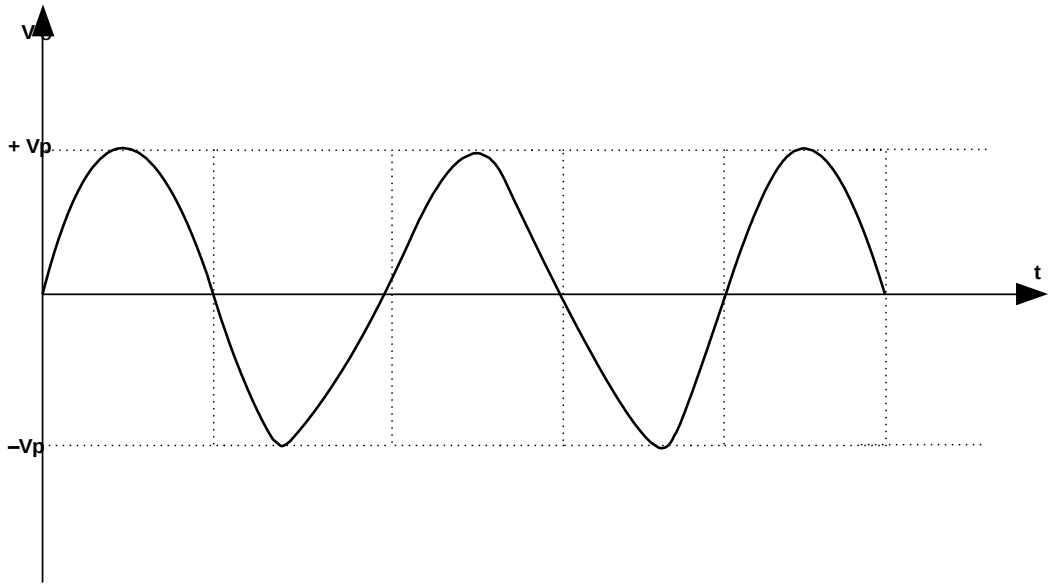
CIRCUIT DIAGRAM:



Tabulation:

Derived frequency (Hz)	Observed frequency (Hz)	Amplitude (V)	Time period (ms)

Model Graph:



Procedure:

1. Connect the components as shown in the circuit.
2. Switch on the power supply and CRO.
3. Note down the output voltage at CRO.
4. Plot the output waveform on the graph.
5. Redesign the circuit to generate the sine wave of frequency 2 KHz.
6. Compare the output with the theoretical value of oscillation.

Observation:

Peak to peak amplitude of the output = Volts.
Frequency of oscillation = Hz.

Result:

Thus, Wien Bridge Oscillator was designed using op-amp and tested.

EXP 12. DESIGN A VOLTAGE DIVIDER CIRCUIT WITH SPICE SIMULATOR

AIM:

To familiarize with SPICE simulator using a voltage divider circuit.

OBJECTIVES:

- To create circuit schematic.
- To simulate a circuit.
- To view and understand Netlist.
- To view Output File and understand Analysis Directive.
- To view simulated output.

TOOL REQUIRED:

SPICE circuit simulator installed in a Personal Computer.

THEORY:

The voltage divider circuit consists of resistors connected in series and parallel.

According to voltage division rule, voltage will be dropped across different resistors.

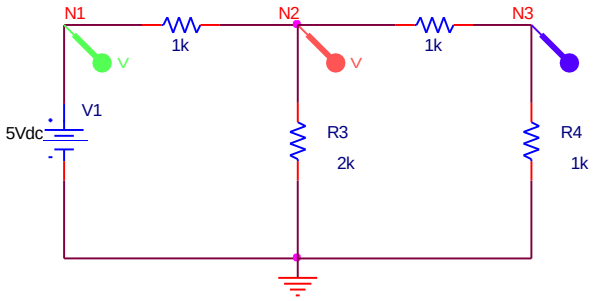
PROCEDURE:

1. Open the available SPICE simulation software. C:\Program Files\ORCAD\CAPTURE
   → CAPTURE CIS
2. Create a new project. File →New→Project.
3. Name the Project. Select→Analog or Mixed Signal Circuit Wizard.
4. Give location to save Project. Browse→Select path
5. Select the Part Symbol Libraries to be Included. Select Libraries →Add→Finish.
6. Schematic Window opens. Place Parts from Libraries. Libraries→ANALOG, Part→R. Libraries→SOURCE, Part→ VDC.
7. Edit the values of Parts. Double click on value→ Give new value.
8. Place Ground. Library→ CAPSYM, Symbol→ GND, Name→0.
9. Connect the parts using Place Wire.
10. Name the nodes using Place Net Alias.
11. Connect Voltage/Level Marker, from where outputs are required.
12. Simulate the circuit. PSpice→New Simulation Profile. Analysis Type→DC Sweep, Name→V1, Sweep type→Linear, Start value→ 0V, End value→10V, Increment→ 1V.
13. Run the simulation. Probe window opens, showing the voltages

measured by Voltage/Level Marker. New traces can be added in this plot. Trace→Add trace. Axis range can be edited. Plot→ X Axis→Data range → User defined→ Enter Start to End value→OK. New plot can be added in the window. Plot→ Add plot to window. Select the new plot and add traces.

14. Data statements will be specified in netlist. PSpice→View Netlist.
15. SPICE will generate an output file that contains the values of all voltages and currents in the circuit, analysis directives and libraries included.

CIRCUIT DIAGRAM:



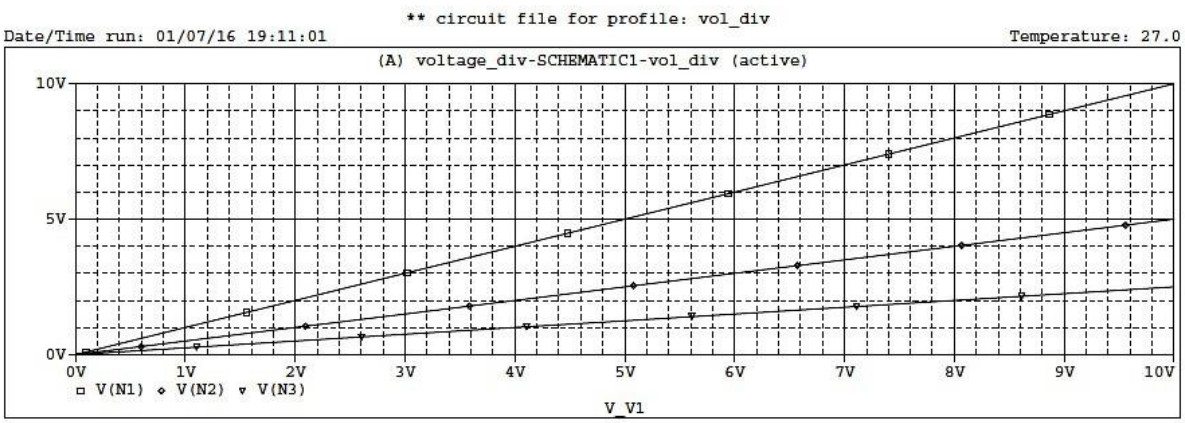
* Data statements

```
V_V1        N1 0 5Vdc
R_R1        N1 N2  1k
R_R2        N2 N3  1k
R_R3        N2  0 2k
R_R4        N3 0  1k
```

*Analysis directives:

```
.DC LIN V_V1 0 10 1
.PROBE
```

OBSERVATION:



RESULT:

Familiarized with SPICE simulation software using a voltage divider circuit. Created the circuit schematic and simulated the circuit. Netlist and Analysis directives are studied.