SRM VALLIAMMAI ENGINEERING OLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF MEDICAL ELECTRONICS

QUESTION BANK

IV SEMESTER

MD3463 – ANALOG AND DIGITAL INTEGRATED CIRCUITS

Regulation – 2023

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Prepared by

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SUBJECT : MD3463 – ANALOG AND DIGITAL INTEGRATED CIRCUITS

SEM / YEAR: IV/ II - YEAR B.E.

UNIT I

INTRODUCTION TO OPERATIONAL AMPLIFIER AND ITSAPPLICATIONS

Operational amplifier –ideal characteristics, Performance Parameters, Linear and Nonlinear Circuits and their analysis- voltage follower, Inverting amplifier, Non-inverting Amplifiers, Differentiator, Integrator, Voltage to Current converter, Instrumentation amplifier, Low pass, High pass filter and band pass filters, Comparator, Multivibrator and Schmitt trigger.

PART – A

Q. No	Questions	CO	BT Level	Competence
1.	What is an operational amplifier?	CO1	BTL 1	Remembering
2.	Write down the characteristics of ideal operational amplifier.	CO1	BTL 1	Remembering
3.	Differentiate the ideal and practical characteristics of an op-amp.	CO1	BTL 2	Understanding
4.	Draw the Internal Block diagram of Op – Amp (IC 741).	CO1	BTL 2	Understanding
5.	Define Slew rate.	CO1	BTL 1	Remembering
6.	Why open loop OP-AMP configurations are not used in linear applications?	CO1	BTL 2	Understanding
7.	Define virtual ground of an OP-Amp.	CO1	BTL 1	Remembering
8.	What are the applications of V-I converter?	CO1	BTL 1	Remembering
9.	Mention some of the linear applications of op – amps.	CO1	BTL 2	Understanding
10.	Mention some of the non – linear applications of op-amps.	CO1	BTL 2	Understanding
11.	What are the areas of application of non-linear op- amp circuits?	CO1	BTL 1	Remembering
12.	Give an application of inverting amplifier.	CO1	BTL 2	Understanding
13.	What is a differentiator?	CO1	BTL 1	Remembering
14.	What are the main drawbacks of ideal differentiator?	CO1	BTL 1	Remembering
15.	What are the characteristics of the comparator?	CO1	BTL 1	Remembering
16.	Mention some commonly used active filters.	CO1	BTL 2	Understanding
17.	Why IC 741 is not used for high frequency applications?	CO1	BTL 2	Understanding
18.	What is voltage follower?	CO1	BTL 1	Remembering
19.	What is the need for an instrumentation amplifier?	CO1	BTL 1	Remembering
20.	List the features of instrumentation amplifier.	CO1	BTL 2	Understanding
21	What do you mean by multivibrator?	CO1	BTL 2	Understanding
22	What is an astable multivibrator?	CO1	BTL 1	Remembering
23	What is a bistable multivibrator?	CO1	BTL 1	Remembering
24	What is a Schmitt trigger?	CO1	BTL 1	Remembering

PART B

1.	With a help of a block diagram, explain the various stages present in an operational amplifier.	(16)	**CO1**	**BTL 4**	**Analyzing**
2	(i) Write down the characteristics and their respective values of an ideal Operational amplifier. (ii) Compare the ideal and practical characteristics of IC741.	(10) (6)	**CO1**	**BTL 4**	**Analyzing**
3	List and explain the DC characteristics of an operational amplifier.	(16)	**CO1**	**BTL 4**	**Analyzing**
4	Explain in detail about Open and closed loop configurations of op-amp.	(16)	**CO1**	**BTL 3**	**Applying**
5	Describe about Inverting amplifier and Non-Inverting amplifier with neat diagram.	(16)	**CO1**	**BTL 4**	**Analyzing**
6	Describe the operation of voltage follower with neat diagram.	(16)	**CO1**	**BTL 3**	**Applying**
7	(i) Discuss the working of a differentiator using op-amp. (ii) List out the errors in ideal differentiator and analyse the practical differentiator for those error.	(13) (3)	**CO1**	**BTL 4**	**Analyzing**
8	With neat figures describe the working of an integrator using op-amp.	(16)	**CO1**	**BTL 4**	**Analyzing**
9	Derive the expression for output voltage of an practical integrator.	(16)	**CO1**	**BTL 4**	**Analyzing**
10	Write the operation of Current to Voltage and Voltage to current converter circuits.	(16)	**CO1**	**BTL 4**	**Analyzing**
11	Explain the working of three op-amp Instrumentation Amplifier with neat diagram.	(16)	**CO1**	**BTL 3**	**Applying**
12	Explain the working of Low pass filter and High pass filter in detail.	(16)	**CO1**	**BTL 3**	**Applying**
13	Explain the working of Band pass filter in detail.	(16)	**CO1**	**BTL 3**	**Applying**
14	With neat diagram, explain the operation of a monostable multivibrator using opamp.	(16)	**CO1**	**BTL 4**	**Analyzing**
15	Illustrate the working of Astable Multivibrator using op-amp with applications in detail.	(16)	**CO1**	**BTL 3**	**Applying**
16	Describe about the working of Comparator with neat circuit diagram.	(16)	**CO1**	**BTL 4**	**Analyzing**
17	Explain the working of Schmitt Trigger with neat sketch.	(16)	**CO1**	**BTL 3**	**Applying**

UNIT II
DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS AND PLL

Types of D/A converter -Weighted resistor, R-2R ladder DAC, D/A Accuracy and Resolution. A/D converter - Flash, Dual slope, Successive approximation, A/D Accuracy and Resolution. Voltage controlled oscillator, Voltage to Frequency converters. PLL-Closed loop analysis of PLL, Frequency multiplication/ division, FSK demodulator.

PART - A

Q. No	Questions	CO	BT Level	Competence
1.	Classify the A/D converters based on their operational features.	**CO2**	**BTL 1**	**Remembering**
2.	List the direct type ADCs.	**CO2**	**BTL 2**	**Understanding**
3.	What is the principle of operation of successive Approximation ADC?	**CO2**	**BTL 1**	**Remembering**

4.	What is the main drawback of a dual-slop ADC?		**CO2**	**BTL 1**	**Remembering**
5.	Define conversion time.		**CO2**	**BTL 1**	**Remembering**
6.	Find the number of resistors required for an 8-bit weighted resistor D/A converter. Consider the smallest resistance is R and obtain those resistance values.		**CO2**	**BTL 2**	**Understanding**
7.	Mention the advantages of inverted R-2R (current type) ladder D/A converter over R -2R (voltage type) D/A converter?		**CO2**	**BTL 2**	**Understanding**
8.	Which is the fastest A/D converter? Give reason.		**CO2**	**BTL 2**	**Understanding**
9.	What would be produced by a DAC whose output range is 0-10v and whose input binary number is 10111100 (for a 8 bit DAC)?		**CO2**	**BTL 2**	**Understanding**
10.	Calculate the number of comparators required for realizing a 4 bit flash A/D converter.		**CO2**	**BTL 2**	**Understanding**
11.	A 12 bit D/A converter have resolution of 30 mV/ LSB. Find the full scale output voltage.		**CO2**	**BTL 2**	**Understanding**
12.	How many comparators are required to build n –bit flash type A/D converter?		**CO2**	**BTL 2**	**Understanding**
13.	What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is 0110 for a 4 bit DAC.		**CO2**	**BTL 2**	**Understanding**
14.	State the advantages of dual slope ADC.		**CO2**	**BTL 1**	**Remembering**
15.	What is voltage controlled oscillator?		**CO2**	**BTL 1**	**Remembering**
16.	Why VCO is also called as V to F converter?		**CO2**	**BTL 2**	**Understanding**
17.	Define capture range.		**CO2**	**BTL 1**	**Remembering**
18.	Outline the basic building blocks of PLL.		**CO2**	**BTL 1**	**Remembering**
19.	Define lock-in range of PLL.		**CO2**	**BTL 1**	**Remembering**
20.	What is Pull in time?		**CO2**	**BTL 1**	**Remembering**
21	Name two advantages of an R-2R ladder DAC over a weighted resistor DAC.		**CO2**	**BTL 2**	**Understanding**
22	Define resolution in a D/A converter.		**CO2**	**BTL 1**	**Remembering**
23	What is frequency shift keying technique?		**CO2**	**BTL 1**	**Remembering**
24	What is the main difference between frequency multiplication and division?		**CO2**	**BTL 1**	**Remembering**
	PART B				
1.	Describe about the Weighted resistor DAC with neat diagram.	(16)	**CO2**	**BTL 3**	**Applying**
2.	Explain in detail on the operational features of 4-bit weighted resistor type D/A converter.	(16)	**CO2**	**BTL 4**	**Analyzing**
3.	Analyze the working of R- 2R ladder type DAC.	(16)	**CO2**	**BTL 4**	**Analyzing**
4.	Describe the operation of voltage mode R- 2R ladder D/A converter.	(16)	**CO2**	**BTL 3**	**Applying**
5.	Explain the working of Inverted R- 2R ladder type DAC.	(16)	**CO2**	**BTL 4**	**Analyzing**
6.	Explain in detail about performance analysis of ADC.	(16)	**CO2**	**BTL 4**	**Analyzing**
7.	Elaborate the operation of flash type A/D converter with neat diagram.	(16)	**CO2**	**BTL 3**	**Applying**
8.	Explain in detail about the dual slope type ADC with neat sketch.	(16)	**CO2**	**BTL 3**	**Applying**

9.	Describe the working principle of successive approximation type ADC.	(16)	**CO2**	**BTL 3**	**Applying**
10.	Describe the operation of any two direct type of ADCs and Explain.	(16)	**CO2**	**BTL 3**	**Applying**
11.	Explain the working of a VCO and Derive the expression for voltage to frequency conversion factor.	(16)	**CO2**	**BTL 4**	**Analyzing**
12.	Illustrate the operation of VCO with neat block diagram. Also derive an expression for f0.	(16)	**CO2**	**BTL 4**	**Analyzing**
13.	Explain the process of capturing the lock and also derive for capture range and lock range.	(16)	**CO2**	**BTL 4**	**Analyzing**
14.	Describe the block diagram of PLL with neat sketch?	(16)	**CO2**	**BTL 3**	**Applying**
15.	Discuss any three applications of PLL in detail with neat circuit diagram.	(16)	**CO2**	**BTL 4**	**Analyzing**
16.	Describe the purpose and functioning of Frequency Multiplication/Division in detail.	(16)	**CO2**	**BTL 3**	**Applying**
17.	Construct the block diagram and explain working principle, characteristics of Frequency Demodulator.	(16)	**CO2**	**BTL 3**	**Applying**

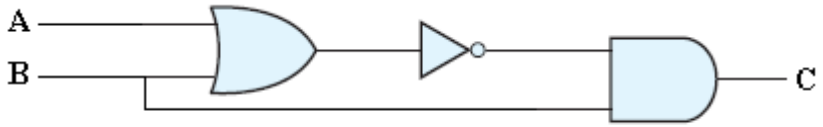
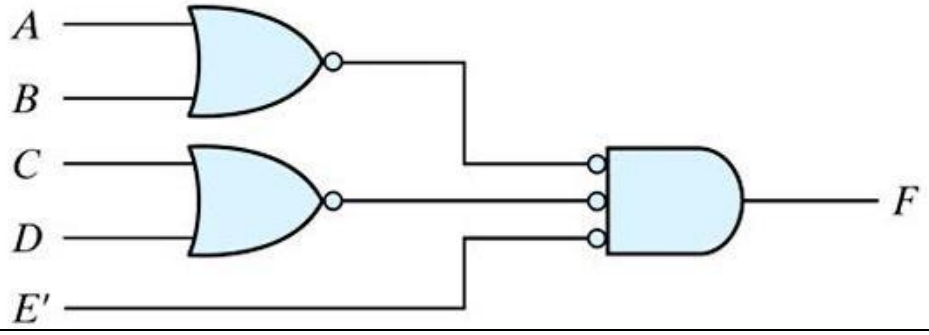
UNIT III

THE BASIC GATES AND COMBINATIONAL LOGIC CIRCUITS

Number Systems – Decimal, Binary, Octal, Hexadecimal, 1‘s and 2‘s complements, Codes –Binary, BCD, 84-2-1, 2421, Excess 3,Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map and tabulation methods. Logic families- TTL, MOS, CMOS, BiCMOS – Comparison of Logic families.

PART - A

Q. No	Questions	CO	BT Level	Competence
1.	Convert the given decimal numbers into their binary equivalent (108.364)10.	**CO3**	**BTL 2**	**Understanding**
2.	Identify the Boolean function $Y=A+BC$ in a sum of minterrms.	**CO3**	**BTL 2**	**Understanding**
3.	Solve the pair of decimal number to BCD and Add (65)10+ (58)10.	**CO3**	**BTL 1**	**Remembering**
4.	Outline the concept of duality in Boolean algebra.	**CO3**	**BTL 1**	**Remembering**
5.	Convert A3BH and 2F3H into Binary and Octal respectively.	**CO3**	**BTL 1**	**Remembering**
6.	Construct the Boolean function to a minimum number of literals XY+X’Z+YZ.	**CO3**	**BTL 1**	**Remembering**
7.	Convert (115)10 into hexadecimal numbers.	**CO3**	**BTL 2**	**Understanding**
8.	Define ‘Minterm’ and ‘Maxterm’.	**CO3**	**BTL 2**	**Understanding**
9.	Find the Excess-3 code for the following decimal numbers. (18)10 and (56)10.	**CO3**	**BTL 2**	**Understanding**
10.	Draw the active high tri-state Gate & write its truth table.	**CO3**	**BTL 2**	**Understanding**
11.	Determine AND gate and OR gate using NAND gates.	**CO3**	**BTL 2**	**Understanding**
12.	Write the principle of Distributive law.	**CO3**	**BTL 1**	**Remembering**

13.	What is meant by Prime Implicants and Essential prime implicants?		**CO3**	**BTL 1**	**Remembering**
14.	Simplify the Boolean expression: F=XY+X(Y+Z) +Y(Y+Z).		**CO3**	**BTL 2**	**Understanding**
15.	Compute the given function using NAND gates only. F(X, Y, Z) =Σm (0, 6).		**CO3**	**BTL 2**	**Understanding**
16.	Write the equivalent Gray code for [10110]2.		**CO3**	**BTL 1**	**Remembering**
17.	If A & B are Boolean variables and if A=1 &$A+B$=0, determine B?		**CO3**	**BTL 2**	**Understanding**
18.	Apply De-Morgan's theorem to simplify$A+BC$.		**CO3**	**BTL 2**	**Understanding**
19.	Implement Y= Σ (1, 4, 5, 6, 7) in SOP form using AOI logic.		**CO3**	**BTL 2**	**Understanding**
20.	Determine the Boolean expression for the output of the system shown in figure. 		**CO3**	**BTL 2**	**Understanding**
21	Perform 2's complement subtraction of 010110 – 100101.		**CO3**	**BTL 2**	**Understanding**
22	Interpret the Boolean function and the truth table of the given logic.		**CO3**	**BTL 2**	**Understanding**
23	Write the Boolean expression for the output of the system shown in figure 		**CO3**	**BTL 2**	**Understanding**
24	Reduce the expression $ABC+ABC$ using Boolean theorems.		**CO3**	**BTL 1**	**Remembering**
	PART- B				
1.	Simplify the Minimized logic function using K-Maps. F (A, B, C, D) = Σm (1, 3, 5, 8, 9, 11, 15) + Σd (2, 13). Implement the minimal SOP using NAND and NOR gates.	(16)	**CO3**	**BTL 3**	**Applying**
2.	Find the function F(A,B,C,D,E) = Σm (1,4,6,10,20,22,24,26)+ Σd(0,11,16,27) using K-map method. Draw the circuit of the minimal expression using basic gates.	(16)	**CO3**	**BTL 3**	**Applying**
3.	Analyze the given function Y (M, N, O, P, Q) =Σm(0,2,4,6,9,13,21,23,25,29,31). Draw the K-map and implement the simplified expression using basic gates.	(16)	**CO3**	**BTL 3**	**Applying**
4.	Minimize the following Boolean expressions using Boolean Algebra and draw the logic diagram. (i) F (X, Y, Z) =$(X+Y)(X(Y+Z))+XY+XZ$. (ii) F (X, Y, Z) =$XYZ+XYZ+XY$ (iii) F(X,Y,Z) =$XYZ+XZ+YZ$	 (6) (5) (5)	**CO3**	**BTL 3**	**Applying**
5.	(i) Explain about Excess-3 codes and Gray Code with an	(6)	**CO3**	**BTL 3**	**Applying**

	example. (ii) Convert the Gray code (110101) to Binary code. (iii) Convert the binary number (10101101)2 to Gray code	(5) (5)			
6.	Using K-map method, Reduce the following Boolean function F=Σm (0, 2, 3, 6, 7) + Σd (8, 10, 11, 15) and obtain minimal SOP.	(16)	**CO3**	**BTL 3**	**Applying**
7.	Write the minimized Boolean expression for the function using K-map and draw the logic diagram. F (w, x, y,z)=Σm(0,1,2,4,5,6,8,9,12,13,14).	(16)	**CO3**	**BTL 3**	**Applying**
8.	Illustrate the logical Expression on a 4-variable K – map F=ABCD+AB'C'D'+AB'C+AB & realize using only NAND gates.	(16)	**CO3**	**BTL 3**	**Applying**
9.	Elaborate the minimization of the given Boolean function using Quine-Mc-Cluskey method F=Σm (0, 1, 2, 5, 7, 8, 9, 10, 13, 15). Realize the simplified function using logic gates.	(16)	**CO3**	**BTL 4**	**Analyzing**
10.	Using K-map method, simplify the given Boolean function and obtain minimum POS expression and draw the logic diagram. X=Πm(1,3,5,7,9)+Πd(8,11,15).	(16)	**CO3**	**BTL 4**	**Analyzing**
11.	Simplify using Karnaugh Map for the following functions and draw the logic diagram using basic gates. Y (A, B,C,D)=ΠM(0,3,4,9,10,12)+Πd(2,7,8,13)	(16)	**CO3**	**BTL 3**	**Applying**
12.	Solve the following Function using Tabulation method F=Σm(1,2,3,7,8,9,10,11,14,15) and realize the circuit using logic gates.	(16)	**CO3**	**BTL 4**	**Analyzing**
13.	(i) Solve (725.25)8 to its decimal, binary and Hexadecimal equivalent. (ii) Find 1's and 2's Complement of 8-digit binary number 10101101.	(8) (8)	**CO3**	**BTL 3**	**Applying**
14.	(i) Implement Y=$(A+C)(A+D)(A+B+C)$ (ii) Solve by perfect induction (a) A+AB = A (b) A(A+B) = A (c) A+A'B = A+B and (d) A(A'+B) =AB	(8) (8)	**CO3**	**BTL 3**	**Applying**
15.	Minimize the following Boolean function using K-map and implement the same using only NAND gates. F (A, B, C, D) = (D'+A'B'C' + AB'C' + A'BC'D).	(16)	**CO3**	**BTL 3**	**Applying**
16.	Determine simplified SOP for the following Boolean function using Quine- McCluskey Method. F(A, B, C, D) = Σm(1, 3, 4, 5, 9, 10, 11) + Σd(6, 8).	(16)	**CO3**	**BTL 4**	**Analyzing**
17.	(a) Convert the following:	(8)	**CO3**	**BTL 4**	**Analyzing**

	(i) $(A3B)_{16}$ to Decimal number (ii) $(32)_8$ to Hexadecimal number (b) Subtract $(1010)_2$ from $(1000)_2$ using 1's and 2's Complement.	(8)			

UNIT IV **COMBINATIONAL LOGIC CIRCUITS**					
Design of combinational circuits - Code-Converters, Half and Full Adders, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Magnitude Comparator, Decoder, Encoder, Priority Encoder, and Mux/Demux.					
PART - A					
Q. No	Questions		**CO**	**BT Level**	**Competence**
1.	Define combinational circuits.		**CO4**	**BTL 1**	**Remembering**
2.	Name some of the combinational circuits.		**CO4**	**BTL 1**	**Remembering**
3.	Summarize the design procedure of combinational circuits.		**CO4**	**BTL 1**	**Remembering**
4.	Write the Boolean expression for a half adder.		**CO4**	**BTL 1**	**Remembering**
5.	Draw a full adder circuit.		**CO4**	**BTL 1**	**Remembering**
6.	From the truth table derive the logic equation of a half subtractor.		**CO4**	**BTL 1**	**Remembering**
7.	Write down the limitation on the speed of an adder.		**CO4**	**BTL 2**	**Understanding**
8.	Differentiate between half adder and full adder.		**CO4**	**BTL 2**	**Understanding**
9.	Why is MUX called as a data selector?		**CO4**	**BTL 2**	**Understanding**
10.	List out the applications of multiplexer.		**CO4**	**BTL 2**	**Understanding**
11.	Mention the uses of demultiplexer.		**CO4**	**BTL 2**	**Understanding**
12.	How the decoder functions as a demultiplexer?		**CO4**	**BTL 2**	**Understanding**
13.	What do you mean by comparator?		**CO4**	**BTL 1**	**Remembering**
14.	Identify maximum number of outputs for a decoder with a 6-bit data word.		**CO4**	**BTL 1**	**Remembering**
15.	Point out the function of select inputs of a MUX		**CO4**	**BTL 1**	**Remembering**
16.	Analyze the schematic diagram of 2X1 multiplexer.		**CO4**	**BTL 2**	**Understanding**
17.	Distinguish between a demultiplexer and decoder.		**CO4**	**BTL 2**	**Understanding**
18.	Compare Multiplexer with Demultiplexer.		**CO4**	**BTL 2**	**Understanding**
19.	Define priority encoder.		**CO4**	**BTL 1**	**Remembering**
20.	State the uses of encoder.		**CO4**	**BTL 1**	**Remembering**
21	Mention the applications of Decoder.		**CO4**	**BTL 2**	**Understanding**
22	Examine the logic diagram of 2 to 4 decoder.		**CO4**	**BTL 2**	**Understanding**
23	Implement the Boolean function $F=\Sigma m\ (1, 2, 3, 7)$ using 3:8 decoder.		**CO4**	**BTL 2**	**Understanding**
24	How to design a 1-bit comparator using basic gates.		**CO4**	**BTL 2**	**Understanding**
PART- B					
1.	(i)Explain the design procedure for combinational circuits. (ii) Write a note on Carry Look Ahead adders.	(8) (8)	**CO4**	**BTL 3**	**Applying**
2.	Write the truth table for full adder, reduce the equation using k-map and design full adder using logic gates.	(16)	**CO4**	**BTL 3**	**Applying**
3.	Explain how full adder can be designed by using two half adder circuits with the circuit diagram.	(16)	**CO4**	**BTL 3**	**Applying**
4.	Write a brief note on the following combinational circuits: (i) Half subtractor	(8)	**CO4**	**BTL 3**	**Applying**

	(ii) Full subtractor	(8)			
5.	Explain the working of 4-bit parallel adder with necessary diagram and example.	(16)	**CO4**	**BTL 3**	**Applying**
6.	Construct a 4-bit BCD adder and with necessary illustrations.	(16)	**CO4**	**BTL 3**	**Applying**
7.	From the truth table derive the Boolean expression for 4:1 MUX and 8:1 MUX and implement using basic gates.	(16)	**CO4**	**BTL 2**	**Understanding**
8.	Implement the following Boolean function using 8X1 multiplexer. F(A,B,C,D)=$\bar{A}B\bar{D}$+ACD+$\bar{B}$CD+$\bar{A}\bar{C}$D	(16)	**CO4**	**BTL 3**	**Applying**
9.	Formulate the following Boolean function using 4 x 1 multiplexers. F(A,B,C,D)= Σ (1,2,3,6,7,8,11,12,14)	(16)	**CO4**	**BTL 3**	**Applying**
10.	Realize the function F(w, x, y, z)= Σm (1,4,6,7,8,9,10,11,15) using 4 to 1 Multiplexer.	(16)	**CO4**	**BTL 4**	**Analyzing**
11.	Describe about multiplexer and Simplify the following function using 8x1 Mux F(A,B,C,D)=Σm (0,2,6,10,11,12,13)+d (3,8,14).	(16)	**CO4**	**BTL 3**	**Applying**
12.	(i) Draw and explain the working of 1:8 demultiplexer and realize it using basic gates? (ii) Implement the following functions using demultiplexer: F1(A,B,C)=Σm(0,3,7) F2(A,B,C)=Σm(1,2,5)	(8) (8)	**CO4**	**BTL 4**	**Analyzing**
13.	Explain a 3X8 Priority encoder with truth table, Boolean expression and logic diagram.	(16)	**CO4**	**BTL 4**	**Analyzing**
14.	Design a logic circuit using 4x1 Multiplexer which has four inputs A, B, C, and D. The output X of the circuit is logic 1 if two or more inputs are logic 1.	(16)	**CO4**	**BTL 4**	**Analyzing**
15.	Obtain the circuit that implements an 8-to-3 binary encoder with neat diagram.	(16)	**CO4**	**BTL 3**	**Applying**
16.	Design a 2-bit magnitude comparator with three outputs: A>B, A=B and A<B.	(16)	**CO4**	**BTL 2**	**Understanding**
17.	With necessary diagrams, explain in detail about the working of a 4-bit look ahead carry adder. Also mention its advantages over conventional adder.	(16)	**CO4**	**BTL 3**	**Applying**

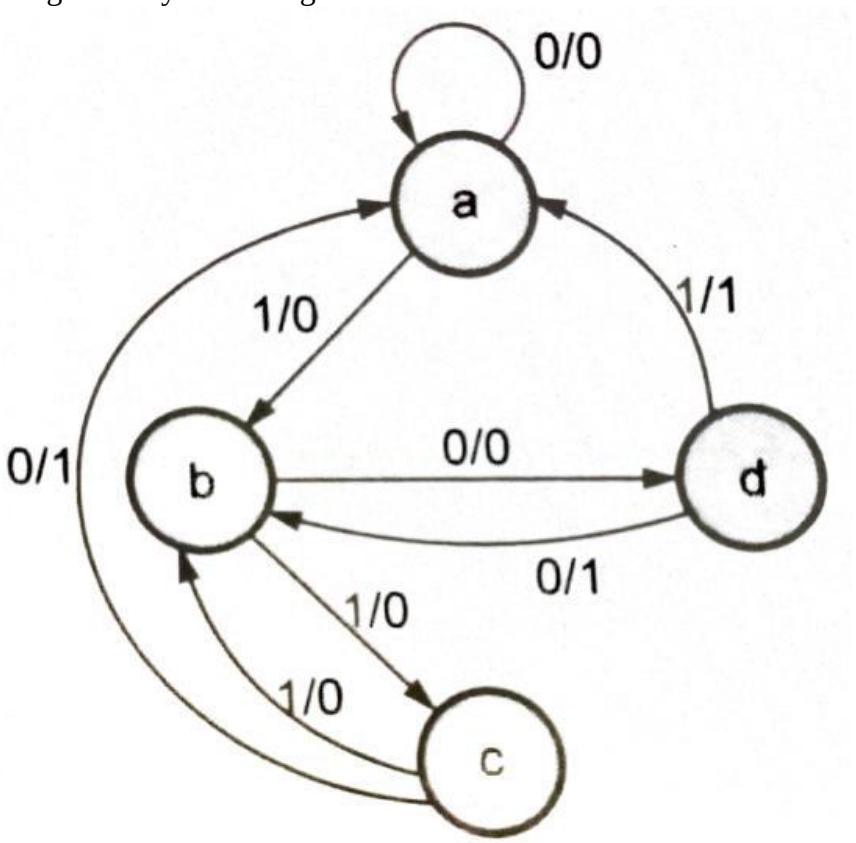
UNIT V
SEQUENTIAL LOGIC CIRCUITS

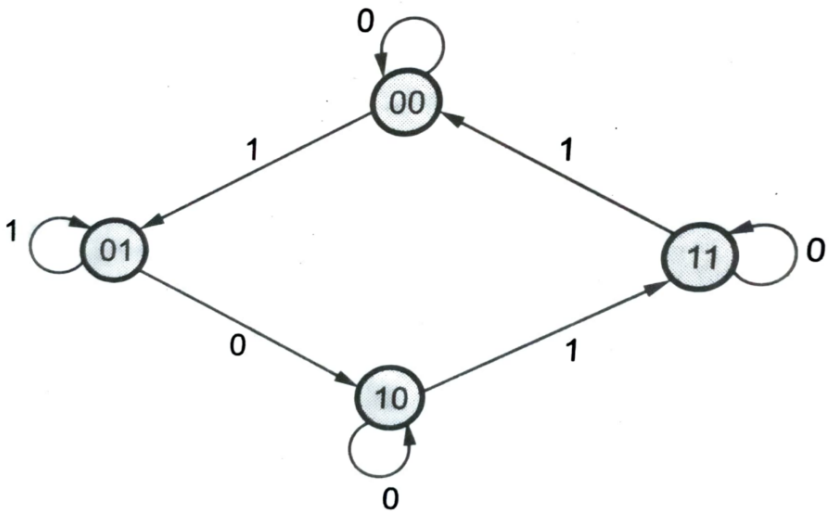
Flip flops – SR, JK, T, D, Master/Slave FF, Triggering of FF, Analysis and design of clocked sequential circuits – state minimization, state assignment, circuit implementation. Counters, Ripple Counters, Ring Counters. Types of Registers, Serial In - Serial Out, Serial In - Parallel out, Parallel In -Serial Out, Parallel In - Parallel Out, Universal Shift Register.

PART - A

Q.	Questions	CO	BT	Competence

No			Level	
1.	List the classification of Sequential circuits.	**CO5**	**BTL 2**	**Understanding**
2.	Compare combinational and sequential circuits.	**CO5**	**BTL 2**	**Understanding**
3.	Define a flip-flop.	**CO5**	**BTL 1**	**Remembering**
4.	List the types of flip-flop.	**CO5**	**BTL 2**	**Understanding**
5.	Differentiate between latch and flip-flop.	**CO5**	**BTL 2**	**Understanding**
6.	Write the excitation table for JK Flip flop.	**CO5**	**BTL 1**	**Remembering**
7.	Draw the state transition diagrams of flip-flops.	**CO5**	**BTL 2**	**Understanding**
8.	Write the characteristic equation from the truth table of SR flip-flop.	**CO5**	**BTL 2**	**Understanding**
9.	Convert D flip-flop to T flip-flop.	**CO5**	**BTL 2**	**Understanding**
10.	Mention any two differences between the edge triggering and level triggering.	**CO5**	**BTL 2**	**Understanding**
11.	Obtain the characteristic equation for D flip-flop.	**CO5**	**BTL 1**	**Remembering**
12.	Interpret the significance of state assignment.	**CO5**	**BTL 1**	**Remembering**
13.	Draw the state diagram of Mod-10 counter.	**CO5**	**BTL 2**	**Understanding**
14.	Sketch the circuit diagram of ring Counter.	**CO5**	**BTL 2**	**Understanding**
15.	Identify the flip-flops required to build a binary counter that counts from 0 to 1023.	**CO5**	**BTL 2**	**Understanding**
16.	Examine the difference between Mealy and Moore state machines.	**CO5**	**BTL 1**	**Remembering**
17.	What is the minimum number of flip-flops needed to design a counter of Modulus 10?	**CO5**	**BTL 1**	**Remembering**
18.	List out the applications of shift registers.	**CO5**	**BTL 2**	**Understanding**
19.	Distinguish between synchronous sequential circuits and asynchronous sequential circuits.	**CO5**	**BTL 2**	**Understanding**
20.	Construct a NAND based logic diagram of JK FF.	**CO5**	**BTL 1**	**Remembering**
21	Define universal shift register.	**CO5**	**BTL 1**	**Remembering**
22	Name the types of shift registers.	**CO5**	**BTL 1**	**Remembering**
23	A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. Compute the Q output.	**CO5**	**BTL 2**	**Understanding**
24	Sketch the 4-bit Johnson counter.	**CO5**	**BTL 2**	**Understanding**
	PART- B			
1.	(i) Define Flip flop? Explain about the operations of different flip flops. (ii) List the applications of Flip flop.	(8) (8)	**CO5**	**BTL 3**	**Applying**
2.	Explain about JK flip-flop with truth table, characteristic equation and input & output waveforms.	(16)	**CO5**	**BTL 3**	**Applying**
3.	Realize SR flip-flop using D flip-flop and JK flip-flop.	(16)	**CO5**	**BTL 3**	**Applying**
4.	(i) Explain the steps for the design of clocked synchronous sequential circuit. (ii) Obtain the reduced state table for the given tabulation.	(8) (8)	**CO5**	**BTL 3**	**Applying**
5.	Describe the functions with the state diagram and characteristics equation of T FF.	(16)	**CO5**	**BTL 3**	**Applying**

6.	Examine a state table, characteristic table and an excitation table for SR Flip Flop.	(16)	**CO5**	**BTL 4**	**Analyzing**
7.	Design a clocked sequential machine using T flip-flops for the following state diagram. Use state reduction if possible. Also use straight binary state assignment. 	(16)	**CO5**	**BTL 4**	**Analyzing**
8.	Analyze the design procedure of a MOD-5 synchronous counter using JK flip-flops and implement it.	(16)	**CO5**	**BTL 3**	**Applying**
9.	With the D flip-flop, design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000.	(16)	**CO5**	**BTL 4**	**Analyzing**
10.	Using SR flip flops, design a counter which counts in the following sequence 000, 111, 1101,100,011,010,001, 000,…..	(16)	**CO5**	**BTL 4**	**Analyzing**
11.	Analyze a counter to count the sequence 0,1,2,4,5,6 using SR FFs.	(16)	**CO5**	**BTL 3**	**Applying**
12.	Implement a J-K counter for the states 3, 4, 6, 7 and 3.	(16)	**CO5**	**BTL 3**	**Applying**
13.	With the neat block diagram explain the operation of universal shift register.	(16)	**CO5**	**BTL 4**	**Analyzing**
14.	Explain in detail about the working of mod-3 counter with neat diagram.	(16)	**CO5**	**BTL 3**	**Applying**
15.	Describe about the operation of 4-bit ring counter with waveforms.	(16)	**CO5**	**BTL 3**	**Applying**
16.	Construct the design of a synchronous decade counter using D flip-flop.	(16)	**CO5**	**BTL 4**	**Analyzing**

17.	Analyze a synchronous sequential circuit using JK Flip-flop for the given state diagram.  	(16)	**CO5**	**BTL 4**	**Analyzing**