SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM NAGAR, KATTANKULATHUR – 603 203.

DEPARTMENT OF MEDICAL ELECTRONICS

LABORATORY MANUAL

MD3465 - ANALOG AND DIGITAL CIRCUITS LABORATORY

Regulation - 2023

Semester/Branch	**:**	**IV semester MDE**
Academic Year	**:**	**2024 - 2025 (EVEN)**
Prepared By	**:**	**Ms. Vanmathi. P, A.P (O.G)**

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SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF MEDICAL ELECTRONICS

VISION OF THE INSTITUTE

Educate to excel in social transformation

MISSION OF THE INSTITUTE

• To contribute to the development of human resources in the form of professional engineers and managers of international excellence and competence with high motivation and dynamism, who besides serving as ideal citizen of our country will contribute substantially to the economic development and advancement in their chosen areas of specialization.
• To build the institution with international repute in education in several areas at several levels with specific emphasis to promote higher education and research through strong institute-industry interaction and consultancy.

VISION OF THE DEPARTMENT

To develop an excellent progressive quality education, translational research through inventive collaborations as per industry requirements to improve the healthcare and well-being of humankind.

MISSION OF THE DEPARTMENT

M1: To Acquaint students with the current technology to provide consultations and technical support to hospitals, healthcare and service sectors.
M2: To educate students with the fundamental knowledge, interdisciplinary problem solving skills and confidence required to excel in medical electronics through progressive learning.
M3: To propagate creativity, responsibility, commitment and leadership qualities and exhibit professional ethics and values.

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PROGRAM OUTCOMES

1.Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2.Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3.Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4.Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5.Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.
6.The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7.Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8.Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9.Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10.Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11.Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12.Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOME(PSOs)

PSO1: Ability to apply the acquired knowledge of basic skills, mathematical foundations, principles of electronics, modelling and design of electronics based systems in solving engineering Problems.
PSO2: Ability to understand and analyze the interdisciplinary problems for developing innovative sustained solutions with environmental concerns.
PSO3: Ability to update knowledge continuously in the tools like MATLAB, NS2, XILINIX and technologies like VLSI, Embedded, Wireless Communications to meet the industry requirements.
PSO4: Ability to manage effectively as part of a team with professional behaviour and ethics.

SYLLABUS

MD3465 ANALOG AND DIGITAL INTEGRATED CIRCUITS LABORATORY

L T P C 0 0 3 1.5

OBJECTIVES:

• To study the characteristics of inverting, non-inverting, and instrumentation amplifier.

• To learn the linear and non-linear applications of operational amplifiers.

• To identify the combinational circuits and design procedures.

• To understand the function of sequential circuits.

• To exhibit the student in simulating analog circuits.

LIST OF EXPERIMENTS:

1. Design of inverting and non-inverting amplifier.

2. Design of Integrator and Differentiator.

3. Design of Instrumentation amplifier.

4. Design of Active low pass, High pass filter and Band pass filter

5. Design of Astable and Monostable multivibrator using 555 timer.

6. Design of RC Phase shift and Wien bridge oscillators using op-amp.

7. Design of Schmitt Trigger using op-amp.

8. Study of logic gates, Half adder and Full adder.

9. Design and implementation of multiplexer and demultiplexer.

10. Design and implementation of encoder and decoder using logic gates.

11. Design and implementation of shift registers.

12. Design and implementation of mod-N counter.

13. Simulation and analysis of circuits using software (any open access).

TOTAL PERIODS: 45

COURSE OUTCOMES:

On completion of the course, student will be able to
CO1: Learn and design amplifiers using op-amp.
CO2: Explore the filters and multivibrators.
CO3: Analyze the performance of combinational circuits.
CO4: Design and test the performance of sequential circuits.
CO5: Simulate and analyse amplifier circuits using software.

LIST OF EXPERIMENTS

CYCLE-I
ANALOG EXPERIMENTS

1. Design of inverting and non-inverting amplifier.

2. Design of Integrator and Differentiator.

3. Design of Instrumentation amplifier.

4. Design of Active low pass, High pass filter and Band pass filter

5. Design of Astable and Monostable multivibrator using 555 timer.

6. Design of RC Phase shift and Wien bridge oscillators using op-amp.

7. Design of Schmitt Trigger using op-amp.

CYCLE-II
DIGITAL EXPERIMENTS

8. Study of logic gates, Half adder and Full adder.

9. Design and implementation of multiplexer and demultiplexer.

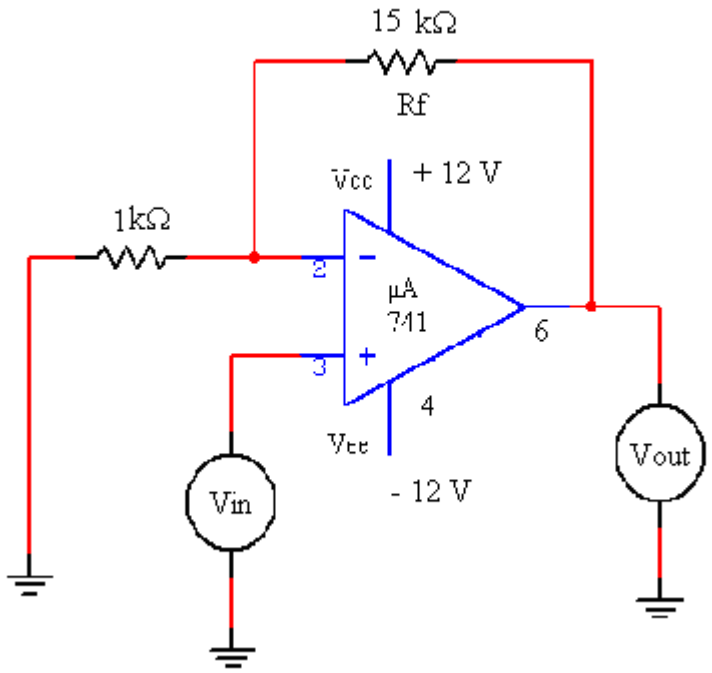
10. Design and implementation of encoder and decoder using logic gates.

11. Design and implementation of shift registers.

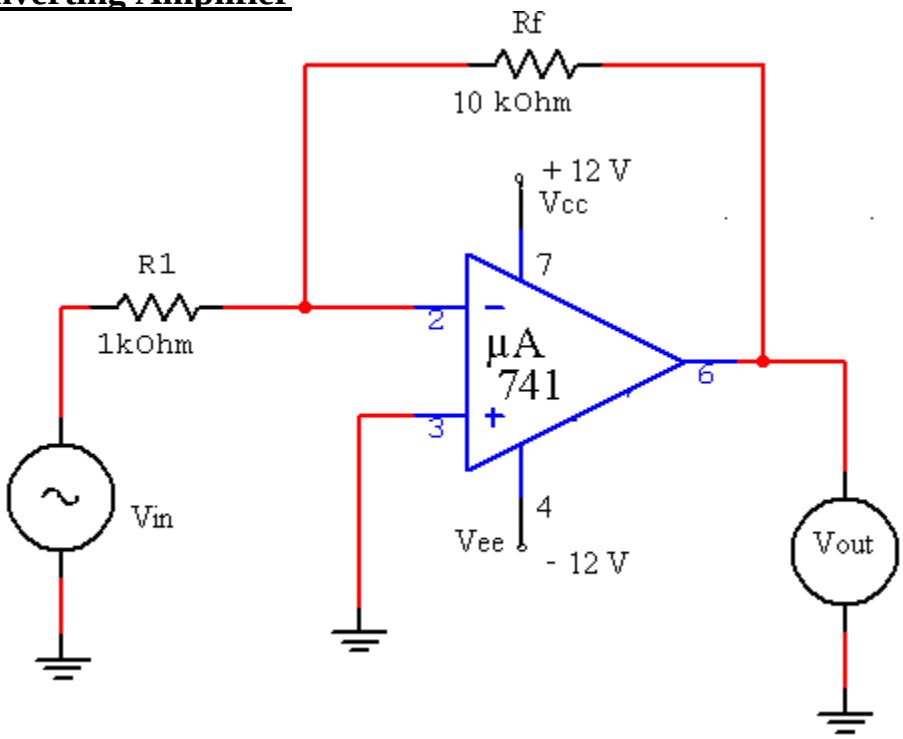
12. Design and implementation of mod-N counter.

13. Simulation and analysis of circuits using software (any open access).

Non Inverting Amplifier



Inverting Amplifier



Ex.No:1 **INVERTING AND NON-INVERTING AMPLIFIER**

Preparatory Exercise:

1. What is an op-amp? Why it is called so?
2. Define the term input offset voltage, input bias current, gain bandwidth product.
3. Define slew rate in an op-amp.
4. List the ideal characteristics of an op-amp.
5. List the linear and non-linear applications of an op-amp.

AIM:

To design a Inverting amplifier and Non-Inverting amplifier using an op-amp

i) Non-Inverting amplifier with a gain of 11.

ii) Inverting amplifier with a gain of -10.

DESCRIPTION

Inverting amplifier:

Input : Sinusoidal signal of 1Vp-p at 1 KHz

Output: Inverted Sinusoidal signal of 10 Vp-p at 1 KHz

Non Inverting Amplifier

Input : Sinusoidal signal of 1Vp-p at 1 KHz

Output: Sinusoidal signal of 16 Vp-p at 1 KHz

APPARATUS REQUIRED:

S.No	COMPONENTS	RANGE	QUANTITY
1	IC – 741	---	1
2	Resistors	10KΩ,15KΩ,100KΩ,1KΩ	2
3	AFG	(0-1MHz)	1
4	CRO	20MHz	1

FORMULA:

Inverting amplifier **:** Output voltage V_O = -Rf/R1 Vin

Non – Inverting amplifier : Output voltage Vo = (1+Rf/R1) Vin

DESIGN :

Inverting Amplifier

Gain Av = - (Rf/R1)

Given Av = -10

-10 = - (Rf/R1)

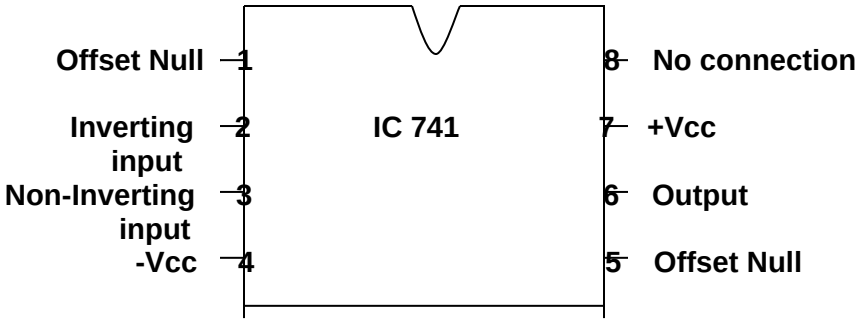
Thus,

Rf= 10 R1

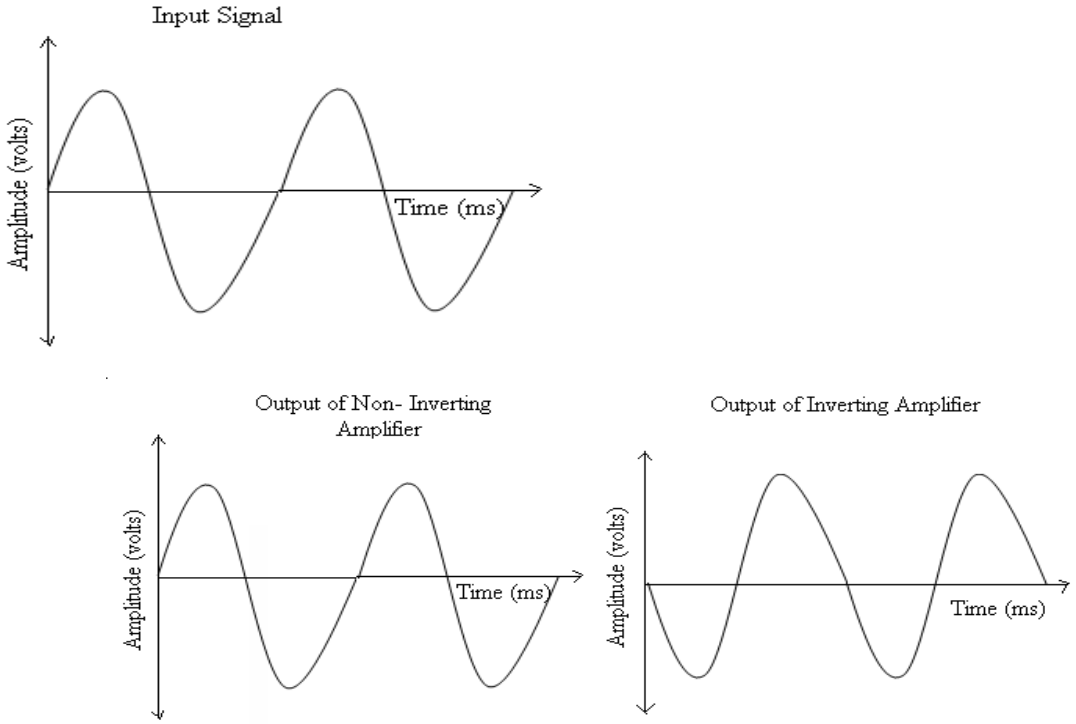
Let R1 = 1kΩ

Then Rf=10kΩ

PIN DIAGRAM:



Model Graph



Tabulation

Experiment	Amplitude (volts)		Time (ms)		Gain =Vo/Vin	
	Input	Output	Input	Output	Theoretical	Practical
Inverting Amplifier						
Non-Inverting Amplifier						

Non inverting Amplifier

Gain Av = 1+ Rf/R1

Given Gain Av=11

11 = 1+ Rf/R1

Rf/R1 = 10

Thus,

Rf = 10 R1

Let R1 =1KΩ

Then Rf = 10 KΩ

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Set the input voltage and note the output waveform at pin number 6 for the inverting and non-inverting amplifiers.
3. From the input and output values calculate the gain of the amplifiers and verify with the theoretical gain value of the amplifiers.
4. Use linear graph to plot the input and output waveforms.

THEORY:

INVERTING AMPLIFIER

This is used in application where output signal is 180^0 out of phase with input signal. It is a current voltage converter driven by a voltage source instead of a current source. The feedback resistance Re. A closed loop cut off gain because of negative feedback. The negative feedback also stabilizes the voltage gain and input impedance. This also decreases distortion and offset voltage.

NON INVERTING AMPLIFIER

This is approximately and ideal voltage amplifier, because of high input impedance, low output impedance, stable voltage gain. This produces output voltage which is in phase with input voltage as with it is the requirement for much application.

RESULT:

Thus the Inverting amplifier and Non – Inverting Amplifier are designed and output is verified for the given specification.

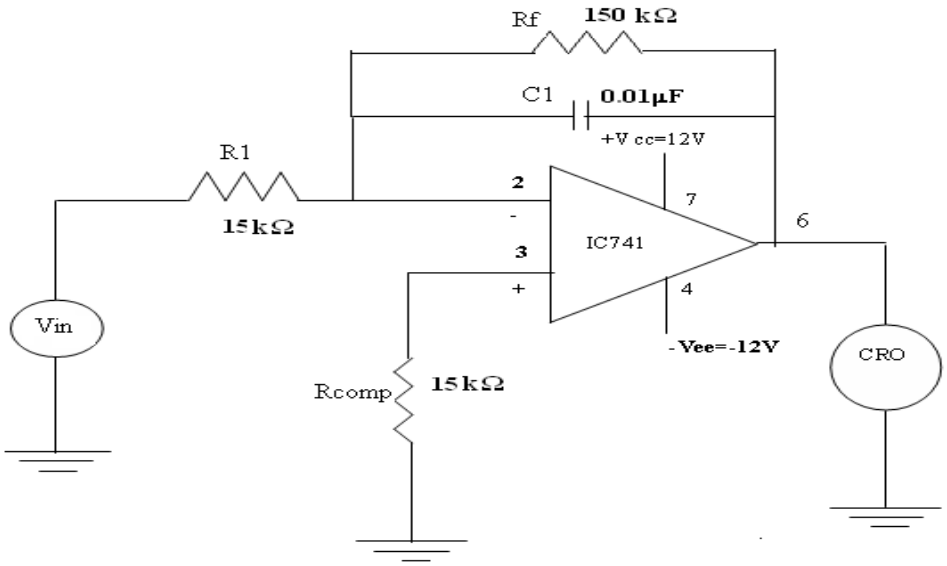
Common Mode Rejection Ratio (CMRR) =

Review Questions:

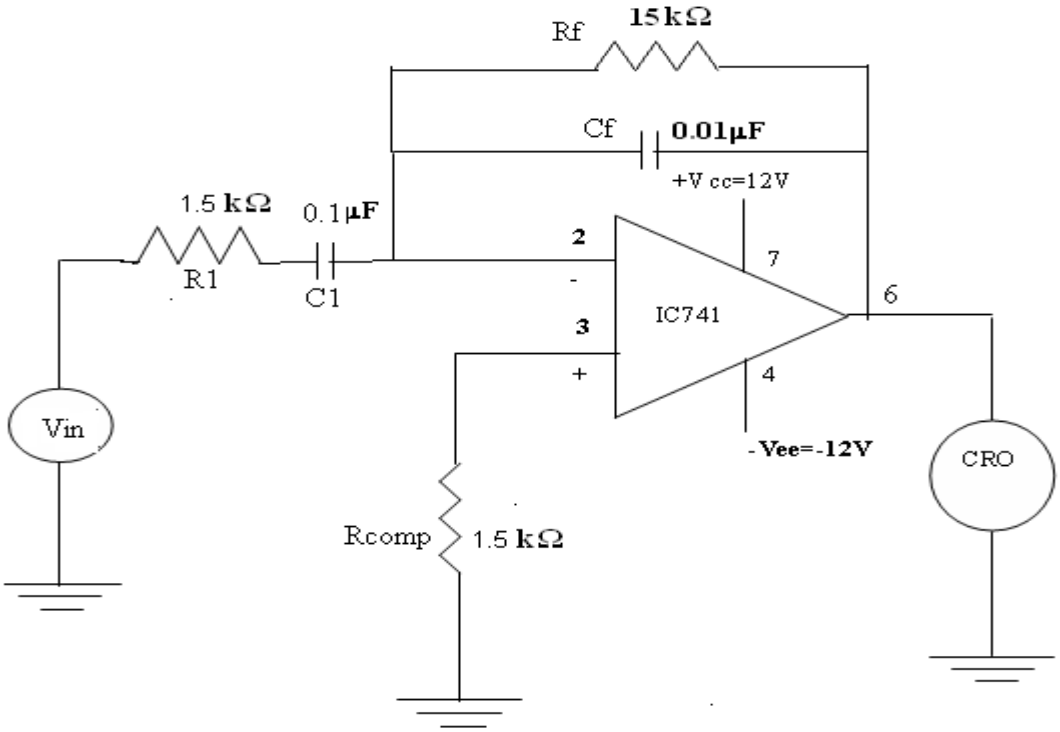
1. How will be the output of an inverting amplifier compared to the input signal?
2. What is a sign changer and a scale changer circuit?
3. When do we call an inverting amplifier as a phase inverter?
4. What is CMRR?

CIRCUIT DIAGRAM:

INTEGRATOR



DIFFERENTIATOR



EX.No:2 INTEGRATOR AND DIFFERENTIATOR

Preparatory Exercise:

1. What is an op-amp? Why it is called so?
2. List the ideal characteristics of an op-amp.
3. What are the building blocks of an op-amp?
4. What are the limitations of an ideal integrator circuit using an op-amp?

AIM:

Design and implement the following

1) Practical integrator circuit with the gain of 10 to integrate a square wave of 1 KHz
2) Practical differentiator for 1 V Peak at 1000Hz is applied as a input

DESCRIPTION

Integrator:

Input : Square input of 1Vp-p at 1 KHz
Output : Inverted Triangular signal of 10 Vp-p at 1 KHz.
Refinement : At low frequency gain becomes infinite to avoid the saturation problem a resistor is connected in shunt to the feedback capacitor. For the sine input, output will be a negative cosine signal

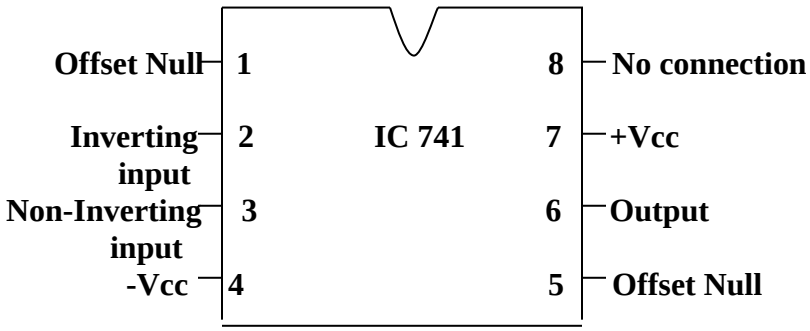
Differentiator:

Input : Square input of 1Vp-p at 1000Hz
Output : Spike signal of 2 Vp-p.
Refinement : At high frequency circuit becomes sensitive to noise as the input impedance decreases with the increase in frequency. Thus to eliminate the unstability of the circuit, feedback circuit can be connected. For the sine input, output will be a cosine signal

APPARATUS REQUIRED:

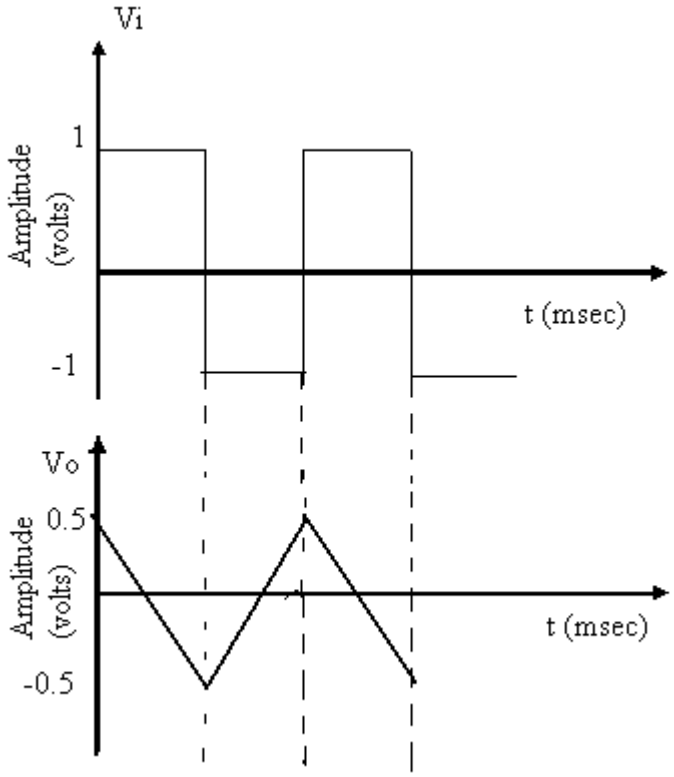
APPARATUS NAME	RANGE	QUANTITY
AFG		1
CRO		1
Resistors	1K, 15.9k, 10K, 100k, 1.59k	1
Capacitors	0.01μF, 0.1 μF, 1.6μF	1
Op-Amp	IC741	
Bread Board		1
RPS		1

PIN DIAGRAM



MODEL GRAPH:

INTEGRATOR



DESIGN:

INTEGRATOR

A= 10

$R_f/R_1 = 10$

$R_f = 10\ R_1$

Assume $R_1 = 15k\Omega$

$R_f = 150\ k\Omega$

$f= 10\ f_a$

f = 1kHz Given

$f_a = 1k\Omega$

$f_a = 1/ (2\pi R_f\ C_f)$

$C_f = 1/2\pi R_f f_a)$

Let $C_f = 0.01\mu F$

$Rcomp= R_1R_f /(R_1+R_f)=13.6\ k\Omega$

DIFFERENTIATOR

$\mathbf{f}_a = f_{max} = 100Hz$

$=1/(2\pi R_fC_1)$

Assume $C_1 = 0.1\mu F$

$R_f = 1/(2\pi C_1f_a)$

$R_f = 15.9\ k\Omega$

Let $R_f = 15\ K\Omega$, Choose $f_b = 10f_a = 1kHz = 1/(2\pi R_1C_1)$

$R_1 = 1/(2\pi f_bC_1)$

$R_1 = 1.5\ k\Omega$

$R_f\ C_f = R_1C_1$

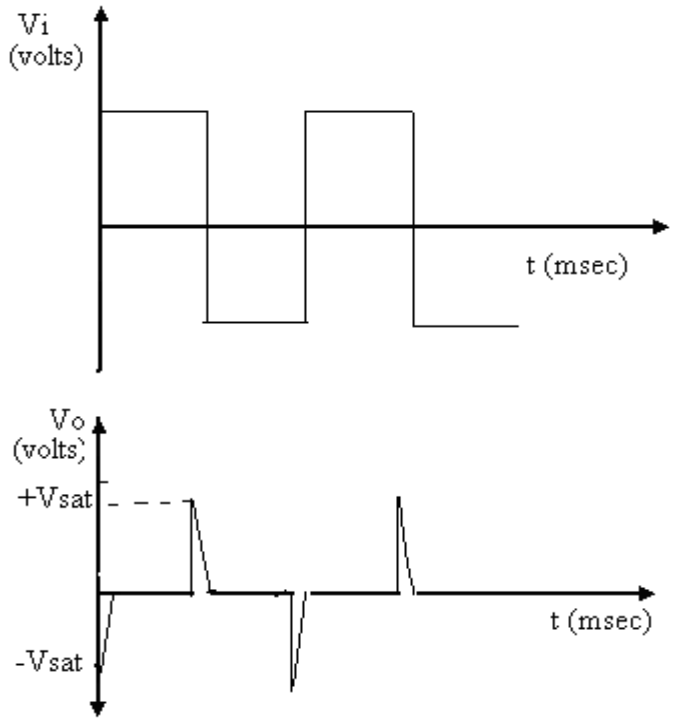
$C_f= R_1C_1/ R_f$

Let Cf= 0.01μF

$Rcomp= R_1R_f/(R_1+R_f)=1.5k\Omega$

MODEL GRAPH:

DIFFERENTIATOR



OBSERVATIONS

Name of the Circuit	Waveform	Amplitude(volts)	Time (ms)
Integrator	Input –Sine wave		
	Output –Cosine wave		
	Input – Square wave		
	Output - Triangular wave		
Differentiator	Input –Sine wave		
	Output –Cosine wave		
	Input – Square wave		
	Output - Spike		

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. The resistance R_{comp} is also connected to the (+) input terminal to minimize the effect of the input bias circuit.
3. It is noted that the gain of the integrator decreases with increasing frequency.
4. Thus the integrator circuit does not have any high frequency problem.

THEORY:

INTEGRATOR

A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However in the op-amp integrator by MILLER's theorem, the effective input capacitance becomes C_f $(1-A_v)$, where A_v is the gain of the op-amp. The gain A_v is the infinite for an ideal op-amp, so the effective time constant of the Op-amp integrator becomes very large which results perfect integration.

DIFFERENTIATOR

A simple high pass RC circuit can also work as an integrator when time constant is very large. The output voltage Vo is a constant $(-R_fC_1)$ times the derivative of the input voltage V_i. The minus sign indicates a 180º phase shift of the output waveform Vo with respect to the input sign. At high frequency, the differentiator may become unstable and break into oscillation. The input impedance $(1/\omega C_1)$ decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. This drawback can be overcome by using practical differentiator circuit.

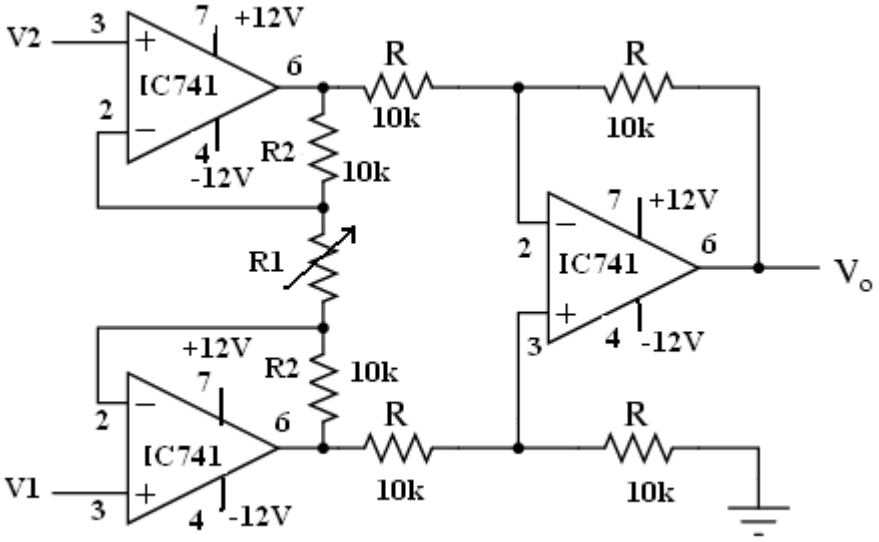
RESULT:

Thus the integrator and differentiator using op-amp has been designed and the output waveforms are observed and verified.

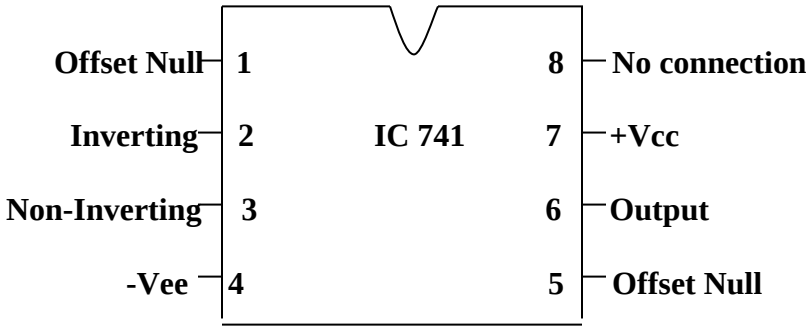
Review Questions:

1. What are the limitations of an ideal differentiator circuit using an op-amp?
2. Can we use integrator as a filter?
3. Can we use differentiator as a filter?

INSTRUMENTATION AMPLIFIER



PIN DIAGRAM



Ex.No. 3: INSTRUMENTATION AMPLIFIER

Preparatory Exercise:

1. What is an op-amp? Why it is called so?
2. Define the term input offset voltage, input bias current, gain bandwidth product.
3. Define slew rate in an op-amp.
4. List the ideal characteristics of an op-amp.
5. What are the building blocks of an op-amp?

AIM:

To study the operation and the varying gain range of an instrumentation amplifier.

DESCRIPTION

Input : Set the dc input voltage in both the input terminals V1 and V2.
Output : Vary the resistor R1 to obtain the output voltage with varying gain

APPARATUS REQUIRED*:*

S.NO	ITEM	RANGE	QUANTITY
1	Op-amp	IC741	1
2	Resistors	10kΩ	6
3	Decade Resistance box	-	1
4	Multimeter	-	1
5	RPS	DUAL(0-30) V	2

DESIGN:

Assume the resistors in the differential amplifier stage to be of the same value R =10kΩ

Using Superposition theorem the output of the Instrumentation amplifier is

$V_o = -(R/R)V_a + (1+R/R)V_b = V_b - V_a$

Where $V_a = -R2/R1(V1-V2) + V2$

and $V_b = R2/R1(V1-V2)+V1$

Thus $V_o = V_b - V_a = (V1-V2)(1+2R2/R1)$

Gain of an Instrumentation amplifier is

$Av = V_o/(V1-V2) = (1+2R2/R1)$

For $Av = 3$

$3=(1+2R2/R1)$

Then $R2 = R1$

Let R2 = 10kΩ then set the variable resistor R1 = 10kΩ

OBSERVATIONS:

V1 (Volts)	V1 (Volts)	R1 (Ohms)	Vo (Volts)	Gain	
				Theoretical 1+2R2/R1	Practical V0/V1-V2

Thus the gain of the instrumentation amplifier can be varied over a range of 1.5 to 1.2 by varying the variable resistance R1 from 20K to 50K.

PROCEDURE:

1. Connect the components as per the circuit diagram.
2. Initially set the variable resistor R1 to the minimum value and note down the output voltage and compute the gain.
3. Repeat the procedure in step 2 for various values of R1 and note down the corresponding output voltage to find the range of gain.

THEORY:

Instrumentation Amplifiers are high gain differential amplifiers with high input impedance and a single ended output. They are mainly used to amplify very small differential signals from strain gauges, thermocouples or current sensing resistors in motor control systems. They also have very good common mode rejection in excess of 100dB at DC. The negative feedback of the top op-amp causes the voltage at Va to be equal to the input voltage V1. Likewise, the voltage at Vb is equal to the value of V2. This produces a voltage drop across R1 which is equal to the voltage difference between V1 and V2. This voltage drop causes a current to flow through R1, and as the two inputs of the buffer op-amps draw no current (virtual earth), the same amount of current flowing through R1 must also be flowing through the two resistors R2. This voltage drop between points Va and Vb is connected to the inputs of the differential amplifier which amplifies it by a gain of 1 (assuming that all the "R" resistors are of equal value). Then the overall voltage gain of the instrumentation amplifier circuit is

$$V_{out} = (V_1 - V_2)\left[1 + \frac{2R_2}{R_1}\right]$$

The differential gain of the circuit can be changed by changing the value of R1.

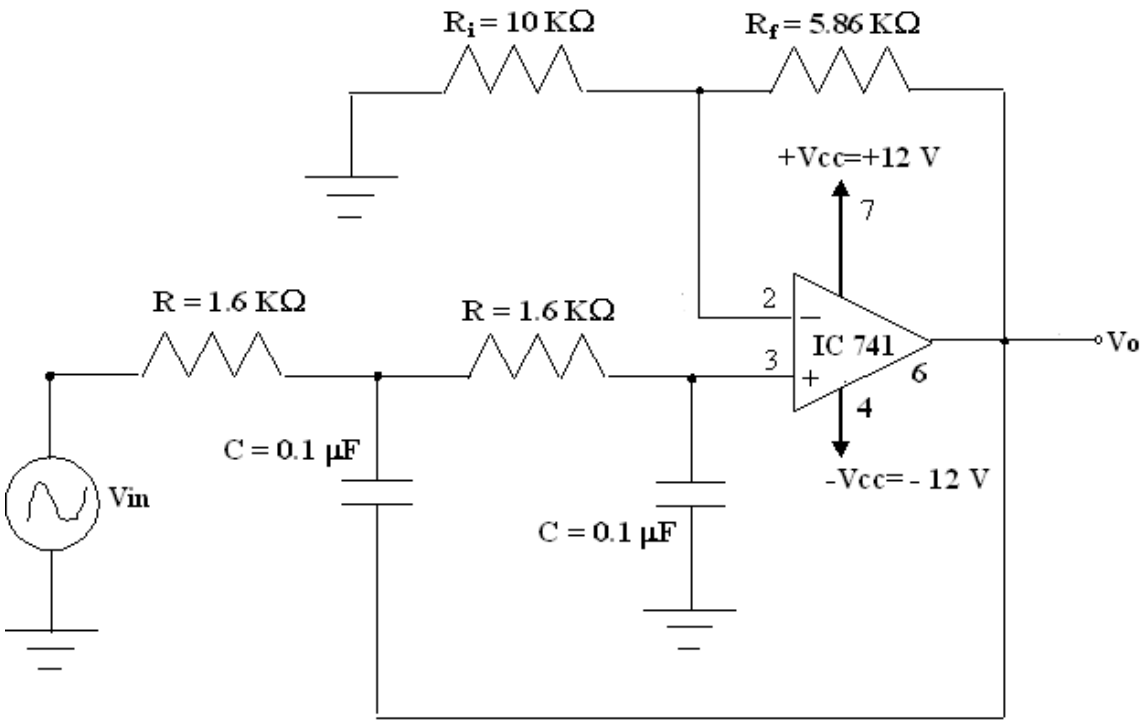
RESULT:

Thus by varying the variable resistor R1 a wide range of gain can be obtained from the instrumentation amplifier.

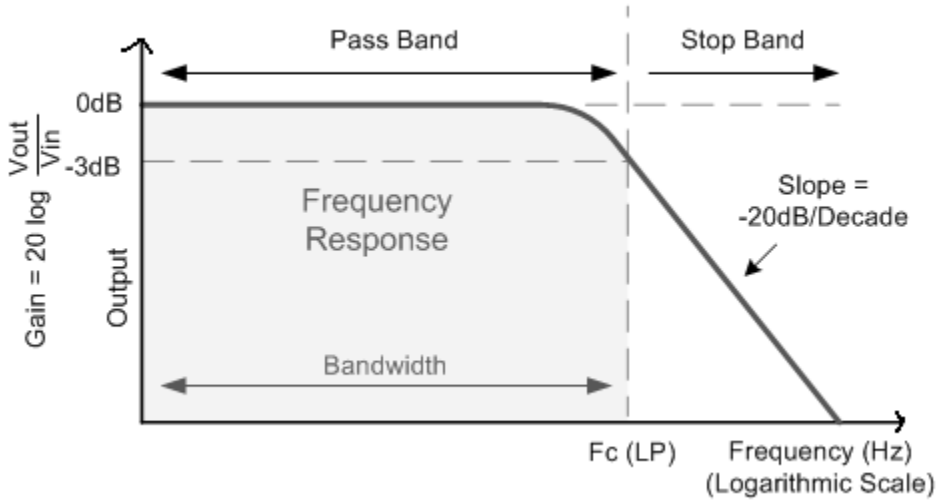
Review Questions:

1. What are the advantages of negative feedback in an op-amp?
2. List the linear and non-linear applications of an op-amp.
3. What is an instrumentation amplifier?
4. List some applications of an instrumentation amplifier.

CIRCUIT DIAGRAM:



Frequency Response Characteristics: (Use Semi – log Graph):



Ex. No. 4: SECOND ORDER ACTIVE LOW PASS FILTER & ACTIVE WIDE BAND PASS FILTER

Preparatory Exercise:

1. What is an op-amp? Why it is called so?
2. List the ideal characteristics of an op-amp.
3. What are the building blocks of an op-amp?
4. What is an electric filter?
5. State the advantages of an active filter.

Preparatory Exercise:

AIM:

Design a second order active Butterworth low pass filter using IC 741 having upper cut-off frequency 1 KHz, also determine its frequency response and Design a second order active band pass pass filter using IC 741.

DESCRIPTION

Input : Sinusoidal signal input of 4Vp-p, varying from 100Hz to 10 kHz.
Output : Output voltage remains constant with a gain of 4 is obtained in the frequency range of 100Hz to 600Hz approximately. Beyond this range gain decreases with a roll off rate 20dB/decade.

APPARATUS REQUIRED*:*

S.NO	ITEM	RANGE	QUANTITY
1	Op-amp	IC741	1
2	Resistors	10KΩ,1.5KΩ,5.6 KΩ	1
3	Capacitor	0.1 μF	1
4	CRO	-	1
5	RPS	DUAL(0-30) V	1

DESIGN:

Given:

Upper cut-off frequency f_H = 1 kHz

$$f_H = 1/ (2\pi RC)$$

Let C = 0.1 μF, R = 1.6 KΩ

For n = 2, α (damping factor) = 1.414,

Passband gain = $A_o = 3 - \alpha = 3 - 1.414 = 1.586$.

Transfer function of second order Butterworth Low-pass filter is:

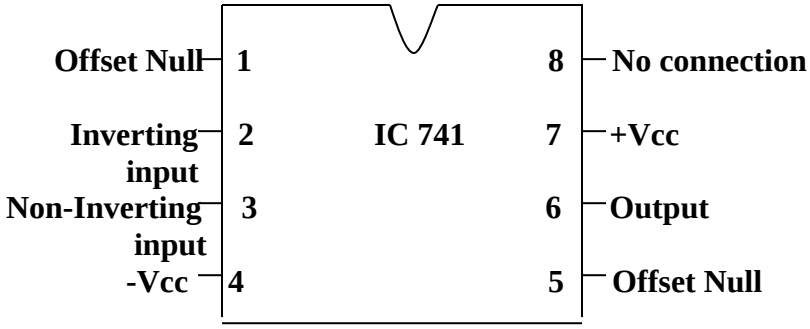
$$H(s) = \frac{1.586}{S^2 + 1.414\, s + 1}$$

Now $A_o = 1 + (R_f / R_1) = 1.586$

Thus, $R_f = 0.586 R_i$

Let R_i = 10 kΩ, then R_f = 5.86 kΩ

PIN DIAGRAM



OBSERVATION:

V_{IN} = 1 Volts

S.No.	Frequency (Hz)	Output Voltage V_O (Volts)	Voltage Gain Av=20 log Vo/Vi (dB)

THEORY:

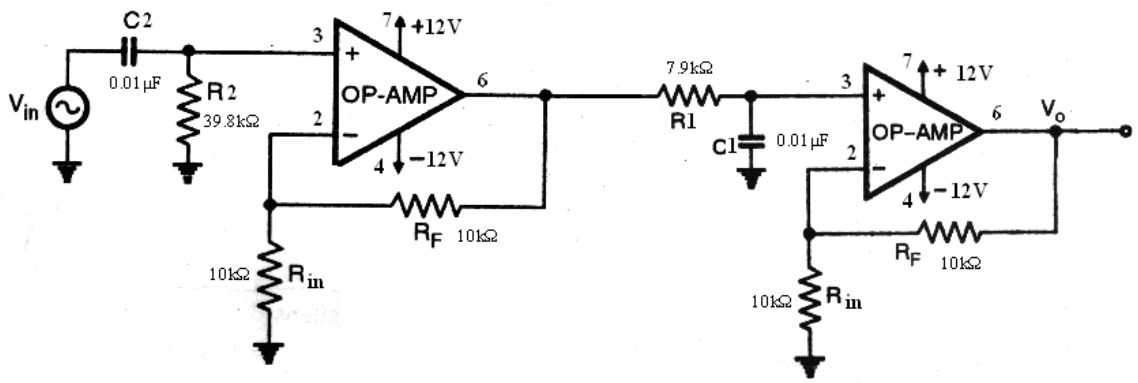
A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter An improved filter response can be obtained by using a second order active filter. A second order filter consists of two RC pairs and has a roll-off rate of -40 dB/decade. A general second order filter (Sallen Kay filter) is used to analyze different LP, HP, BP and BSF.

PROCEDURE :

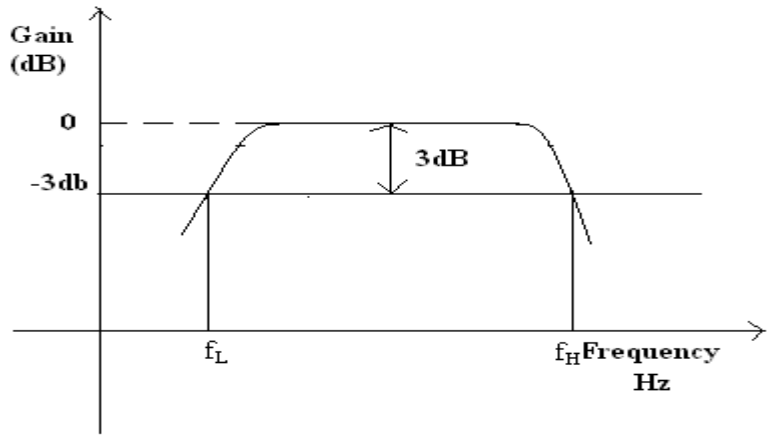
1. The connections are made as shown in the circuit diagram.
2. The sinusoidal signal is applied as an input to the RC filter pair circuit to the non-inverting terminal with an amplitude of 4Vp-p and 100Hz.
3. The supply voltage is switched ON and the output voltages are noted using CRO by varying the frequencies from 100Hz to 10 KHz and tabulate the readings.
4. Calculate the voltage Gain using the formula and plot the frequency response characteristics using Semi-log graph sheet and determine the cut-off frequency by drawing -3 dB line in the graph.

CIRCUIT DIAGRAM

BAND PASS FILTER



Frequency Response Characteristics: (Use Semi – log Graph):



WIDE BAND ACTIVE BAND PASS FILTER

DESCRIPTION

Input : Sinusoidal signal input of 4Vp-p, varying from 100Hz to 10 kHz.
Output : Output voltage remains constant with a gain of 4 is obtained in the frequency range of 100Hz to 600Hz approximately. Beyond this range gain decreases with a roll off rate 20dB/decade.

APPARATUS REQUIRED*:*

S.No.	ITEM	RANGE	QUANTITY
1	Op-amp	IC741	2
2	Resistors	10kΩ,7.9kΩ,39.8kΩ	1
3	Capacitor	0.01 μF	2
4	CRO	-	1
5	RPS	DUAL(0-30) V	1
6	Function Generator	-	1

DESIGN:

Given:
Cut-off frequency of High pass filter section f_L = 400 Hz
Cut-off frequency of Low pass filter section f_H = 2kHz

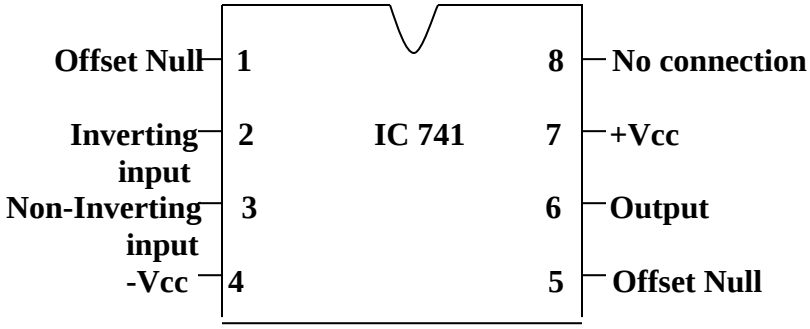
$$f_L = 1/ (2\pi R_2 C_2)$$
$$f_H = 1/ (2\pi R_1 C_1)$$

Let , $R_f = R_i$ = 10kΩ for both LPF and HPF section
For **LPF** , f_H = 2kHz = $1/ (2\pi R_1 C_1)$
Let C_1= 0.01 μF, R_1 = 7.9kΩ
For **HPF** , f_L = 400 Hz = $1/ (2\pi R_2 C_2)$
Let C_2= 0.01 μF, R_2 = 39.8kΩ

For a wideband band pass filter Quality factor Q< 10
Q = fo/BW

Where Center frequency $f_o = \sqrt{f_H f_L}$ = 894.4 and
Bandwidth BW = $f_H - f_L$ = 1600
Quality factor Q = 0.56 < 10

PIN DIAGRAM



OBSERVATION:

V_{IN} = 4 Volts

S.No.	Frequency (Hz)	Output Voltage V_O (Volts)	Voltage Gain Av=20 log Vo/Vi (dB)

THEORY:

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter .A wide band-pass filter can be formed by cascading a HPF and LPF section. If the HPF and LPF are of the first order, then the band pass filter will have a roll-off rate of -20dB /decade. The range of frequencies lying between the lower and upper cut-off frequencies is the pass band for the BPF. The BPF is classified based on the Quality factor.(i) Narrow band filter Q>10 (ii) Wide band filter Q <10.

PROCEDURE :

1. The connections are made as shown in the circuit diagram.
2. The sinusoidal signal is applied as an input to the RC filter pair circuit to the non-inverting terminal with an amplitude of 4Vp-p and 100Hz.
3. The supply voltage is switched ON and the output voltages are noted using CRO by

varying the frequencies from 100Hz to 10 KHz and tabulate the readings.

4. Calculate the voltage Gain using the formula and plot the frequency response characteristics using Semi-log graph sheet and determine the cut-off frequency by drawing -3 dB line in the graph.

RESULT:

Thus the second order Active Low Pass filter is designed and its frequency response characteristic curves are drawn.

Theoretical cut-off frequency =
Practical cut-off frequency =

Thus the wide band pass filter is designed and its frequency response characteristic curves are drawn.

Theoretical lower cut-off frequency and upper cut –off frequency:

f_L = f_H=

Practical lower cut-off frequency and upper cut –off frequency

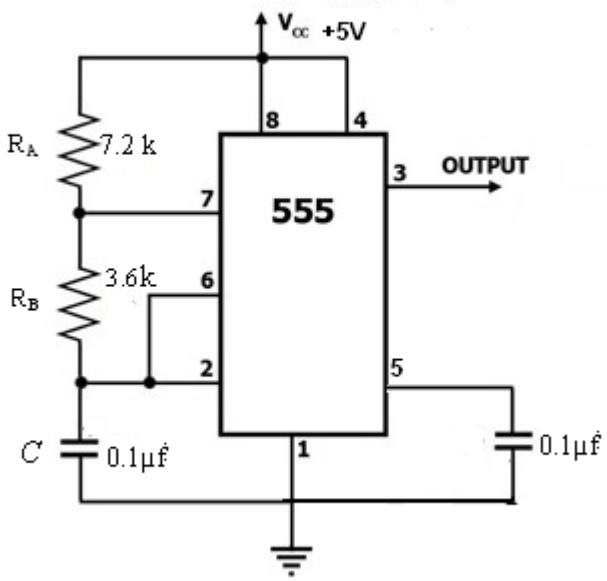
f_L = f_H=

Review Questions :

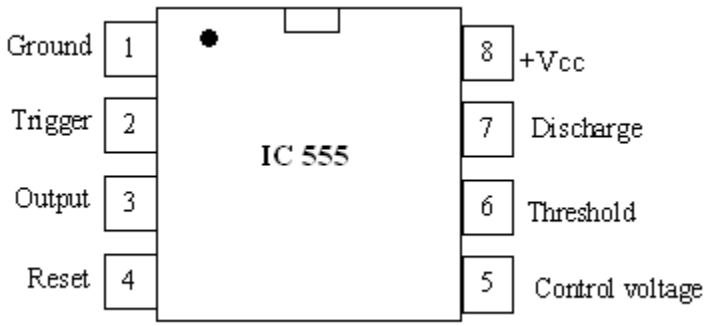
1. What is passband and stopband in frequency response of an op-amp?
2. Why -3dB line is drawn to determine the cut-off frequency?
3. What is Sallen –key filter?
4. What is a low pass filter?
5. How do you classify band pass filter as narrow band or as a wide band?

CIRCUIT DIAGRAM

ASTABLE MULTIVIBRATOR



PIN DIAGRAM



Ex.No.5 ASTABLE & MONOSTABLE MULTIVIBRATOR USING 555 TIMER

Preparatory Exercise:

1. What is a Multivibrator?
2. What is a Timer IC?
3. Differentiate amplifier and IC.

AIM:

Design and implement the Astable multivibrator using 555 timer to generate a signal of frequency of 1 KHz and duty cycle D = 75%

Design and implement the Monostable multivibrator to generate a pulse width of *1 ms* by using 555 timer**.**

DESCRIPTION

Input : Input is not required

Outpur: Rectangular wave output is obtained at pin no. 3 with T_{ON} 0.75ms and T_{OFF} 0.25ms and magnitude is ±Vsat. At pin no.6 across capacitor charging and discharging voltage oscillating between 1/3 Vcc to 2/3 Vcc is noted.

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	7.2kKΩ,3.6 KΩ	Each 1
3	CAPACITOR	0.01μF, 0.1μF	Each 1
4	RPS	(0-30) V	1
5	CRO	-	1

DESIGN :

f = $1.44/(R_A+2R_B)C$

D = $T_{ON}/T = R_A+R_B/(R_A+2R_B)$

Assume C = 0.1μf

f = $1.44/(R_A+2R_B)C$, Given f = 1kHz

1kHz = $1.44/(R_A+2R_B)0.1$ μf

R_A+2R_B =14400 ----------1

D = $T_{ON}/T = R_A+R_B/(R_A+2R_B)$

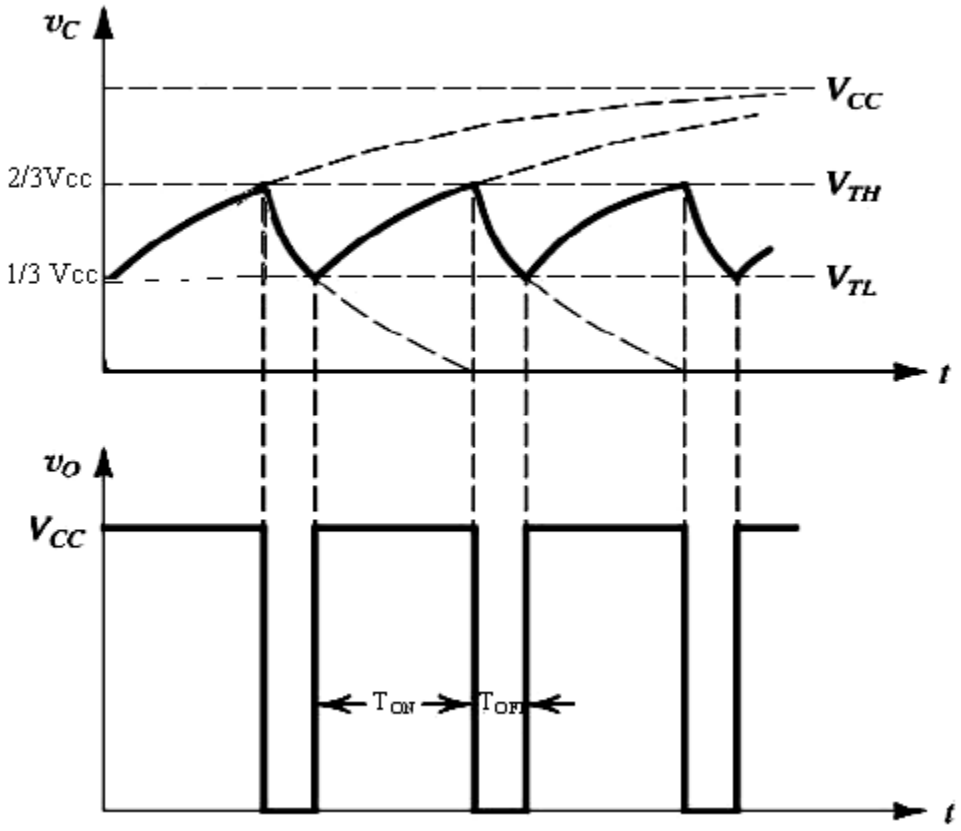
0.75 = $R_A+R_B/(R_A+2R_B)$

R_B = 0.5 R_A----------2

Substitute eqn (2) in eqn (1) $R_A + 2(0.5R_A) = 14400$

Then $R_A = 7.2\ k\Omega$ $R_B = 0.5\ R_A$, $R_B = 3.6\ k\Omega$

MODEL GRAPH



OBSERVATION

Amplitude = (volts)

T_{ON} = (msec)

T_{OFF} = (msec)

Time period $= T_{ON} + T_{OFF} =$ (msec)

PROCEDURE:

1. The connections are made as per the diagram.

2. The output of the astable multivibrator I at pin 3 is measured and its frequency is verified with the theoretical frequency.
3. For monostable multivibrator the trigger input is given
4. The output is observed at pin 3 and across capacitor.
5. The theoretical frequency is verified with the practical.
6. This experiment can be repeated for various values of c for different frequency
7. Plot the output graphs.

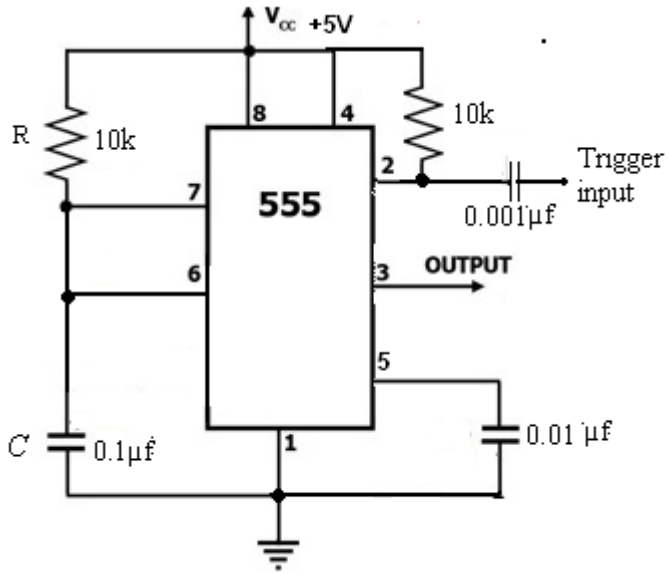
THEORY:

The IC555 timer is a 8 pin IC that can be connected to external components for astable operation. The simplified block diagram is drawn. The OP-AMP has threshold and control inputs. Whenever the threshold voltage exceeds the control voltage, the high output from the OP –AMP will set the flip-flop. The collector of discharge transistor goes to pin 7. When this pin is connected to an external trimming capacitor, a high Q output from the flip flop will saturate the transistor and discharge the capacitor. When Q is low the transistor opens and the capacitor charges.

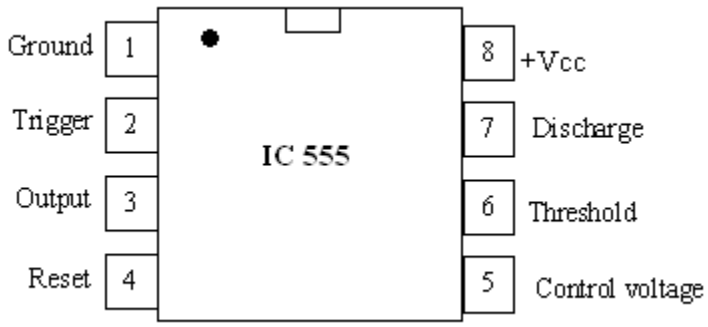
The complementary signal out of the flip-flop goes to pin 3 and output. When external reset pin is grounded it inhibits the device. The on – off feature is useful in many application. The lower OP- AMP inverting terminal input is called the trigger because of the voltage divider. The non-inverting input has a voltage of +Vcc/3; the OP-Amp output goes high and resets the flip flop.

CIRCUIT DIAGRAM:

MONOSTABLE MULTIVIBRATOR



PIN DIAGRAM:



DESCRIPTION

Input : Apply the trigger input of 10 kHz, 2V to pin no. 2.The frequency of triggering should be greater than width of T_{ON} period.

Output : At pin number 6 the output is Pulse wave at 1Hkz and magnitude is Vsat

At pin no.6 ie across the capacitor it is a charging and discharging voltage (triangular vave) with the magnitude of ± BVsat

APPARATUS REQUIRED:

S.NO	ITEM	RANGE	Q.TY
1	IC	NE555	1
2	RESISTOR	10KΩ	2
3	CAPACITOR	0.01μF,0.001uF 0.1μF	1 1
4	RPS	(0-30) V	1
5	DIODE	1N4007	1
5	CRO	-	1

DESIGN :

T = 1ms

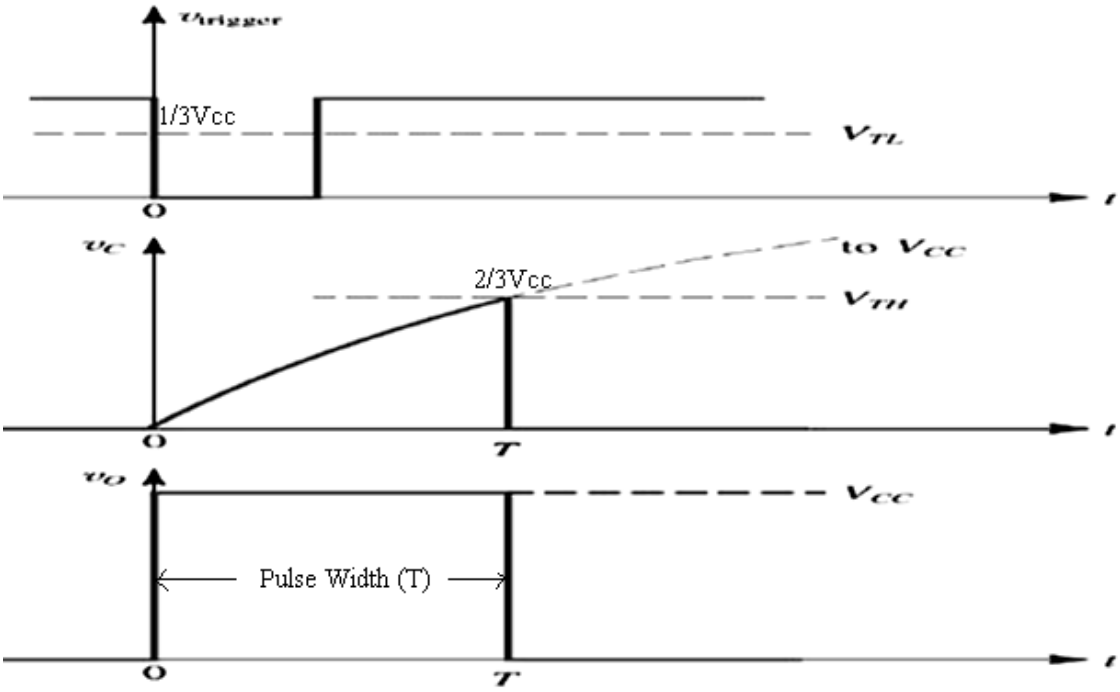
Assume C = 0.01μF

T = 1.096RC

R = T / 1.096C = $(1*10^{-3})$ / $(1.096*0.01*10^{-6})$

= 9.12 kΩ ≈ 10 kΩ

MODEL GRAPH



OBSERVATION

Amplitude = (volts)

T_{ON} = (msec)

T_{OFF} = (msec)

Time period $=T_{ON} + T_{OFF}$ = (msec)

PROCEDURE:

1. The connections are made as per the diagram.
2. For monostable multivibrator the trigger input is given
3. The output is observed at pin 3 and across capacitor.
4. The theoretical frequency is verified with the practical.
5. This experiment can be repeated for various values of c for different frequency
6. Plot the output graphs.

THEORY:

A monostable multivibrator has one stable state and a quasistable state. When it is triggered by an external agency it switches from the stable state to quasistable state and returns back to stable state. The time during which it states in quasistable state is determined from the time constant RC. When it is triggered by a

continuous pulse it generates a square wave. Monostable multi vibrator can be realized by a pair of regenerative coupled active devices, resistance devices and op-amps.

RESULT:

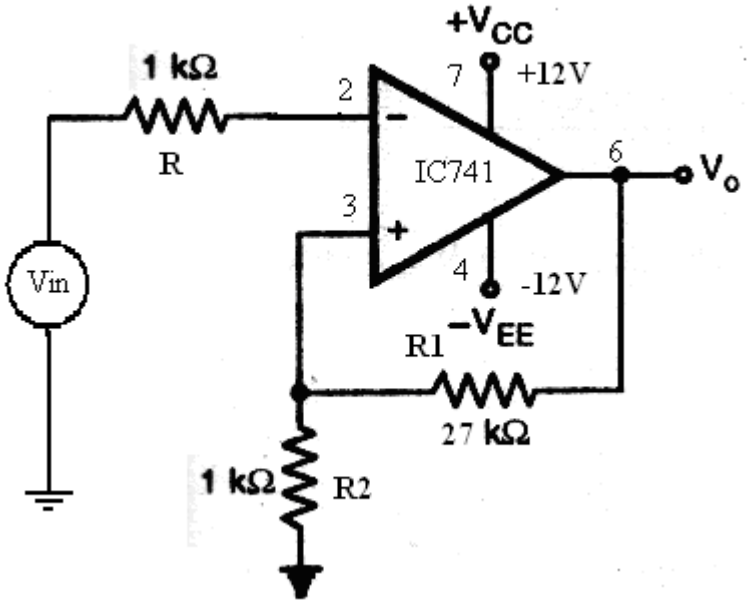
Thus the Astable and monostable multivibrator using IC555 was designed and its output waveform is traced.

Review Questions:

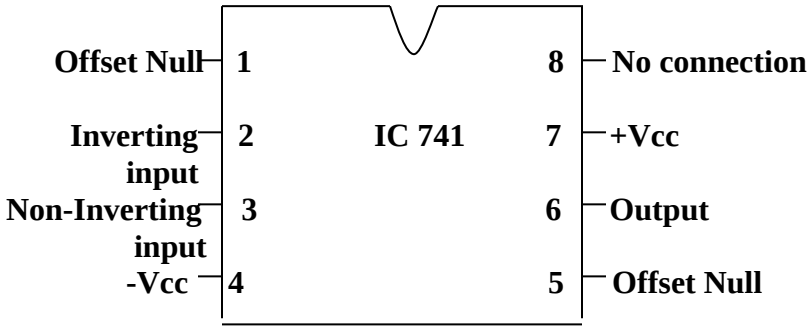
1. What is an astable multivibrator?
2. How astable mode of 555 Timer can be modified to get a square wave generator?
3. What is an monostable multivibrator?
4. How monostable mode of 555 Timer is designed?
5. Define duty cycle.

CIRCUIT DIAGRAM:

SCHMITT TRIGGER



PIN DIAGRAM:



Ex.No. 7 : SCHMITT TRIGGER

Preparatory Exercise:

1. What is an op-amp? Why it is called so?
2. List the ideal characteristics of an op-amp.
3. What are the building blocks of an op-amp?
4. List the applications of a comparator.

AIM

To design and implement a Schmitt trigger for the following specifications V_{UT} = 0.5 v, V_{LT}= -0.5v, Vsat = +12 V and $-V_{sat}$=-12V and V_{ref}=0v.

DESCRIPTION

Comparator:

Input : Sine input of 4V at 10 KHz
Output : Square Signal of 24 Vp-p at 10 KHz.
Hysterisis loop : Set the CRO in XY mode and view the hysteresis loop.

APPARATUS REQUIRED:

S.No.	ITEM	RANGE	QUANTITY
1	OP-AMP	IC741	1
2	RESISTOR	1kΩ,27kΩ	2,1
3	CRO	-	1
4	RPS	DUAL(0-30) V	1

DESIGN:

Given: $V_{UT} = -V_{LT} = 0.5V$

$V_{UT} = + Vsat\ R2/(R1+R2)$

$0.5 = 12\ (R2/(R1+R2))$

$R1 = 23\ R2$

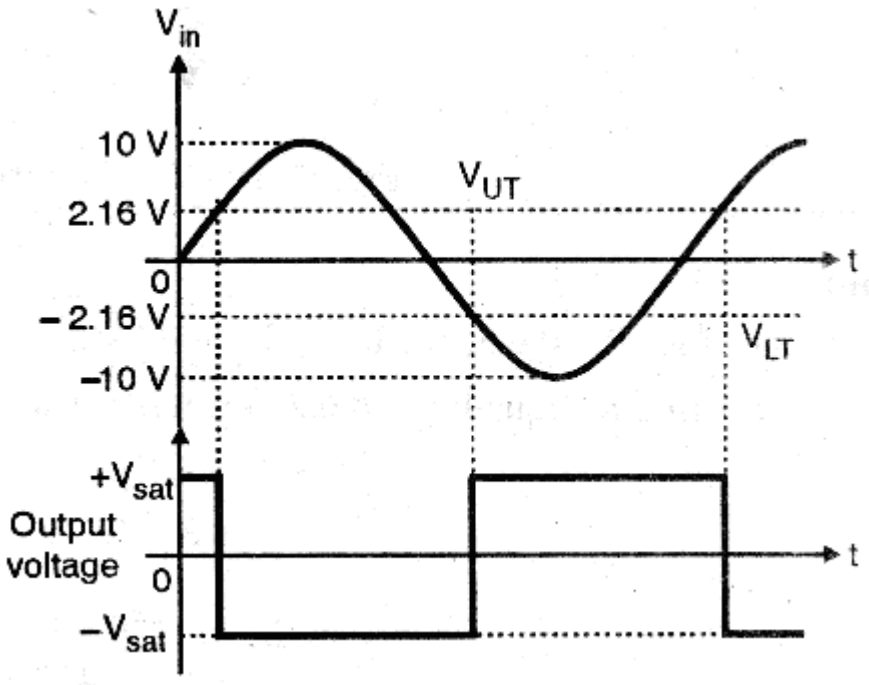
Assume $R2 = 1k\Omega$

Then $R1 = 23\ 1k\Omega$

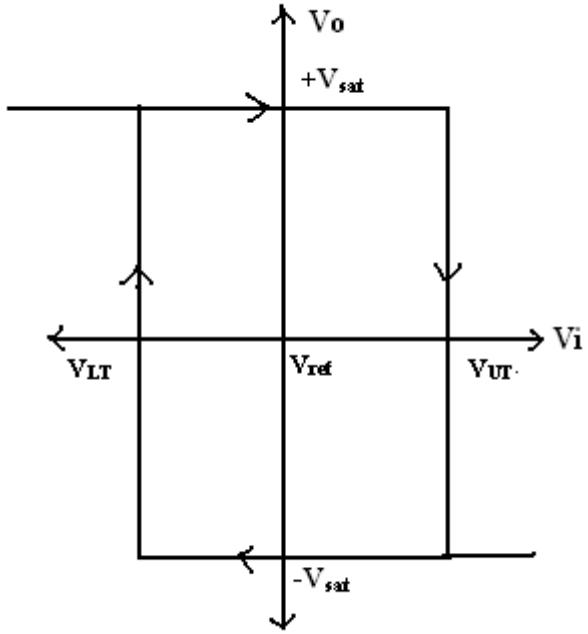
PROCEDURE :

1. The connections are made as shown in the circuit diagram.
2. Apply the input signal of desired amplitude and frequency to the negative input terminal of an op-amp.
3. Compare the input sine signal with the square wave output signal to determine the upper threshold voltage (V_{UT}) and the lower threshold voltage (V_{LT}).
4. Turn the timeperiod knob in CRO to the XY mode and determine the V_{UT} and the V_{LT} values and compare it with the previous observation in step 3.
5. Plot the input signal , output signal and the hysteresis loop in a linear graph.

MODEL GRAPH



HYSTERESIS LOOP



THEORY:

Comparator

Schmitt trigger is useful in converting a slowly varying input signal into a square waveforms. It is a regenerative comparator. The input voltage is applied to the negative terminal and the feedback is applied to the positive input terminal of the op-amp. Tthe output voltage V_O swings between the +Vsat and the –Vsat when each time the input signal V_i exceeds the threshold levels V_{UT} and V_{LT}. The hysteresis or backlash for a comparator occurs when a positive feedback is employed. It is defined as the difference between the V_{UT} and V_{LT}.

RESULT:

The Schmitt trigger circuit is connected and the waveforms are observed and theoretical and practical values of the threshold values are verified.

	V_{UT} (volts)	**V_{LT} (volts)**
Theoretical values =		
Practical values =		

(From the graph) Hysteresis width = $V_{UT} - V_{LT}$ =

Review Questions:

1. Why Schmitt trigger is called as a regenerative comparator?
2. What is Hysteresis?
3. Mention the applications of Schmitt trigger.

EXPT NO: 8

DATE :

STUDY OF LOGIC GATES, HALF ADDER AND FULL ADDER

AIM:

To study the basic logic gates and construct half adder, full adder circuits and verifies their truth tables using logic gates.

COMPONENTS REQUIRED:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	NAND GATE 2 I/P	IC 7400	1
5.	NOR GATE	IC 7402	1
6.	X-OR GATE	IC 7486	1
7.	X-NOR GATE	IC747266	1
8.	AND GATE 3 I/P	IC 7411	1

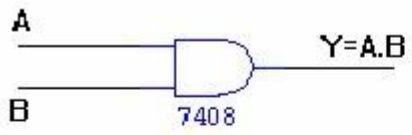
9.	NAND GATE 3 I/P	IC 7410	1
10.	IC TRAINER KIT	-	1
11.	PATCH CORD	-	14

PRE-LAB EXCERICE:

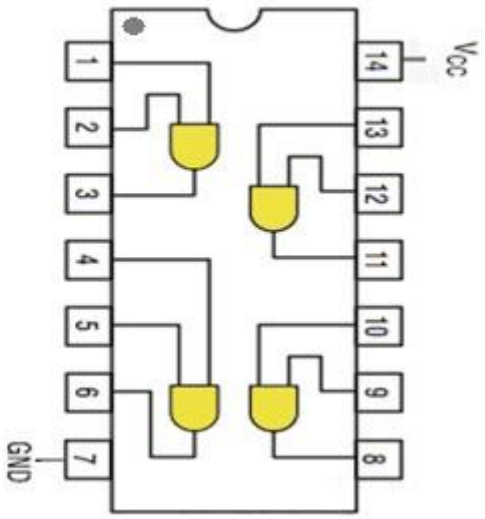
1. Differentiate Bit, Byte, and Nibble.
2. Explain the term universal gate.
3. What is a truth table? What is its significance in logic operations?
4. Define Minterm.& Maxterm.
5. What is sequential logic circuit?

AND GATE:

SYMBOL



PIN DIAGRAM

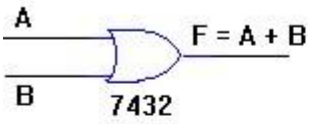


TRUTH TABLE

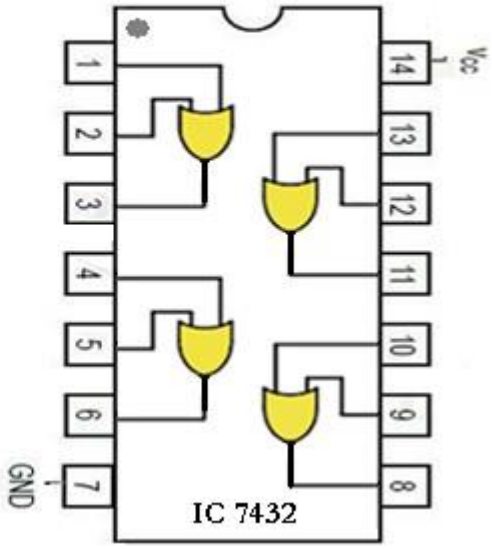
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE:

SYMBOL :



PIN DIAGRAM :



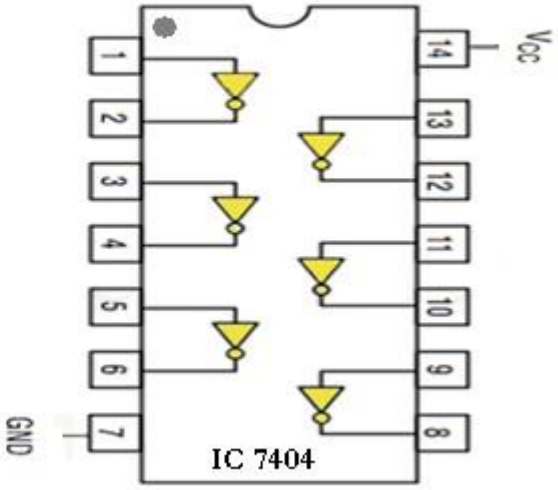
TRUTH TABLE

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

SYMBOL

PIN DIAGRAM

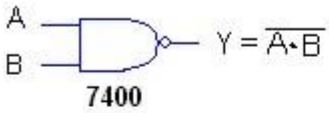


TRUTH TABLE :

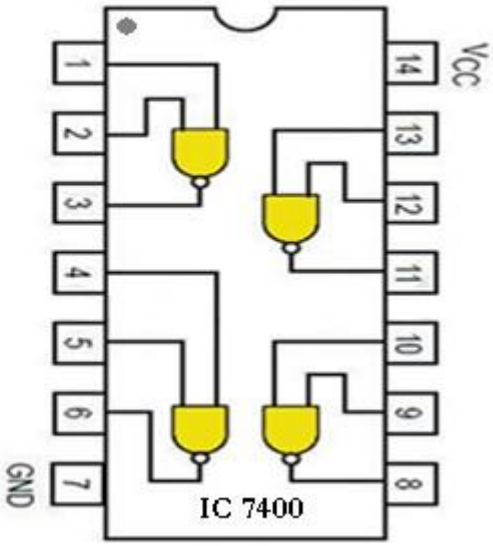
A	$\overline{A}$
0	1
1	0

2-INPUT NAND GATE:

SYMBOL



PIN DIAGRAM



TRUTH TABLE

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

THEORY:

Digital electronics is based on the binary number system. Instead of voltages which vary continuously, as in analog electronics, digital circuits involve voltages which take one of only two possible values. In our case these are 0 and 5 volts (TTL logic), but they are often referred to as LOW and HIGH, or FALSE and TRUE, or as the binary digits 0 and 1.The basic building blocks of digital electronics are logic gates which perform simple binary logic functions (AND, OR, NOT, etc.). From these devices, one can construct more complex circuits to do arithmetic, act as memory elements, and so on. Logic gates and other digital components come in the form of integrated circuits (ICs) which consist of small semiconductor chips packaged in a ceramic or plastic case with many pins.

The ICs are labeled by numbers like 74LSxx, where LS is technologies and xx is a number identifying the type of device.

Circuit that takes the logical decision and the process are called logic gates. Each gate has one or more input and only one output.

OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE (7408):

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE (7432):

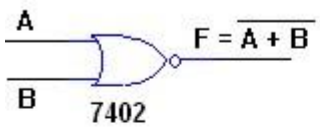
The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE (7404):

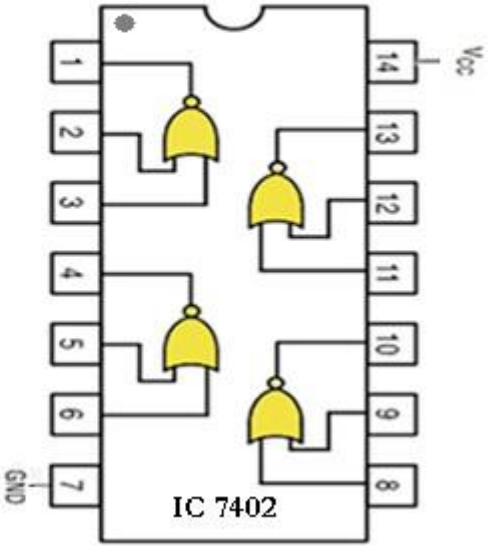
The NOT gate is called an inverter. The output is high when the input is low. The output is low when the input is high. (i.e., output is Complement of the input)

NOR GATE:

SYMBOL :



PIN DIAGRAM :

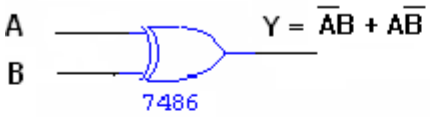


TRUTH TABLE

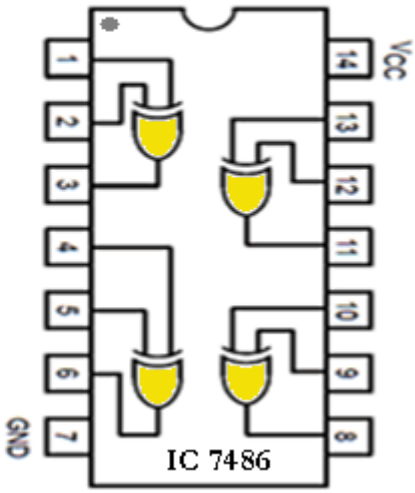
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

X-OR GATE:

SYMBOL



PIN DIAGRAM



TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

NAND GATE (7400):

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low. The output is low level when both inputs are high.

NOR GATE (7402):

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

X-OR (Exclusive OR) GATE (7486):

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

X-NOR (Exclusive NOR) GATE (747266):

The output is high when both the inputs are low and both the inputs are high. The different inputs will produce low output (i.e. Logic '0').

HALF ADDER:

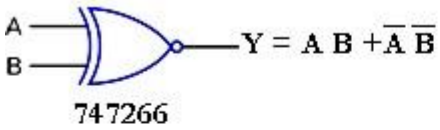
A half adder is a combinational circuit needs two binary inputs and two binary outputs. The input variables designate the augend and addend bits, the output variables produce the sum and carry. The half-adder can be implemented with an exclusive –OR and an AND gate.

FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

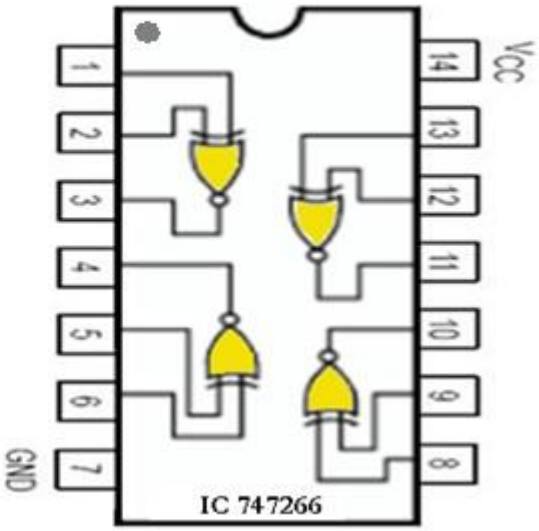
X-NOR GATE :

SYMBOL



747266

PIN DIAGRAM

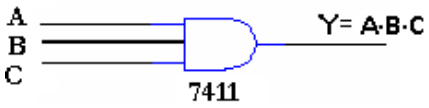


TRUTH TABLE :

A	B	AB + $\overline{A}\overline{B}$
0	0	**1**
0	1	**0**
1	0	**0**
1	1	**1**

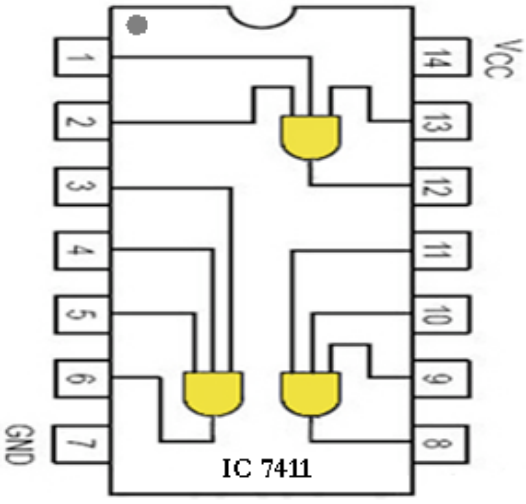
3-INPUT AND GATE :

SYMBOL



7411

PIN DIAGRAM



TRUTH TABLE

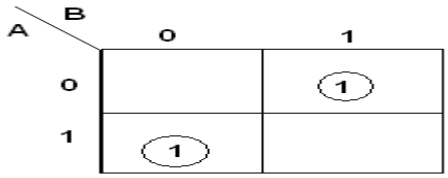
A	B	C	A·B·C
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

HALF ADDER

TRUTH TABLE:

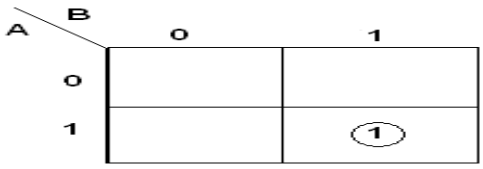
Inputs		Outputs	
A	**B**	**CARRY**	**SUM**
0	**0**	**0**	**0**
0	**1**	**0**	**1**
1	**0**	**0**	**1**
1	**1**	**1**	**0**

K-Map for SUM:



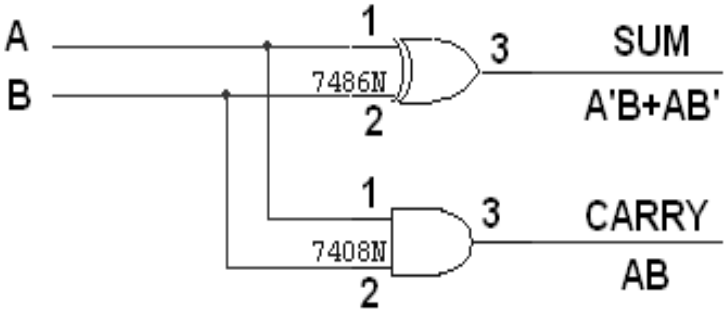
SUM = A'B + AB'
= $A \oplus B$

K-Map for CARRY:



CARRY = AB

LOGIC DIAGRAM:



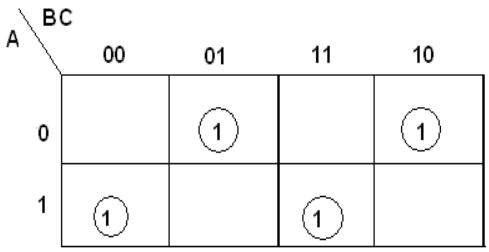
FULL ADDER

FULL ADDER USING TWO HALF ADDER:

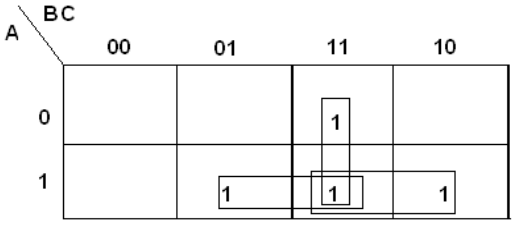
TRUTH TABLE:

Inputs			Outputs	
A	**B**	**C**	**CARRY**	**SUM**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

K-Map for SUM:



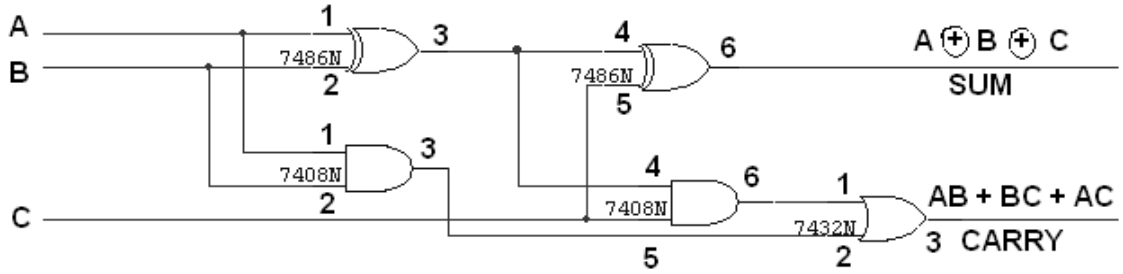
K-Map for CARRY:



SUM = A'B'C + A'BC' + ABC' + ABC
= C(A'B'+AB) + C'(A'B+AB')
= A ⊕ B ⊕ C

CARRY = AB + BC + AC

LOGIC DIAGRAM:



PROCEDURE:

(i) Connections are given as per circuit diagram.

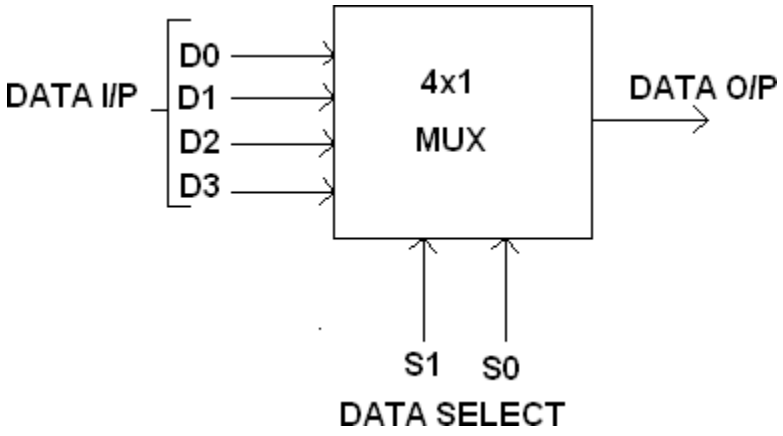
(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

4:1 MULTIPLEXER

BLOCK DIAGRAM:



FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

EXPT NO : 9 **DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER USING LOGIC GATES**

AIM:

i. To design and implement 4 x 1 MUX and 1x 4 DEMUX using logic gates.
ii. To implement the Boolean function F (A, B, C) = ∑m (1,3,4,7) with A as input.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P AND GATE	IC 7411	2
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	32

PRE-LAB EXCERICE:

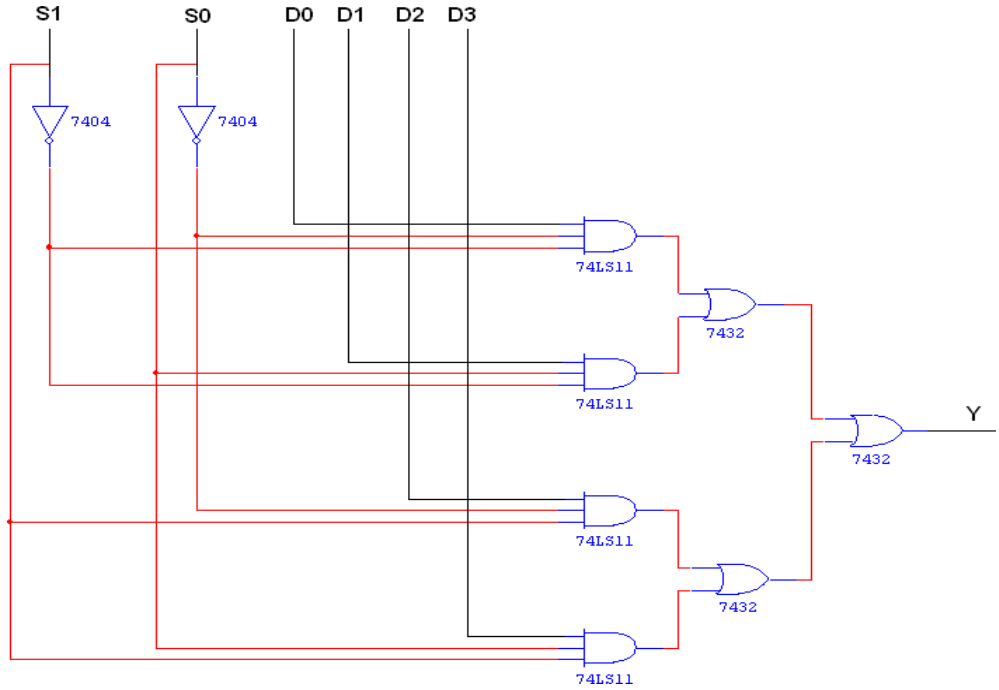
1. What is another name of multiplexer?
2. What is a four channel multiplexer?
3. What is the function of a multiplexer's select inputs?
4. What are the major applications of multiplexers?
5. Identify each MSI device? (a)74157 (b) 71151 (c)74150

THEORY:

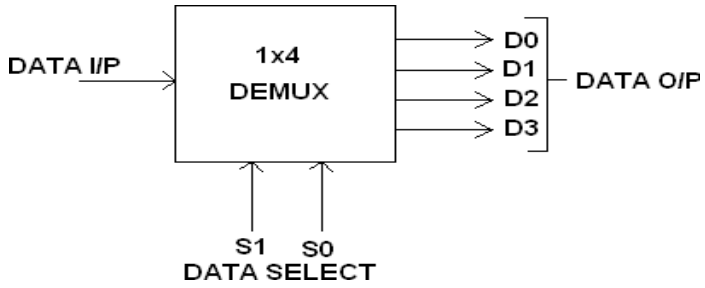
MULTIPLEXER:

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2^n input line and n selection lines whose bit combination determine which input is selected.

LOGIC DIAGRAM FOR MULTIPLEXER:



BLOCK DIAGRAM:



FUNCTION TABLE:

S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

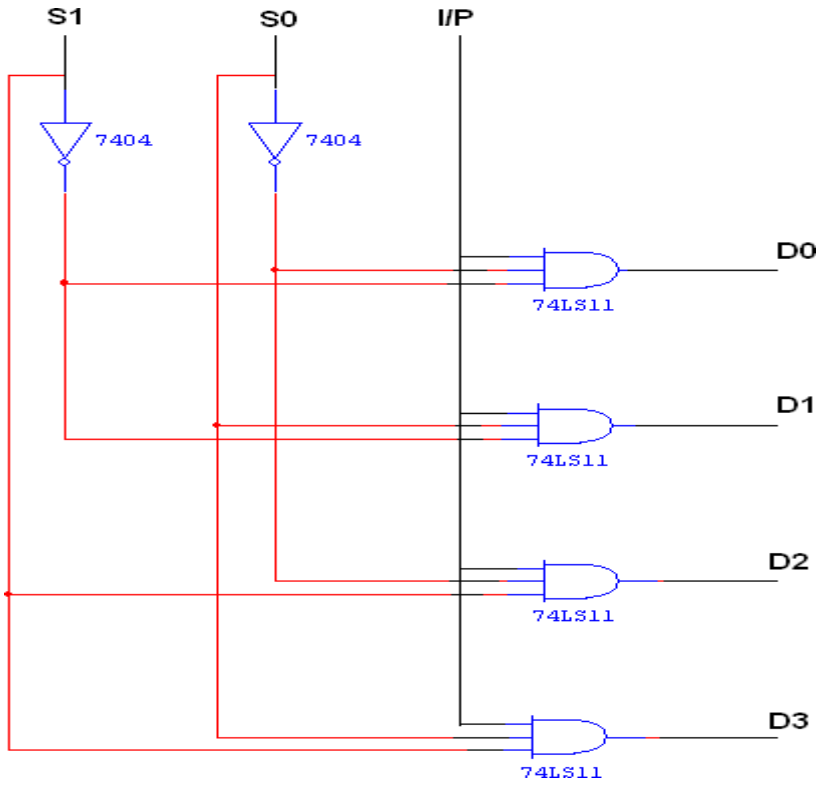
In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

1:4 DEMULTIPLEXER

TRUTH TABLE:

INPUT			OUTPUT			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

LOGIC DIAGRAM FOR DEMULTIPLEXER:



FUNCTION TABLE:

SI	SO	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

IMPLEMENTATION TABLE:

	D0	D1	D2	D3
$\overline{A}$	0	(1)	(4)	5
A	2	(3)	6	(7)
	0	1	$\overline{A}$	A

TRUTH TABLE:

F(A,B,C) = ∑m (1,3,4,7)

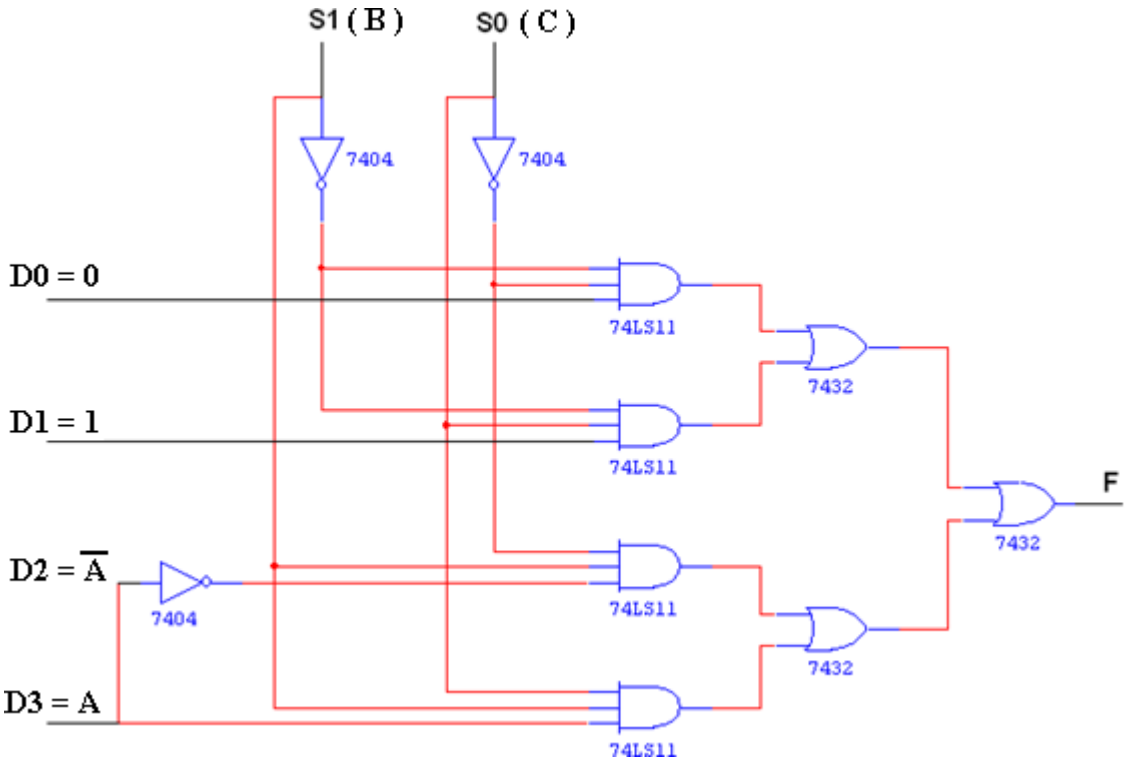
MIN TERM	DATA A	S1 B	S0 C	F
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	1

MULTIPLEXER IMPLEMENTATIONS:

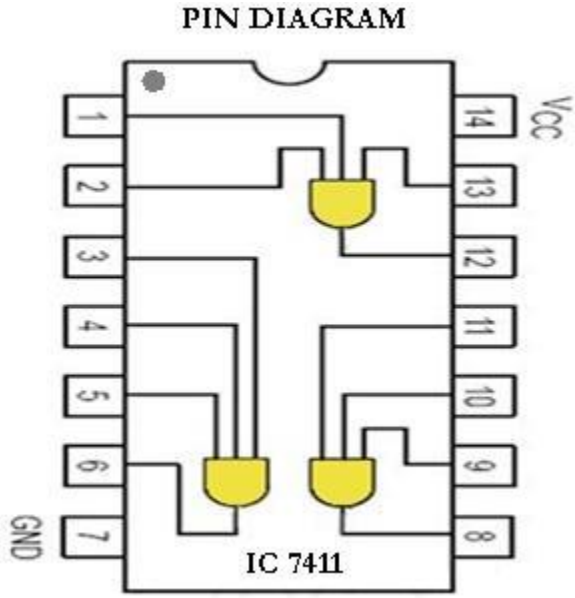
A digital multiplexer is a combinational circuit that selects one digital information from several sources and transmits the selected information on a single output line. It is also called a data selector since it selects one of many inputs and steers the information to the output. It has several data input lines and a single output line. The selection of the particular input line is controlled by a set of selection lines.

General procedure for implementing any Boolean function of n variables with a multiplexer with n-1 selection inputs and 2^{n-1} data inputs, The Boolean function is first listed in a truth table. The first n-1 variables in the table are applied to the selection inputs of the multiplexer. For each combination of the selection variables we evaluate the output as function of the last variable. This function can be 0,1 the variable, or the complement of the variable. These values are then applied to the data inputs in the proper order.

LOGIC DIAGRAM USING BASIC GATES:



3 I/P AND GATE:



PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

APPLICATION:

i. It can be used to implement logic functions in SOP form.

ii. It can be used to as a parallel to serial converter.

POST-LAB EXCERICE:

1. What is another name of demultiplexer?
2. What are the differences between a MUX & DEMUX?
3. How would you construct a logic function generator using multiplexers?
4. Draw logic symbol of a 4-to-1 multiplexer.
5. How many pins in IC74150?

RESULT:

Thus the multiplexer and De-multiplexer using logic gates were designed and implemented.

EXPT NO : 10 DESIGN AND IMPLEMENTATION OF ENCODER AND DECODER USING LOGIC GATES

AIM:

To design and implement encoder and decoder using logic gates.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	3 I/P NAND GATE	IC 7410	2
2.	OR GATE	IC 7432	3
3.	NOT GATE	IC 7404	1
2.	IC TRAINER KIT	-	1
3.	PATCH CORDS	-	27

PRE-LAB EXCERICE:

1. What is meant by encoder?
2. What is meant by decoder?
3. What is priority encoder?
4. What are the applications of encoder and decoder?
5. What is BCD to seven segment decoder?

THEORY:

ENCODER:

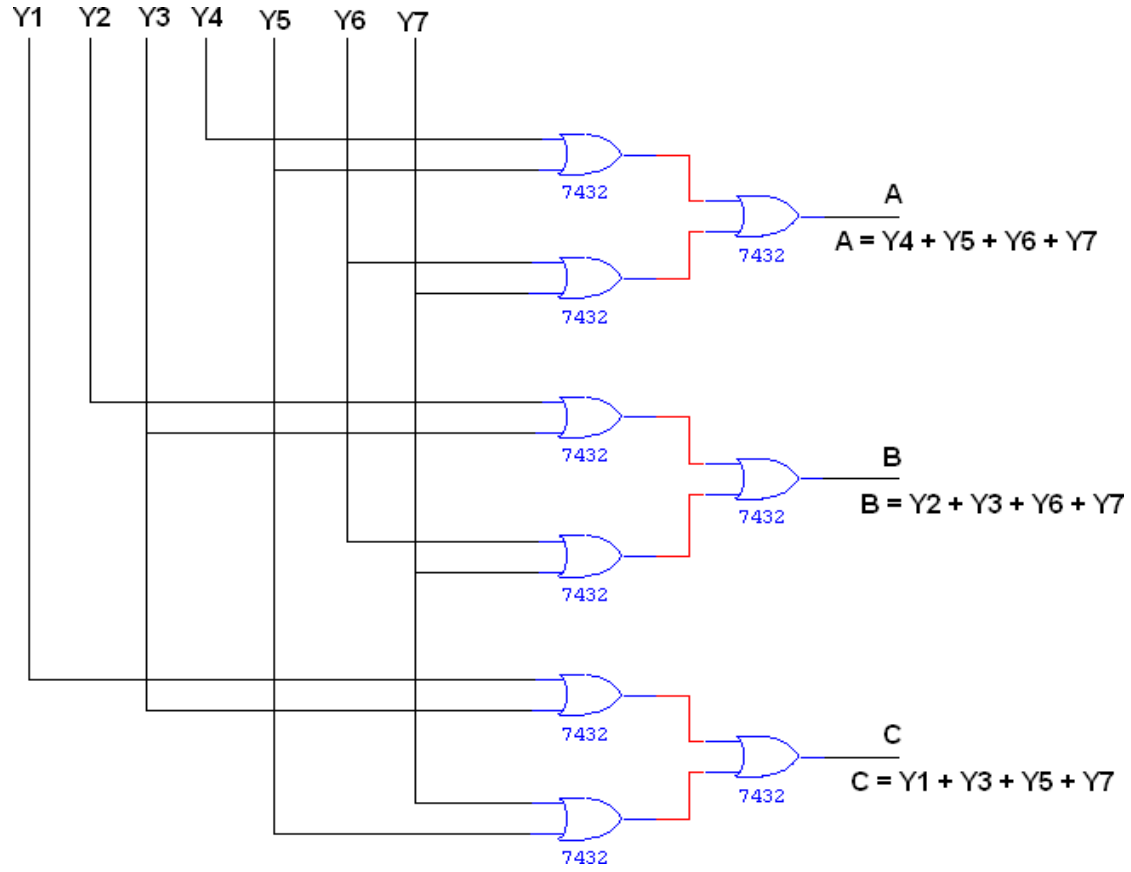
An encoder is a digital circuit that perform inverse operation of a decoder. An encoder has 2^n input lines and n output lines. In encoder the output lines generates the binary code corresponding to the input value. In octal to binary encoder it has eight inputs, one for each octal digit and three output that generate the corresponding binary code. In encoder it is assumed that only one input has a value of one at any given time otherwise the circuit is meaningless. It has an ambiguila that when all inputs are zero the outputs are zero. The zero outputs can also be generated when D0 = 1.

ENCODER

TRUTH TABLE:

INPUT								OUTPUT		
Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	A	B	C
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

LOGIC DIAGRAM

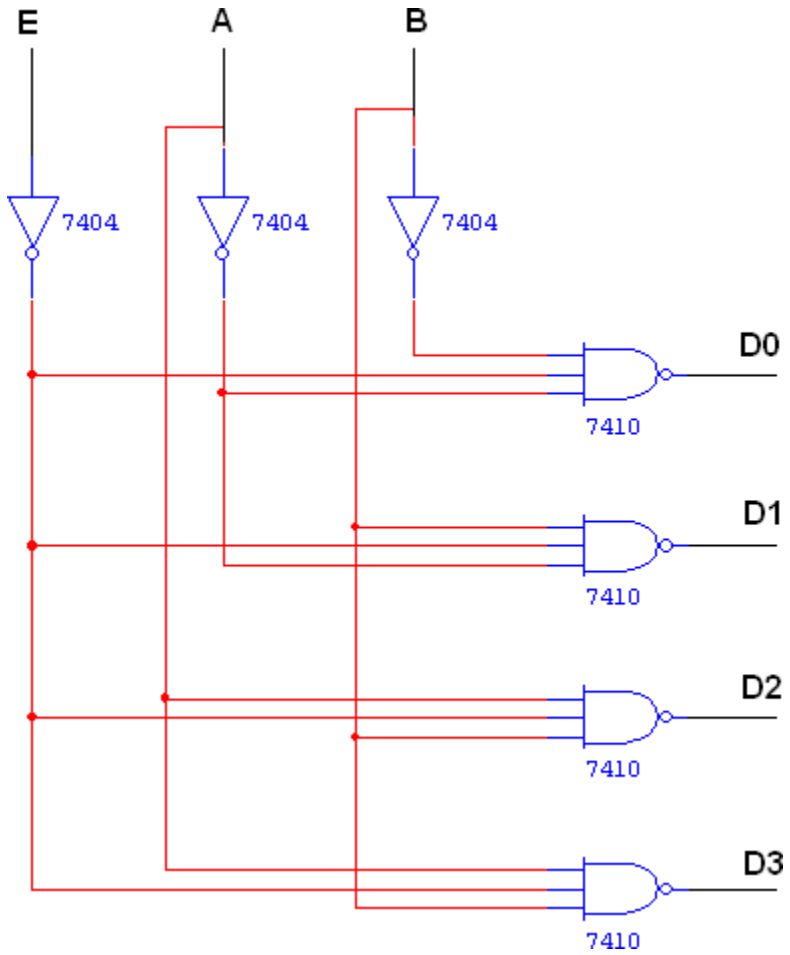


DECODER

TRUTH TABLE:

INPUT			OUTPUT			
E	**A**	**B**	**D0**	**D1**	**D2**	**D3**
1	**0**	**0**	**1**	**1**	**1**	**1**
0	**0**	**0**	**0**	**1**	**1**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**
0	**1**	**0**	**1**	**1**	**0**	**1**
0	**1**	**1**	**1**	**1**	**1**	**0**

LOGIC DIAGRAM:



DECODER:

A decoder is a multiple input multiple output logic circuit which converts coded input into coded output where input and output codes are different. The input code generally has fewer bits than the output code. Each input code word produces a different output code word i.e there is one to one mapping can be expressed in truth table. In the block diagram of decoder circuit the encoded information is present as n input producing 2^n possible outputs. 2^n output values are from 0 through out $2^n - 1$.

PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

POST-LAB EXCERICE:

1. Can more than one decoder output be activated at one time? Justify your answer.
2. What is the function of a decoder's enable input(s)?
3. How does an encoder differ from decoder?
4. How does a priority encoder differ from an ordinary encoder?
5. What is decimal to BCD encoder?

RESULT:

Thus the encoder and decoder using logic gates was designed and implemented and studied.

EXPT. NO: 11 **DATE :**

STUDY OF SHIFT REGISTERS IN VARIOUS MODE OF OPERATION

AIM:

To study and implement shift register in various modes of operation

(i) Serial in serial out
(ii) Serial in parallel out
(iii) Parallel in serial out
(iv) Parallel in parallel out

APPARATUS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	D flip flop	IC 7474	2
2.	OR gate	IC 7432	1
3.	IC Trainer kit	-	1
4.	Patch cords	-	As required

THEORY:

SHIFT REGISTER:

The Shift Register is another type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle, hence the name "shift register". It basically consists of several single bit "D-Type Data Latches", one for each bit (0 or 1) connected together in a serial or daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

The data bits may be fed in or out of the register serially, i.e. one after the other from either the left or the right direction, or in parallel, i.e. all together. The number of individual data latches required to make up a single Shift Register is determined by the number of bits to be stored with the most common being 8-bits (one byte) wide, i.e. eight individual data latches. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a ‘‘clear” or “reset” connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

Serial-in to Parallel-out (SIPO):

The register is loaded with serial data, one bit at a time, with the stored data being available in parallel form.

Serial-in to Serial-out (SISO):

The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

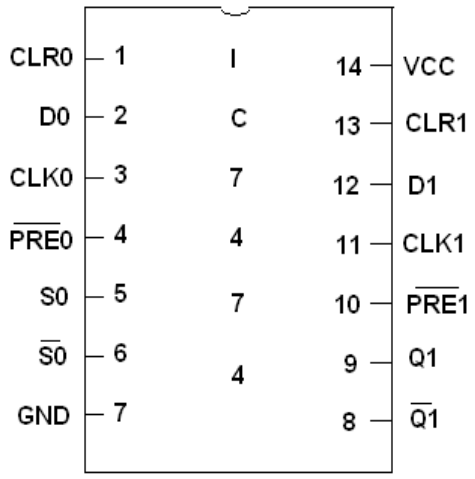
Parallel-in to Serial-out (PISO):

The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

Parallel-in to Parallel-out (PIPO):

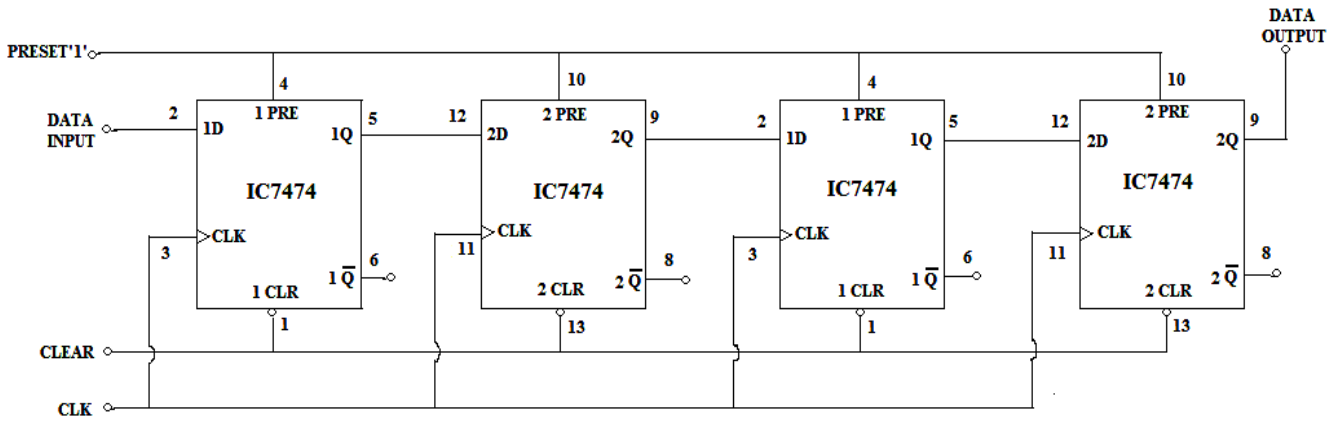
The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

PIN DIAGRAM:



LOGIC DIAGRAM:

SERIAL IN SERIAL OUT:

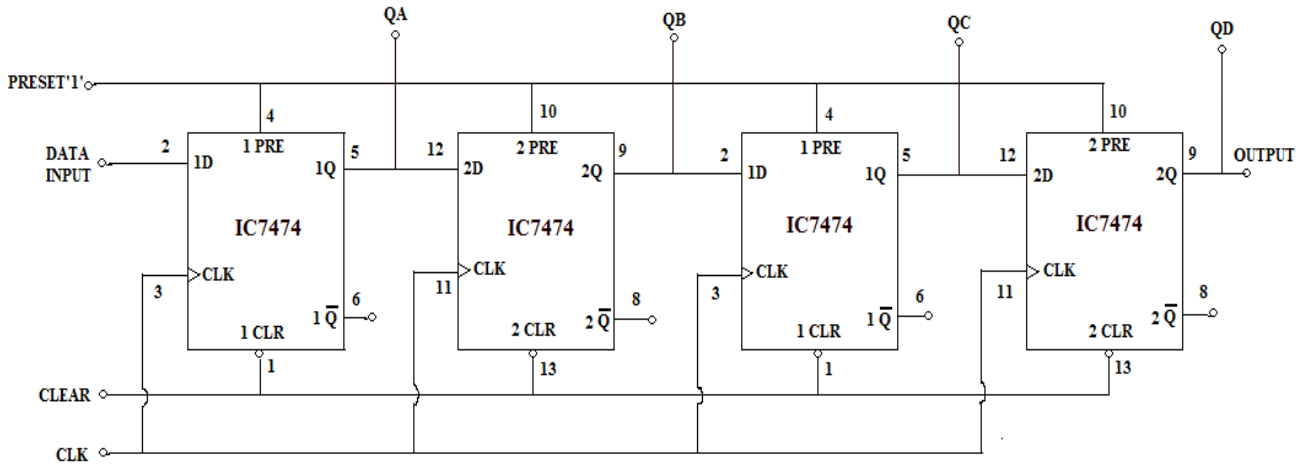


TRUTH TABLE:

CLK	Serial inputs	Serial outputs
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

LOGIC DIAGRAM:

SERIAL IN PARALLEL OUT:

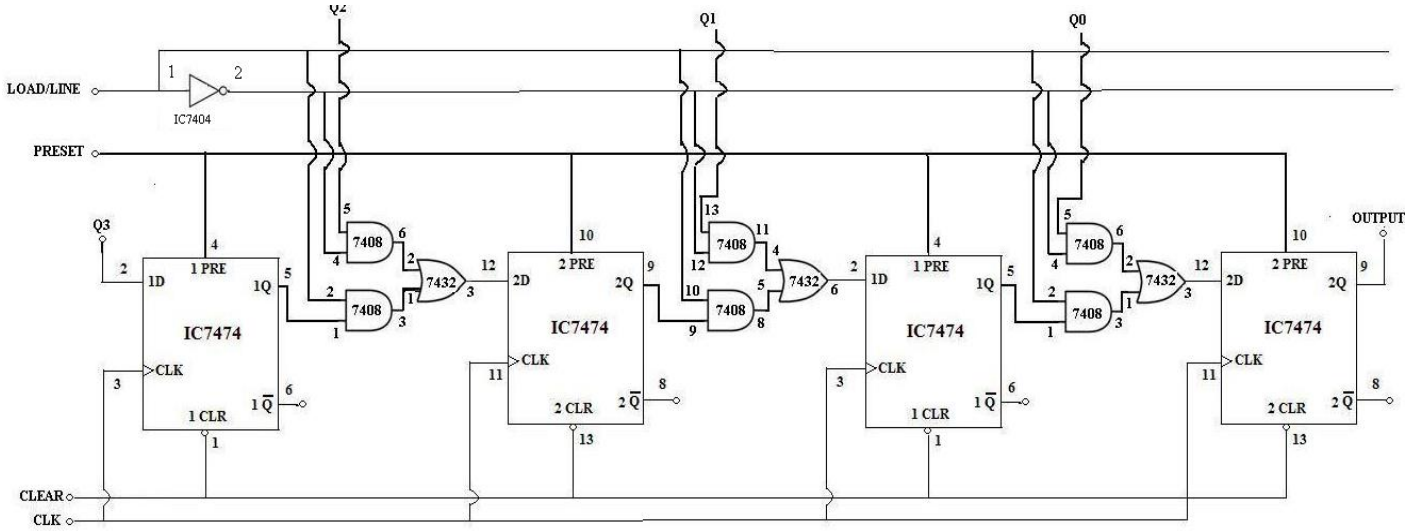


TRUTH TABLE:

CLK	Serial inputs	Parallel Outputs			
		Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	1	1	0	0	1

LOGIC DIAGRAM:

PARALLEL IN SERIAL OUT:

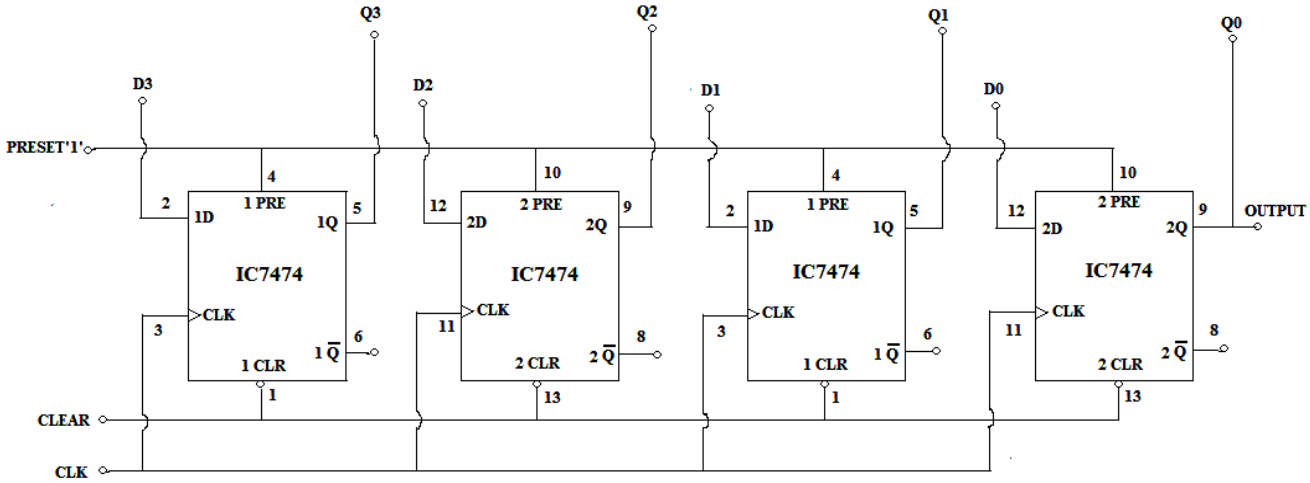


TRUTH TABLE:

CLK	Parallel Inputs				Serial Output
	Q3	Q2	Q1	Q0	
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

LOGIC DIAGRAM:

PARALLEL IN PARALLEL OUT:



TRUTH TABLE:

CLK	Parallel Inputs				Parallel Outputs			
	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

PROCEDURE:

(i) Connections are given as per circuit diagram.

(ii) Logical inputs are given as per circuit diagram.

(iii) Observe the output and verify the truth table.

RESULT:

EXPT NO : 12

Date:

CONSTRUCTION AND VERIFICATION OF 4 BIT RIPPLE COUNTER AND MOD 10/MOD 12 RIPPLE COUNTER

AIM:

To design and verify 4 bit ripple counter mod 10/ mod 12 ripple counter.

COMPONENTS REQUIRED:

Sl.No.	COMPONENT	SPECIFICATION	QTY.
1.	JK FLIP FLOP	IC 7476	2
2.	NAND GATE	IC 7400	1
3.	IC TRAINER KIT	-	1
4.	PATCH CORDS	-	30

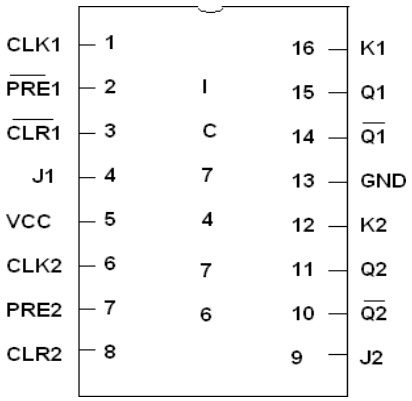
PRE-LAB EXCERICE:

1. What is counter?
2. What are the types of counter?
3. Distinguish between a ripple counter & a synchronous counter.
4. Define the modulus of a counter.
5. How is a modulus counter built using count reset?

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or Q output of previous stage. A soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

PIN DIAGRAM FOR IC 7476:

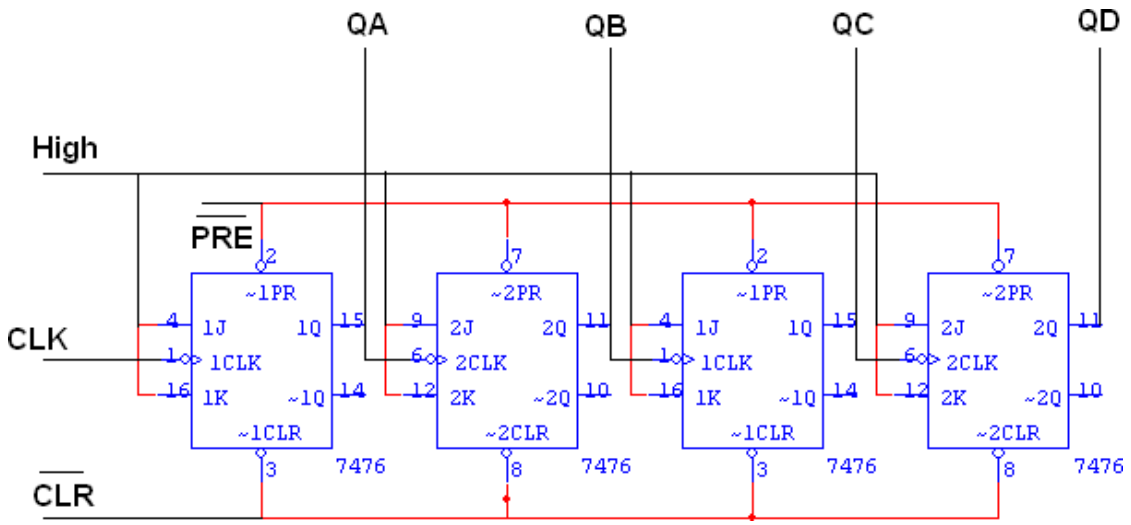


4 BIT RIPPLE COUNTER

TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

LOGIC DIAGRAM:



NOTE:

In 4 bit Ripple counter, Mod-10, and Mod-12 Ripple counter

Use One IC7476 for FF A & C and another One IC7476 for FF B & D.

MOD - 10 RIPPLE COUNTER

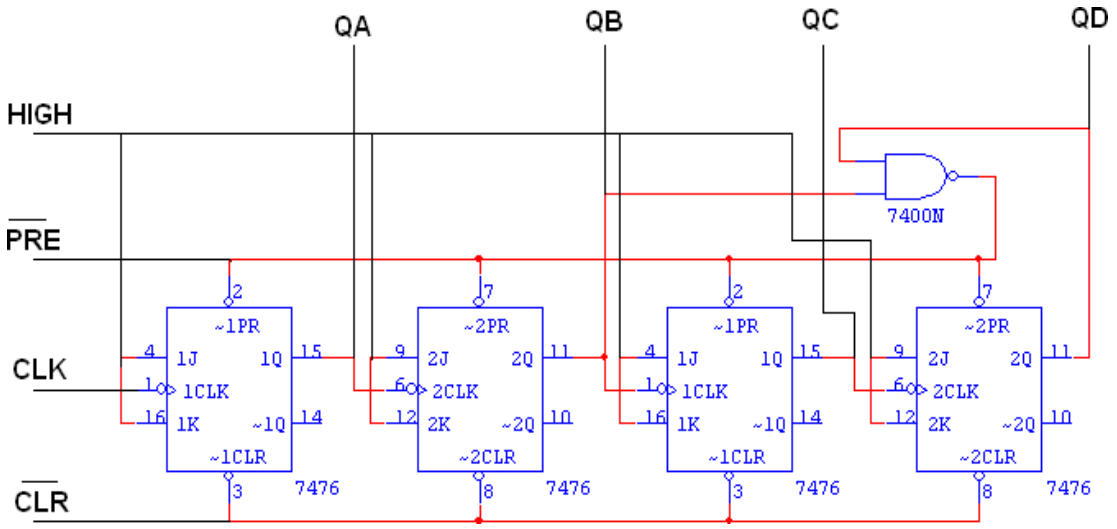
TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

PROCEDURE:

(i) Connections are given as per circuit diagram.
(ii) Logical inputs are given as per circuit diagram.
(iii) Observe the output and verify the truth table.

LOGIC DIAGRAM:



MOD - 12 RIPPLE COUNTER

TRUTH TABLE:

CLK	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	0	0

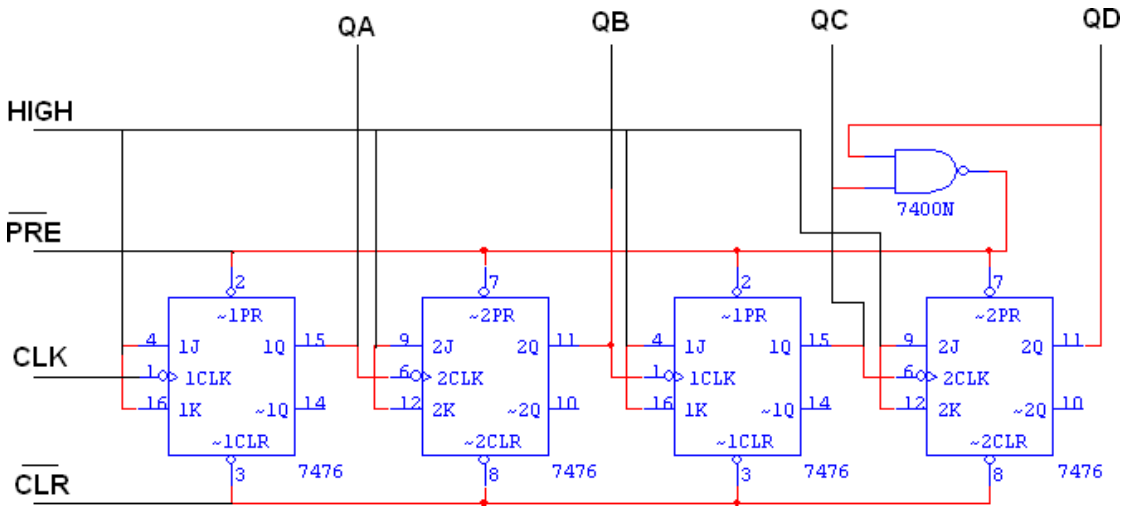
APPLICATIONS:

It is used as frequency divider in digital time pieces such as electronic digital clocks, automobile digital clock and frequency counters.

POST-LAB EXCERICE:

1. What is an in asynchronous sequential circuit?
2. What is a sequence generator?
3. What is an asynchronous decade counter?
4. Define synchronous counter.
5. What is Johnson counter?

LOGIC DIAGRAM:

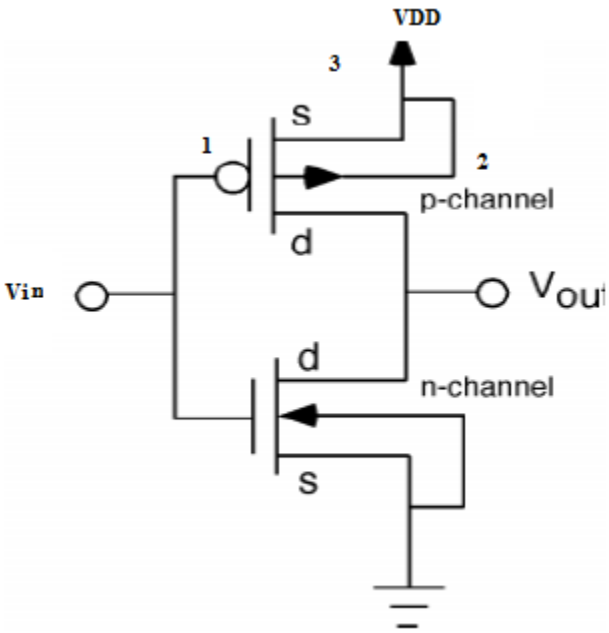


RESULT:

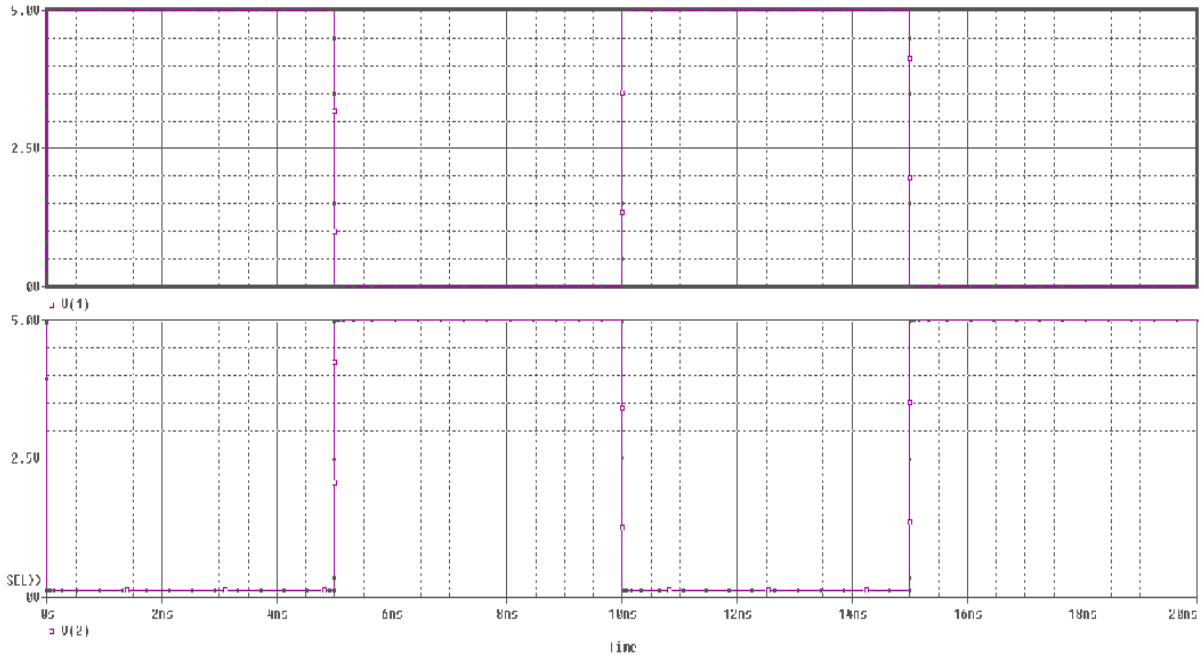
Thus the 4 bit ripple counter and Mod-10 /Mod-12 ripple counter were constructed and their state tables were verified.

CMOS INVERTER

CIRCUIT DIAGRAM



OUTPUT



Ex No 13. PSPICE PROGRAM FOR CMOS INVERTER

AIM:

To simulate a CMOS Inverter using PSPCIE software

PROGRAM FOR CMOS INVERTER

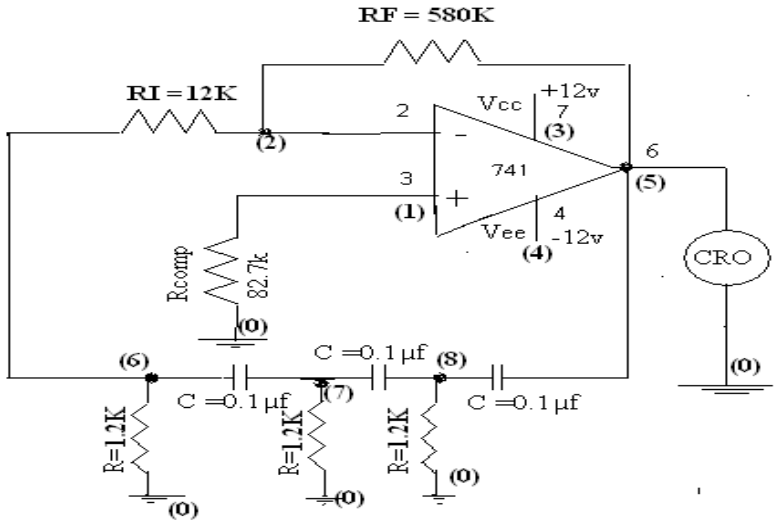
```
VIN 1 0 PULSE(0 5 0 1P 1P 5N 10N)

VDD 3 0 5

M2  2 1 3 3 PTYPE  W=5u L=2.5u

M1  2 1 0 0 NTYPE  W=5u L=5u

.MODEL PTYPE PMOS(KP=15U VTO =1)

.MODEL NTYPE NMOS(KP=30U VTO =1)

.PROBE

.TRAN 1N 20N

.END
```

RESULT:

Thus the CMOS inverter is simulated using PSPICE Software.

RC PHASE SHIFT OSCILLATOR

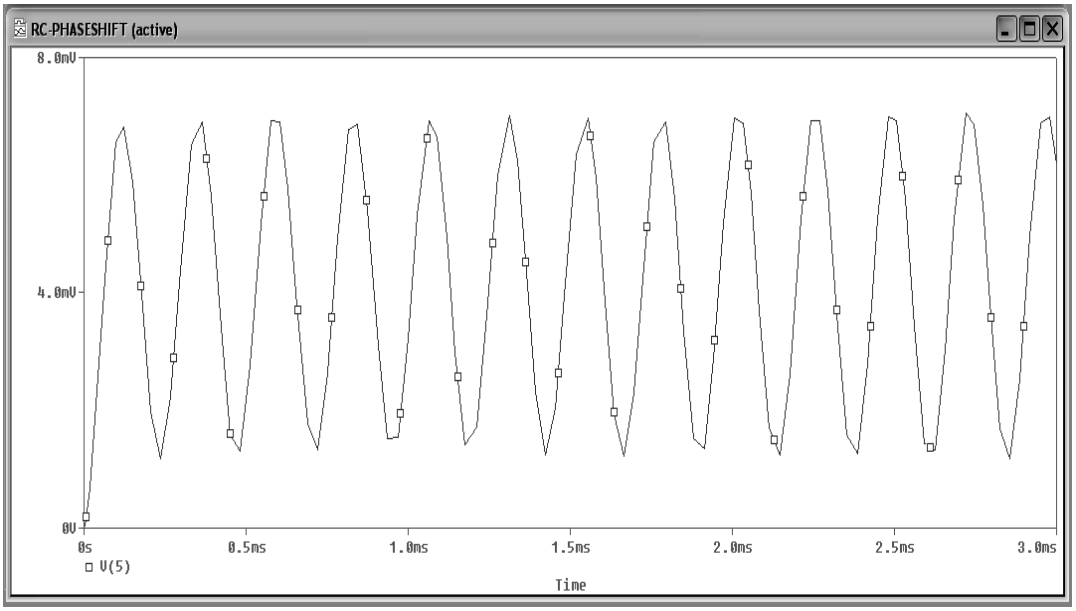
CIRCUIT DIAGRAM



(n) --- Represent node numbers

n --- Represent Pin number of IC

OUTPUT



PSPICE PROGRAM FOR RC PHASE SHIFT OSCILLATOR

AIM:

To simulate the RC phase shift oscillator using PSPICE software

PROGRAM FOR RC PHASE SHIFT OSCILLATOR

```
RCOMP    1    0    82.7K
RI       2    6    12K
RF       2    5    580k
C1       6    7    0.01UF
C2       7    8    0.01UF
C3       8    5    0.01UF
R1       6    0    1.2K
R2       7    0    1.2K
R3       8    0    1.2K
VCC      3    0    DC   12V
VEE      0    4    DC   12V
X1       1    2    3    4    5    UA741
.LIB     OPAMP.LIB
*.LIB    EVAL.LIB
.TRAN5US    3MS    UIC
.PRINT      TRAN V(5)
.PROBE
.END
```

Result

Thus the RC phase shift oscillator is simulated using PSPICE software