SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

III SEMESTER

EC3366 DIGITAL SYSTEMS DESIGN

Academic Year 2025 – 2026 (ODD Semester)

Prepared by

Dr. N. Jothy, Assistant Professor (Sr.G)

Dr. C. Amali, Associate Professor

Dr. S. Senthilmurugan, Assistant Professor (Sel.G)

SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

QUESTION BANK

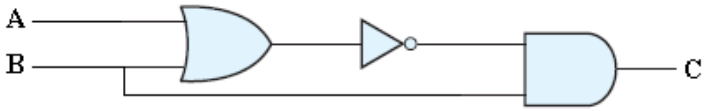
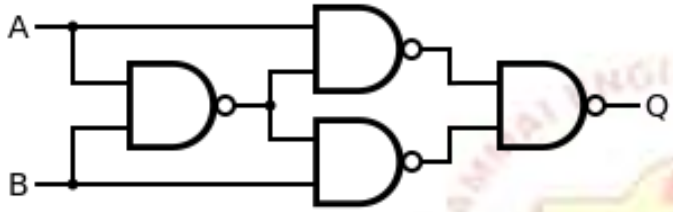
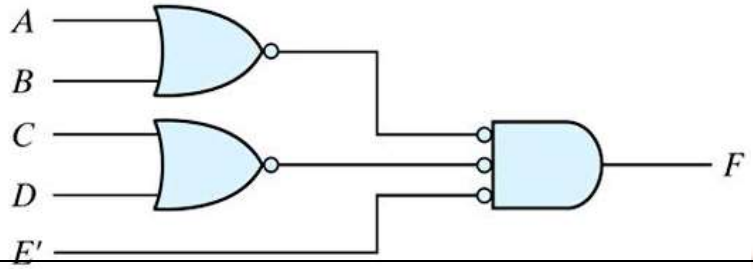
SUBJECT CODE/NAME :EC3366 / DIGITAL SYSTEMS DESIGN

YEAR / SEMESTER : II / III

UNIT I DIGITAL FUNDAMENTALS
Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements, Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes, Boolean theorems, Logic gates, Universal gates, Sum of products and product of sums, Minterms and Maxterms, Karnaugh map and Quine-McCluskey methods.

PART A

Q.No	Questions	CO	BT Level	Domain
1.	Convert the given decimal numbers into their binary equivalent $(108.364)_{10}$.	CO1	BTL 2	Understanding
2.	Convert the binary number 1011 to its decimal equivalent.	CO1	BTL 2	Understanding
3.	Compare Binary code and BCD code briefly.	CO1	BTL 3	Applying
4.	Outline the concept of duality in Boolean algebra.	CO1	BTL 1	Remembering
5.	Convert $A3B_H$ and $2F3_H$ into Binary and Octal respectively	CO1	BTL 2	Understanding
6.	Discuss the importance of Boolean theorems in simplifying logic circuits.	CO1	BTL 2	Understanding
7.	Convert $(115)_{10}$ into hexadecimal numbers.	CO1	BTL 2	Understanding
8.	Define 'Minterm' and 'Maxterm'.	CO1	BTL 1	Remembering
9.	State the Boolean theorem for commutativity.	CO1	BTL 1	Remembering
10.	Draw the active high tri-state Gate & write its truth table.	CO1	BTL 1	Remembering
11.	Illustrate the operation of an AND gate with its truth table.	CO1	BTL 2	Understanding
12.	Write the principle of Distributive law.	CO1	BTL 1	Remembering
13.	What is meant by Prime Implicants and Essential prime implicants?	CO1	BTL 1	Remembering
14.	Discuss the importance of Boolean theorems in simplifying logic circuits.	CO1	BTL 2	Understanding
15.	Compute the given function using NAND gates only. $F(X, Y, Z) = \sum m(0,6)$.	CO1	BTL 2	Understanding
16.	Write the equivalent Gray code for $[10110]_2$.	CO1	BTL 1	Remembering
17.	Differentiate between SOP and POS forms with an example.	CO1	BTL 2	Understanding

18.	Explain each step of the simplification process for the given expression $\overline{A + B\overline{C}}$ using De-Morgan's theorem.	CO1	BTL 2	Understanding
19.	Demonstrate how to implement Y = ∑(1, 4, 5, 6, 7) in SOP form using AOI (AND-OR-Invert) logic.	CO1	BTL 2	Understanding
20.	Determine the Boolean expression for the output of the system shown in figure. 	CO1	BTL 2	Understanding
21.	Summarize the steps involved in the Quine-McCluskey method	CO1	BTL 2	Understanding
22.	Interpret the Boolean function and the truth table of the given logic. 	CO1	BTL 2	Understanding
23.	Interpret the Boolean expression for the output of the system shown in the figure and explain the process used to derive it. 	CO1	BTL2	Understanding
24.	Simplify the expression $A\overline{B}C + \overline{A}\overline{B}C$ using Boolean theorems.	CO1	BTL 2	Understanding

PART – B

1.	Simplify the Minimized logic function using K-Maps. F (A, B, C, D) = ∑m (1,3,5,8,9,11,15)+ ∑d(2,13). Implement the minimal SOP using NAND and NOR gates.	(16)	CO1	BTL3	Applying
2.	Use the K-map method to find the minimal function for F(A,B,C,D,E) = ∑m(1,4,6,10,20,22,24,26) + ∑d(0,11,16,27). Draw the circuit of the minimal expression using basic gates.	(16)	CO1	BTL 3	Applying
3.	Analyze the given function Y (M, N, O, P, Q) =$\sum m(0,2,4,6,9,13,21,23,25,29,31)$. Draw the K-map and implement the simplified expression using basic gates.	(16)	CO1	BTL 4	Analyzing

4.	Analyze and minimize the following Boolean expressions using Boolean algebra. Draw the logic diagram for the minimized expressions. (i) F (X, Y, Z) =$(X+Y)\left(\overline{\overline{X}(\overline{Y}+\overline{Z})}\right)+\overline{XY}+\overline{XZ}$. (ii) F (X, Y, Z) =$\overline{XY}Z+\overline{X}YZ+X\overline{Y}$ (iii) F(X,Y,Z) =$XYZ+\overline{X}Z+YZ$	(6) (5) (5)	CO1	BTL 4	Analyzing
5.	(i) Apply your knowledge to explain Excess-3 codes and Gray Code with an example. (ii) Convert the Gray code (110101) to Binary code. (iii) Convert the binary number $(10101101)_2$ to Gray code	(6) (5) (5)	CO1	BTL 3	Applying
6.	Simplify the minimized Boolean expression for the function using K-map and draw the logic diagram. F (w, x, y,z)=$\sum m(0,1,2,4,5,6,8,9,12,13,14)$.	(16)	CO3	BTL 3	Applying
7.	Illustrate the logical Expression on a 4-variable K – map F=ABCD+AB'C'D'+AB'C+AB & realize using only NAND gates.	(16)	CO1	BTL 3	Applying
8.	Elaborate the minimization of the given Boolean function using Quine-Mc-Cluskey method F=∑m (0,1,2,5,7,8,9,10,13,15). Realize the simplified function using logic gates.	(16)	CO1	BTL 4	Analyzing
9.	Using K-map method, simplify the given Boolean function and obtain minimum POS expression and draw the logic diagram. X=$\prod m(1,3,5,7,9)+\prod d(8,11,15)$.	(16)	CO1	BTL 3	Applying
10.	Solve the following Function using Tabulation method F=∑m(1,2,3,7,8,9,10,11,14,15) and realize the circuit using logic gates.	(16)	CO1	BTL 3	Applying
11.	(i) Convert $(725.25)_8$ to its decimal, binary and Hexadecimal equivalent. (ii) Find 1's and 2's Complement of 8-digit binary number 10101101.	(8) (8)	CO1	BTL 3	Applying
12.	(i) Implement Y=$(A+C)(A+\overline{D})(A+B+\overline{C})$ (ii) Solve by perfect induction (a) A+AB = A (b) A(A+B) = A (c) A+A'B = A+B and (d) A(A'+B) =AB	(8) (8)	CO1	BTL 3	Applying
13.	Minimize the following Boolean function using K-map and implement the same using only NAND gates. F(A, B, C, D) = (D'+A'B'C' + AB'C' + A'BC'D).	(16)	CO1	BTL 3	Applying
14.	Determine simplified SOP for the following Boolean function using Quine- McCluskey Method. F(A, B, C, D) = ∑m(1, 3, 4, 5, 9, 10, 11) + ∑d(6, 8).	(16)	CO1	BTL 3	Applying
15.	Design the given function using Prime implicant method and Verify your result using K map F=$\sum m(0,1,2,4,5,6,8,9,12,13,14)$.	(16)	CO1	BTL 3	Applying

16.	Construct a Karnaugh Map for the following function F(A,B,C,D,E)= ∑(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31) and draw the logic diagram.	(16)	CO1	BTL 3	Applying
17.	Simplify the SOP form of the function F(A,B,C,D) = ∑m(0, 2, 6 ,8, 10, 12, 14, 15) and implement using basic gates.	(16)	CO1	BTL 4	Analyzing

UNIT II COMBINATIONAL CIRCUIT DESIGN

Design of Half and Full Adders, Half and Full Subtractors, Binary Parallel Adder – Carry look ahead Adder, BCD Adder, Multiplexer, Demultiplexer, Decoder, Encoder, Priority Encoder, Magnitude Comparator, Case study: 8 bit Arithmetic and logic unit.

PART A

Q.No	Questions	CO	BT Level	Domain
1.	Define combinational circuits.	CO2	BTL 1	Remembering
2.	Name some of the combinational circuits.	CO2	BTL 2	Understanding
3.	Summarize the design procedure of combinational circuits.	CO2	BTL 2	Understanding
4.	Write the Boolean expression for a half adder.	CO2	BTL 1	Remembering
5.	Construct a Full Adder circuit using XOR, AND, and OR gates.	CO2	BTL 2	Understanding
6.	From the truth table derive the logic equation of a half subtractor.	CO2	BTL2	Understanding
7.	Explain how a Carry Look-Ahead Adder (CLA) overcomes the speed limitation of ripple carry adders.	CO2	BTL 2	Understanding
8.	Differentiate between half adder and full adder.	CO2	BTL 2	Understanding
9.	Why is MUX called as a data selector?	CO2	BTL 2	Understanding
10.	List out the applications of multiplexer.	CO2	BTL 1	Remembering
11.	Mention the uses of demultiplexer.	CO2	BTL 2	Understanding
12.	How the decoder functions as a demultiplexer?	CO2	BTL 2	Understanding
13.	What do you mean by comparator?	CO2	BTL 1	Remembering
14.	Determine the maximum number of outputs for a decoder with a 6-bit data word.	CO2	BTL2	Understanding
15.	Point out the function of select inputs of a MUX.	CO2	BTL 2	Understanding
16.	Discuss the operation of the multiplexer in routing the selected input to the output Y.	CO2	BTL 1	Remembering
17.	Distinguish between a demultiplexer and decoder.	CO2	BTL 2	Understanding
18.	Compare Multiplexer with Demultiplexer.	CO2	BTL 2	Understanding

19.	Define priority encoder.		CO2	BTL 1	Remembering
20.	State the uses of encoder.		CO2	BTL 1	Remembering
21.	Mention the applications of Decoder.		CO2	BTL 2	Understanding
22.	Examine the logic diagram of 2 to 4 decoder.		CO2	BTL 2	Understanding
23.	Identify and describe the necessary components used for an 8-bit ALU.		CO2	BTL2	Understanding
24.	How to design a 1-bit comparator using basic gates.		CO2	BTL2	Understanding
	PART – B				
1.	(i)Explain the design procedure for combinational circuits. (ii) Write a note on Carry Look Ahead adders.	(6) (10)	CO2	BTL3	Applying
2.	Describe the construction of a full adder using two half adder circuits. Include a logic diagram illustrating the connections between the components.	(16)	CO2	BTL 3	Applying
3.	Discuss in detail about the following combinational circuits: (i) Half subtractor (ii) Full subtractor	 (8) (8)	CO2	BTL 3	Applying
4.	Explain the working of 4-bit parallel adder with necessary diagram and example.	(16)	CO2	BTL 3	Applying
5.	Construct a 4-bit BCD adder and with necessary illustrations.	(16)	CO2	BTL 4	Analyzing
6.	Implement the following Boolean function using 8X1 multiplexer. F(A,B,C,D)=$\bar{A}B\bar{D}$+ACD+$\bar{B}$CD+$\bar{A}\bar{C}$D	(16)	CO2	BTL 3	Applying
7.	Formulate the following Boolean function using 4 x 1 multiplexers. $F(A,B,C,D) = \sum(1,2,3,6,7,8,11,12,14)$.	(16)	CO2	BTL 4	Analyzing
8.	Realize the function F(w, x, y, z)= Σm(1,4,6,7,8,9,10,11,15) using 4 to 1 Multiplexer.	(16)	CO2	BTL 3	Applying
9.	Describe about multiplexer and Simplify the following function using 8x1 Mux F(A,B,C,D)=∑m(0,2,6,10,11,12,13)+d(3,8,14)	(16)	CO2	BTL 4	Analyzing
10.	(i) Draw and explain the working of 1:8 demultiplexer and realize it using basic gates? (ii) Implement the following functions using demultiplexer: F1(A,B,C)=∑m(0,3,7) F2(A,B,C)=$\sum m(1,2,5)$	(8) (8)	CO2	BTL 4	Analyzing
11.	Design a 3X8 Priority encoder with truth table, Boolean expression and logic diagram.	(16)	CO2	BTL 3	Applying
12.	Design a logic circuit using 4x1 Multiplexer which has four inputs A, B, C, and D. The output X of the circuit is logic 1 if two or more inputs are logic 1.	(16)	CO2	BTL 3	Applying

13.	Explain about the purpose of decoder and implement a full adder and full subtractor using decoder.	(16)	CO2	BTL 3	Applying
14.	(i) Design and implement the circuit using multiplexer which has 3 inputs (A,B,C) and one output Z. The output is HIGH, when the input is less than 3, otherwise 0. (ii) Implement the function f(w1, w2, w3) = ∑m(0, 1, 3, 4, 6, 7) by using a 3-to-8 binary decoder and an OR gate.	(8) (8)	CO2	BTL 4	Analyzing
15.	Implement the following Boolean function using an 8:1 multiplexer considering D as the input and A,B,C as selection lines : F(A, B, C, D) =AB'+BD+B'CD'	(16)	CO2	BTL 3	Applying
16.	Explain the following with necessary diagrams: (i) Full adder using multiplexer. (ii) Full subtractor using demultiplexer.	(8) (8)	CO2	BTL 3	Applying
17.	Design a 2-bit magnitude comparator with three outputs: A>B, A=B and A<B.	(16)	CO2	BTL 4	Analyzing

UNIT III SYNCHRONOUS SEQUENTIAL CIRCUITS

Flip flops – SR, JK, T, D, Master/Slave FF – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design - Moore/Mealy models, Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register

PART A

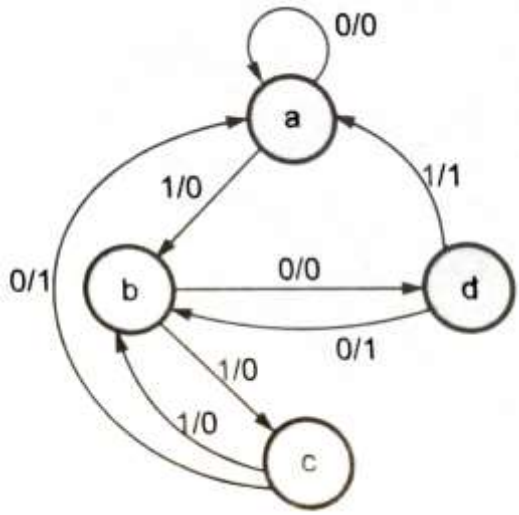
Q.No	Questions	CO	BT Level	Domain
1.	List the classification of Sequential circuits.	CO3	BTL 1	Remembering
2.	Compare combinational and sequential circuits.	CO3	BTL 2	Understanding
3.	Define a flip-flop.	CO3	BTL 1	Remembering
4.	List the types of flip-flop.	CO3	BTL 1	Remembering
5.	Differentiate between latch and flip-flop.	CO3	BTL 2	Understanding
6.	Write the excitation table for JK Flip flop.	CO3	BTL 1	Remembering
7.	Draw the state transition diagrams of flip-flops.	CO3	BTL 2	Understanding
8.	Write the characteristic equation from the truth table of SR flip-flop.	CO3	BTL 2	Understanding
9.	Transform a D flip-flop into a T flip-flop utilizing Boolean algebra and a truth table.	CO3	BTL2	Understanding
10.	Mention any two differences between the edge triggering and level triggering.	CO3	BTL 2	Understanding
11.	Derive the characteristic equation for D flip-flop.	CO3	BTL 2	Understanding
12.	Interpret the significance of state assignment.	CO3	BTL 2	Understanding

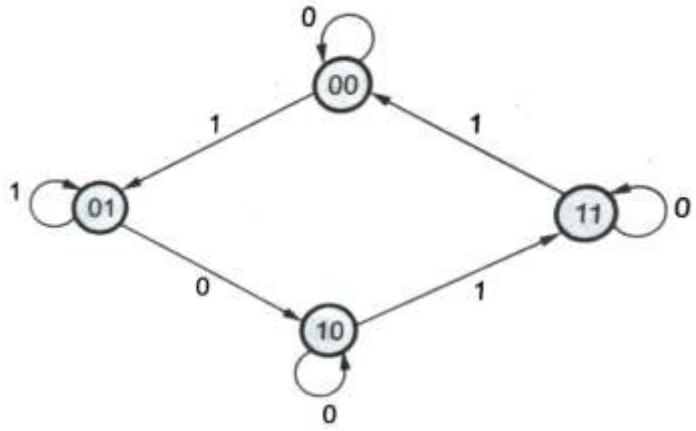
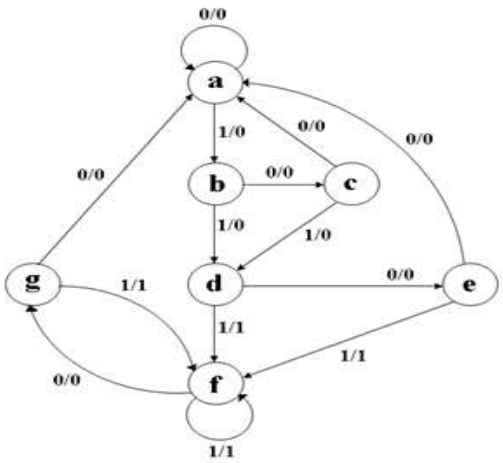
13.	Illustrate the state diagram of Mod-10 counter.		CO3	BTL 2	Understanding
14.	Draw the circuit diagram of ring Counter.		CO3	BTL 1	Remembering
15.	Determine the number of flip-flops needed to construct a binary counter that counts from 0 to 1023.		CO3	BTL2	Understanding
16.	Identify the difference between Mealy and Moore state machines.		CO3	BTL 1	Remembering
17.	What is the minimum number of flip-flops needed to design a counter of Modulus 10?		CO3	BTL 1	Remembering
18.	List out the applications of shift registers.		CO3	BTL 1	Remembering
19.	Distinguish between synchronous sequential circuits and asynchronous sequential circuits.		CO3	BTL 2	Understanding
20.	Construct a NAND based logic diagram of JK FF.		CO3	BTL1	Remembering
21.	Define universal shift register.		CO3	BTL 1	Remembering
22.	Name the types of shift registers.		CO3	BTL 1	Remembering
23.	Calculate the Q output for a J-K flip-flop with J = 1 and K = 1, given a 20 kHz clock input.		CO3	BTL 2	Understanding
24.	Sketch the 4-bit Johnson counter.		CO3	BTL 2	Understanding
	PART – B				
1.	Define flip-flop and describe the operations of various types of flip-flops. Enumerate the applications where flip-flops are used.	(16)	CO3	BTL 3	Applying
2.	Explain about JK flip-flop with truth table, characteristic equation and input & output waveforms.	(16)	CO3	BTL 3	Applying
3.	Realize SR flip-flop using D flip-flop and JK flip-flop.	(16)	CO3	BTL4	Analyzing

An ISO 9001 : 2000 Certified Institution

<table>
<tr>
<td>4.</td>
<td>(i)Describe the process involved in designing a clocked synchronous sequential circuit.

(ii) Obtain the reduced state table for the given tabulation.
<table>
<tr><th rowspan="2">Present state</th><th colspan="2">Next State</th><th colspan="2">Output</th></tr>
<tr><th>X = 0</th><th>X =1</th><th>X =0</th><th>X=1</th></tr>
<tr><td>a</td><td>F</td><td>b</td><td>0</td><td>0</td></tr>
<tr><td>b</td><td>D</td><td>c</td><td>0</td><td>0</td></tr>
<tr><td>c</td><td>F</td><td>e</td><td>0</td><td>0</td></tr>
<tr><td>d</td><td>G</td><td>a</td><td>1</td><td>0</td></tr>
<tr><td>e</td><td>D</td><td>c</td><td>0</td><td>0</td></tr>
<tr><td>f</td><td>F</td><td>b</td><td>1</td><td>1</td></tr>
<tr><td>g</td><td>G</td><td>h</td><td>0</td><td>1</td></tr>
<tr><td>h</td><td>G</td><td>a</td><td>1</td><td>0</td></tr>
</table>
</td>
<td>(8)

(8)</td>
<td>CO3</td>
<td>BTL 4</td>
<td>Analyzing</td>
</tr>
<tr>
<td>5.</td>
<td>Describe the functions with the state diagram and characteristics equation of T FF.</td>
<td>(16)</td>
<td>CO3</td>
<td>BTL 4</td>
<td>Analyzing</td>
</tr>
<tr>
<td>6.</td>
<td>Design a clocked sequential machine using T flip-flops for the following state diagram. Use state reduction if possible. Also use straight binary state assignment.
 
</td>
<td>(16)</td>
<td>CO3</td>
<td>BTL 4</td>
<td>Analyzing</td>
</tr>
<tr>
<td>7.</td>
<td>Analyze the design procedure of a MOD-5 synchronous counter using JK flip-flops and implement it.</td>
<td>(16)</td>
<td>CO3</td>
<td>BTL 4</td>
<td>Analyzing</td>
</tr>
<tr>
<td>8.</td>
<td>With the D flip-flop, design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000.</td>
<td>(16)</td>
<td>CO3</td>
<td>BTL3</td>
<td>Applying</td>
</tr>
</table>

9.	Using SR flip flops, design a counter which counts in the following sequence 000,111,1101,100,011,010,001, 000,…..	(16)	CO3	BTL3	Applying
10.	Analyze a counter to count the sequence 0,1,2,4,5,6 using SR FFs.	(16)	CO3	BTL 4	Analyzing
11.	Implement a J-K counter for the states 3, 4, 6, 7 and 3.	(16)	CO3	BTL3	Applying
12.	Explain in detail about the working of mod-3 counter with neat diagram.	(16)	CO3	BTL 3	Applying
13.	Analyze a synchronous sequential circuit using JK Flip-flop for the given state diagram. 	(16)	CO3	BTL 4	Analyzing
14.	Construct a clocked synchronous sequential logic circuit using JK flip flops for the following state diagram. Use state reduction if possible. 	(16)	CO3	BTL 3	Applying
15.	Draw the BCD ripple counter using JK flip-flop and label the logic diagram.	(16)	CO3	BTL 1	Remembering
16.	Design and implement 4-bit binary counter using D flip-flop which counts all possible odd numbers only.	(16)	CO3	BTL 4	Analyzing

17.	Analyze the operation of 4-bit SISO SIPO, PIPO and PISO shift register and draw its waveforms.	(16)	CO3	BTL 4	Analyzing

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS

Stable and Unstable states, output specifications, Pulse mode sequential circuits, cycles and races, state reduction, race free assignments, Hazards, Essential Hazards, Design of Hazard free circuits.

PART A

Q.No	Questions	CO	BT Level	Domain
1.	Mention the steps for the design of asynchronous sequential circuit.	CO4	BTL 2	Understanding
2.	Identify the design steps of asynchronous sequential circuits.	CO4	BTL 2	Understanding
3.	Compare fundamental mode and pulse mode sequential circuits	CO4	BTL 2	Understanding
4.	Define dynamic hazard. When do they occur?	CO4	BTL 1	Remembering
5.	What are pulse mode circuits?	CO4	BTL 1	Remembering
6.	Write the difference between stable and unstable state.	CO4	BTL 2	Understanding
7.	Specify the significance of state assignment.	CO4	BTL 2	Understanding
8.	Outline the role of asynchronous sequential circuit in digital design.	CO4	BTL 1	Remembering
9.	State the objective of state assignment asynchronous circuit.	CO4	BTL 2	Understanding
10.	Define Hazards. How it can be avoided?	CO4	BTL 1	Remembering
11.	Compare the Static-0 and Static-1 hazards.	CO4	BTL 2	Understanding
12.	Examine the critical race condition in asynchronous sequential circuits with an example.	CO4	BTL 2	Understanding
13.	Mention the causes of essential Hazard.	CO4	BTL 2	Understanding
14.	Distinguish between critical race and non-critical race.	CO4	BTL 2	Understanding
15.	Outline the characteristics of critical race.	CO4	BTL 2	Understanding
16.	List the different techniques used in State assignment.	CO4	BTL 1	Remembering
17.	Differentiate synchronous and asynchronous sequential circuits.	CO4	BTL 1	Remembering
18.	How dynamic hazards can be avoided?	CO4	BTL 2	Understanding
19.	Summarize the methods for critical-race free state assignment.	CO4	BTL 1	Remembering
20.	Construct a K-map to remove static-1 hazard.	CO4	BTL 2	Understanding
21.	Classify the modes of operation of sequential logic circuit.	CO4	BTL 2	Understanding

22.	Examine the preference given to Hazard free design.		CO4	BTL 1	Remembering
23.	Write the difference between cycles and races.		CO4	BTL 1	Remembering
24.	Mention the effects due to Hazards in digital circuit.		CO4	BTL 2	Understanding
	PART – B				
1.	Analyze an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 and C moves from 1 to 0. Otherwise, the output is 0.	(16)	CO4	BTL 4	Analyzing
2.	List the types of hazards. Check whether the following circuit contains a hazard or not $Y = X_1X_2 + X_2'X_3$. If the hazard is present, show the removal of hazard.	(16)	CO4	BTL 3	Applying
3.	An asynchronous sequential circuit is described by the following excitation and output function. Y= X1X2+(X1+X2) Y, Z=Y. (i) Construct the logic diagram. (ii) Develop the transition table and output map. (iii) Identify the behavior of the circuit	 (4) (6) (6)	CO4	BTL 3	Applying
4.	Construct hazard free realization for the following Boolean function. F (A, B, C, D) = ∑m (1,5,6,7) using AND- OR gate network.	(16)	CO4	BTL 3	Applying
5.	(i) Distinguish the design procedure for an asynchronous sequential circuit. (ii) Analyze the state table of serial binary adder with neat diagram.	(10) (6)	CO4	BTL 4	Analyzing
6.	Explain how to design a circuit that has no static hazards and implement the Boolean function F(A,B,C,D) = Σ (0,2,6,7,8,10,12) using AND-OR logic.	(16)	CO4	BTL 3	Applying
7.	Identify the challenges encountered in an asynchronous sequential circuit and elaborate on two specific issues in detail.	(16)	CO4	BTL 3	Applying
8.	(i) Illustrate in detail about Races. (ii) Explain the different methods of state assignment.	(8) (8)	CO4	BTL 3	Applying
9.	Discuss hazards in digital circuits, including static hazards, dynamic hazards, and essential hazards, supported by clear diagrams.	(16)	CO4	BTL 3	Applying
10.	Examine the analysis procedure for asynchronous sequential circuits with necessary illustrations.	(16)	CO4	BTL 4	Analyzing
11.	Illustrate about different hazards that occur in sequential circuits and also about the way to eliminate them.	(16)	CO4	BTL 3	Applying
12.	Select the methods of Race Free State assignment and explain in detail.	(16)	CO4	BTL 3	Applying

13.	Design an Asynchronous sequential circuit with input A and B and an output Y. Initially at any time if both the inputs are 0, the output, Y=0. When A or B = 1, Y =1. When the other input also become 1, Y=0. The output stays at 0 until circuit goes back to initial state.	(16)	CO4	BTL 4	Analyzing
14.	Analyze in detail about state table, stable and unstable state with examples.	(16)	CO4	BTL 4	Analyzing
15.	How the Hazard free circuit is designed? Explain with suitable example.	(16)	CO4	BTL 3	Applying
16.	Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is one, input X is transferred to Z. When Y is zero, the output does not change for any change in X.	(16)	CO4	BTL 4	Analyzing
17.	An Asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit is as follows: $Y1 = x_1x_2+x_1y_2+x_2y_2$ $Y2 = x_2+x_1y_1y_2+x_1y_1$ $Z = x_2+y_1$. (i) Draw the logic diagram. (ii) Derive transition table and output map.	(16)	CO4	BTL 3	Applying

UNIT - V MEMORY DEVICES AND INTRODUCTION TO HDL PROGRAMMING

Basic memory structure- ROM-PROM-EPROM-EEPROM-EAPROM, RAM – Static and Dynamic RAM- Programmable Logic Devices-Programmable Logic Array (PLA) – Programmable Array Logic (PAL). Introduction to HDL: Behavioral – data flow, and algorithmic and structural description, Examples for Combinational and Sequential circuits-Adders-Multiplexer-demultiplexer-Encoder-Decoder-Flipflops-Shift registers.

PART A

Q.No	Questions	CO	BT Level	Domain
1.	Write the difference between ROM and RAM.	CO5	BTL 1	Remembering
2.	Distinguish between volatile and non-volatile memory.	CO5	BTL 2	Understanding
3.	Mention the advantages of DRAM cell over SRAM cell.	CO5	BTL 2	Remembering
4.	What is programmable logic array?	CO5	BTL 1	Remembering
5.	A certain memory has a capacity of 32k x 16. How many bits are there in each word? How many words are being stored and how many memory cells does this memory contain?	CO5	BTL 2	Understanding
6.	What is memory decoding?	CO5	BTL 1	Remembering
7.	Draw the circuitry used to realize 2-bit multiplier using ROM.	CO5	BTL 2	Understanding
8.	Implement the XOR function using a Programmable Read-Only Memory.	CO5	BTL 2	Understanding
9.	List the advantages of EEPROM over EPROM.	CO5	BTL 2	Understanding

10.	How programmable logic devices are classified?		CO5	BTL 2	Understanding
11.	Distinguish between PAL and PLA.		CO5	BTL 2	Understanding
12.	List the operators used in Verilog HDL.		CO6	BTL 1	Remembering
13.	What are the primitive gates supported by Verilog HDL?		CO6	BTL 1	Remembering
14.	Express the modeling styles used in Verilog HDL along with the way they are realized.		CO6	BTL 2	Understanding
15.	Write the Verilog HDL code for half subtractor in data flow model.		CO6	BTL 1	Understanding
16.	Differentiate logical AND and bitwise AND operation in Verilog HDL with example.		CO6	BTL 2	Understanding
17.	Summarize the top-down and bottom-up design followed in Verilog HDL.		CO6	BTL 2	Understanding
18.	Write the Verilog HDL code for D-Latch.		CO6	BTL 1	Remembering
19.	Mention the conditional and unconditional loops supported in Verilog HDL.		CO6	BTL 2	Understanding
20.	Outline the Verilog code for T-flip-flop.		CO6	BTL 2	Understanding
21.	Define the specification of module.		CO6	BTL 1	Remembering
22.	List examples for system task in Verilog.		CO6	BTL 2	Understanding
23.	Differentiate blocking from nonblocking assignments.		CO6	BTL 2	Understanding
24.	Outline about Equality operators in Verilog.		CO6	BTL 2	Understanding
	PART – B				
1.	Explain the classification of semiconductor memories in detail.	(16)	CO5	BTL 3	Applying
2.	Differentiate static and dynamic RAM. Draw the circuits of one cell of each and explain its working principle.	(16)	CO5	BTL 3	Applying
3.	Derive a combinational circuit defined by the function, F1 = AB'C'+AB'C+ABC and F2 = A'BC+AB'C+ABC using PLA with minimal AND gates.	(16)	CO5	BTL 3	Applying
4.	Illustrate the simplified form of Boolean functions, F1(x, y, z) = ∑ (0, 1, 3, 5); F2(x, y, z) = ∑ (3, 5, 7) and obtain its circuit using 3×4×2 PLA.	(16)	CO5	BTL 4	Analyzing
5.	Obtain the circuitry used to realize the following functions using PAL. F1(A, B, C) = ∑ (1, 2, 4, 6); F2(A, B, C) = ∑ (0, 1, 6, 7); F3(A, B, C) = ∑ (1, 2, 3, 5, 7).	(16)	CO5	BTL 4	Analyzing
6.	Analyze the design of BCD to Excess 3 code converter using PLA. Illustrate the design detail along with the PLA program table?	(16)	CO5	BTL 4	Analyzing
7.	List and describe the various categories of operators available in Verilog HDL, including their symbols.	(16)	CO6	BTL 3	Applying

8.	Implement Verilog HDL code for full adder using data flow modeling, and behavioral modelling styles with necessary illustration.	(16)	CO6	BTL 3	Applying
9.	Apply data flow modeling style in Verilog HDL to code for 4:1 multiplexer along with detailed explanation.	(16)	CO6	BTL 3	Applying
10.	Design a 3-bit magnitude comparator and write the Verilog HDL code to realize it using structural modelling.	(16)	CO6	BTL 3	Applying
11.	Write the Verilog HDL code for 4-bit synchronous counter.	(16)	CO6	BTL 4	Analyzing
12.	Assume any one modeling style to describe a 3 to 8 decoder in Verilog HDL.	(16)	CO6	BTL 4	Analyzing
13.	Write the Verilog code to construct a 4-bit ripple carry adder with necessary diagrams.	(16)	CO6	BTL 4	Analyzing
14.	Sketch the following code converters and derive the circuitry used to realize them using PROM device. (i) Binary to gray code (ii) Gray to Binary code	 (8) (8)	CO6	BTL 3	Applying
15.	Construct a combinational circuit using ROM that accepts a three-bit binary number and outputs a binary number equal to the square of the input number.	(16)	CO5	BTL 4	Analyzing
16.	Design a four-bit asynchronous decade counter and write the Verilog code with neat diagram.	(16)	CO6	BTL 4	Analyzing
17.	Using 4×3×4 PALS, determine the circuit used to realize the following Boolean functions. (i) W(A,B,C,D) = ∑m (0,2, 6,7,8,9,12,13) (ii) X(A,B,C,D) = ∑m (0, 2, 6, 7, 8, 9, 12, 13, 14) (iii)Y(A, B, C, D) = ∑m (2, 3, 8, 9, 10, 12, 13) (iv) Z(A,B,C,D) = ∑m(1, 3, 4, 6, 9, 12, 14)	(16)	CO5	BTL 3	Applying