SRM VALLIAMMAI ENGINEERING COLLEGE

S.R.M NAGAR, KATTANKULATHUR-603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LABORATORY MANUAL

Regulation-2023

EC3367 ELECTRONICS CIRCUITS DESIGN LABORATORY

ACADEMIC YEAR: 2025-2026 (Odd)

II YEAR - III SEMESTER

Prepared by

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Course Coordinator

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SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION OF THE INSTITUTE

Educate to excel in social transformation

MISSION OF THE INSTITUTE

- To contribute to the development of human resources in the form of professional engineers and managers of international excellence and competence with high motivation and dynamism, who besides serving as ideal citizen of our country will contribute substantially to the economic development and advancement in their chosen areas of specialization.
- To build the institution with international repute in education in several areas at several levels with specific emphasis to promote higher education and research through strong institute-industry interaction and consultancy.

VISION OF THE DEPARTMENT

To excel in the field of electronics and communication engineering and to develop highly competent technocrats with global intellectual qualities.

MISSION OF THE DEPARTMENT

M1: To train the students with the state-of-art technologies and to develop innovative solutions to cater to the societal needs

M2: To orient the students towards global career with universal moral values and professional ethics

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PROGRAM OUTCOMES

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOME (PSOs)

PSO1: Ability to apply the acquired knowledge of basic skills, mathematical foundations, principles of electronics, modeling and design of electronics based systems in solving engineering problems.

PSO2: Ability to understand and analyze the interdisciplinary problems for developing innovative sustained solutions with environmental concerns.

EC3367 ELECTRONICS CIRCUITS DESIGN LABORATORY

L T P C
0 0 3 1.5

OBJECTIVES:

To impart knowledge on the following topics

1. To learn the characteristics of PN Junction diode.
2. To learn the characteristics of Zener diode.
3. To understand the operation of rectifiers and filters.
4. To study and Testing of BJT and FET amplifiers.
5. To Design of Operation of power amplifiers.
6. To applying knowledge develop an analog application circuits.

LIST OF EXPERIMENTS

1. Characteristics of PN Junction Diode and Zener diode
2. Full Wave Rectifier with Filters.
3. Design of Zener diode Regulator
4. BJT Common Emitter input-output Characteristics.
5. FET Drain current and Transfer Characteristics.
6. Frequency response of CE and CS amplifiers.
7. Frequency response of CC and CD amplifiers
8. Frequency response of Cascade Amplifier.
9. CMRR measurement of Differential Amplifier.
10. Class A Power Amplifier.
11. Class C Power Amplifier.

TOPIC BEYOND SYLLABUS

1. Darlington Amplifiers.
2. Determination of Bandwidth of single stage and multistage amplifiers using BJT.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

On completion of the course, the student will be able to

1. Study the characteristics of PN Junction Diode.
2. Understand the operation of Zener diode.
3. Design and Testing Full Wave Rectifier with Filters.
4. Evaluate AC parameter of BJT and FET amplifiers.
5. Illustrate the Operation of power amplifiers.
6. Develop an analog application circuits.

COURSE OUTCOMES - PROGRAM OUTCOMES MATRIX

CO	PO												PSO	
	1	2	3	4	5	6	7	8	9	10	11	12	1	2
EC3367.1	3	3	2	3	2	1	-	-	3	-	-	2	2	1
EC3367.2	3	3	2	3	2	1	-	-	3	-	-	2	2	1
EC3367.3	3	2	2	3	1	1	-	2	3	-	-	2	3	2
EC3367.4	3	3	2	3	3	2	2	2	3	-	-	2	3	2
EC3367.5	3	2	2	3	2	2	2	2	3	-	-	2	3	2
EC3367.6	3	2	3	3	3	2	2	2	3	3	2	2	3	3
AVG	3	3	2	3	2	2	2	2	3	3	2	2	3	2

LAB Requirements for a Batch of 30 students

1. CRO/DSO (30 MHz) – 15 Nos.
2. Signal Generators / Function Generators (3 MHz) – 15 Nos
3. Dual Generator Power Supplies (0-30 V) – 15 Nos
4. Bread Board – 15 Nos.
5. SPICE simulator

LIST OF EXPERIMENTS

CYCLE I

1. 1.Characteristics of PN Junction Diode and Zener diode
2. Full Wave Rectifier with Filters.
3. Design of Zener diode Regulator
4. BJT Common Emitter input-output Characteristics.
5. FET Drain current and Transfer Characteristics.

CYCLE II

6. Frequency response of CE and CS amplifiers.
7. Frequency response of CC and CD amplifiers
8. Frequency response of Cascade Amplifier.
9. CMRR measurement of Differential Amplifier.
10. Class A Power Amplifier.
11. Class C Power Amplifier.

TOPIC BEYOND SYLLABUS

12. Darlington Amplifiers.
13. Determination of Bandwidth of single stage and multistage amplifiers using BJT.

INDEX

Exp. No.(1a) CHARACTERISTICS OF PN JUNCTION DIODE

AIM:

To determine the VI characteristics of PN Diode.

APPARATUS REQUIRED:

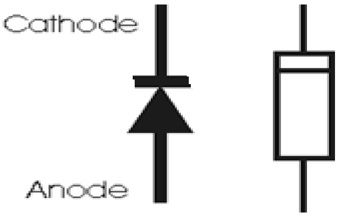
S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30)V	1
2	Ammeter	(0-5)mA, (0-25)mA	1 1
3	Voltmeter	(0-10)V (0-1)V	1 1
4	Connecting wires	-	Required
5	Bread Board		1
6	Resistors	1KΩ	1
7	Diode- PN	BY127	1

THEORY:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion Layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit.The difference of potential across the depletion layer is called the barrier potential. At 2.5degree the barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

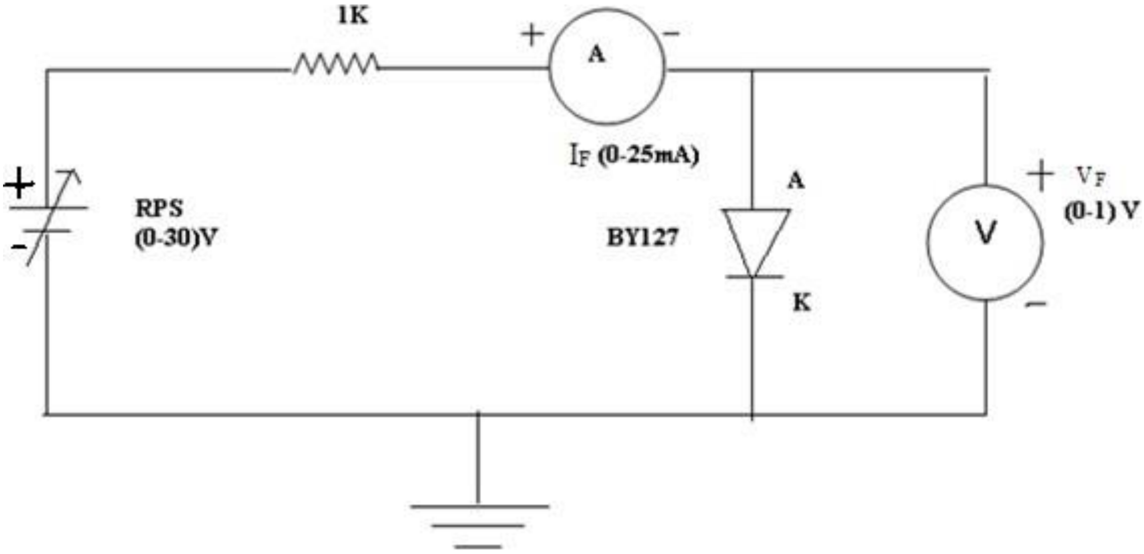
When the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannotcross the junction and the diode does not conduct. But there will be a leakage current due tominority carrier. When diode is forward biased, resistance offered is zero, and when reversebiased resistance offered is infinity. It acts as a perfect switch.

PIN DIAGRAM:

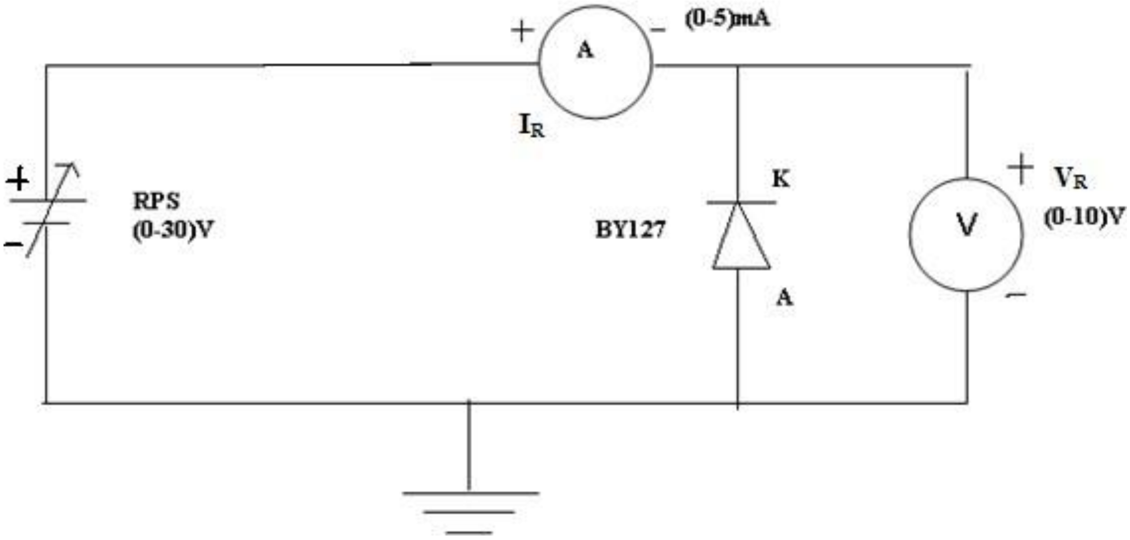


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

TABULATION:

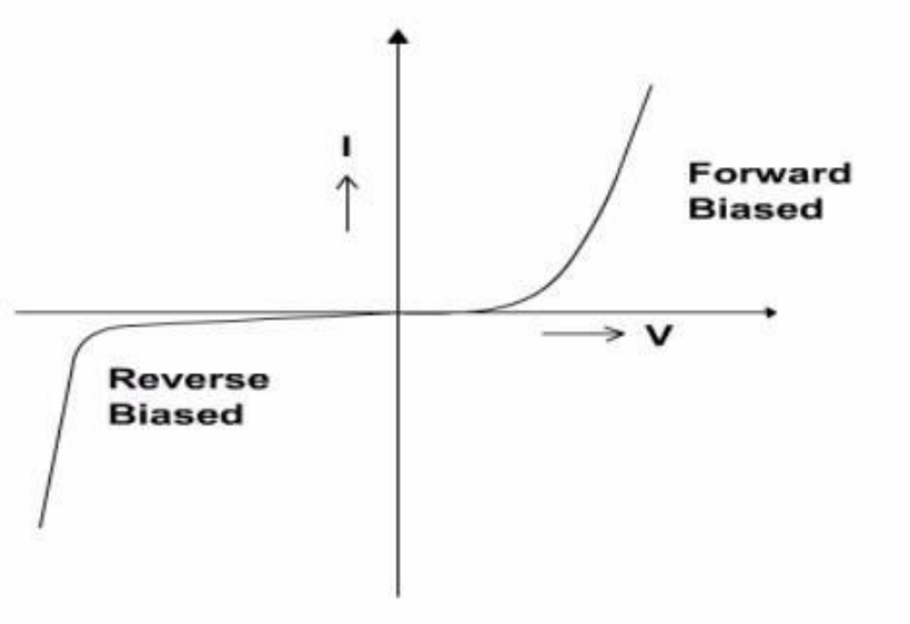
FORWARD BIAS:

V_f(volts)	**I_f(mA)**

REVERSE BIAS:

V_r(volts)	**I_r(mA)**

MODEL GRAPH:



REVIEW QUESTIONS:

1. What is a semiconductor?
2. Write the Diode current Equation.
3. What is the value of V_t at room temperature
4. What is meant by forward bias
5. What is meant by reverse bias?
6. How a PN junction is formed?
7. In what way the width of region can be varied?
8. What is potential barrier?
9. In forward bias condition the current condition is due to?
10. What is reverse saturation current Ico?

Result:

Thus the characteristics of PN Junction diode were drawn**.**

Exp. No.(1b) CHARACTERISTICS OF ZENER DIODE

AIM:

To determine the VI characteristics of Zener Diode

APPARATUS REQUIRED:

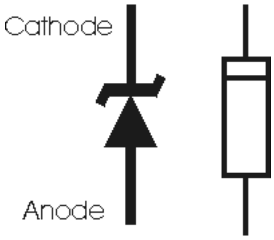
S.No	Name	Range	Type	Qty
1	RPS	(0-30)V		1
2	Ammeter	(0-30) mA		1
3	Voltmeter	(0-10)V (0-1)V		1 1
4	Connecting wires	-		As Required
5	Bread Board			1
6	Resistors	1KΩ		1
7	Diode- Zener	FZ 5V6/ FZ 6V2		1

THEORY:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

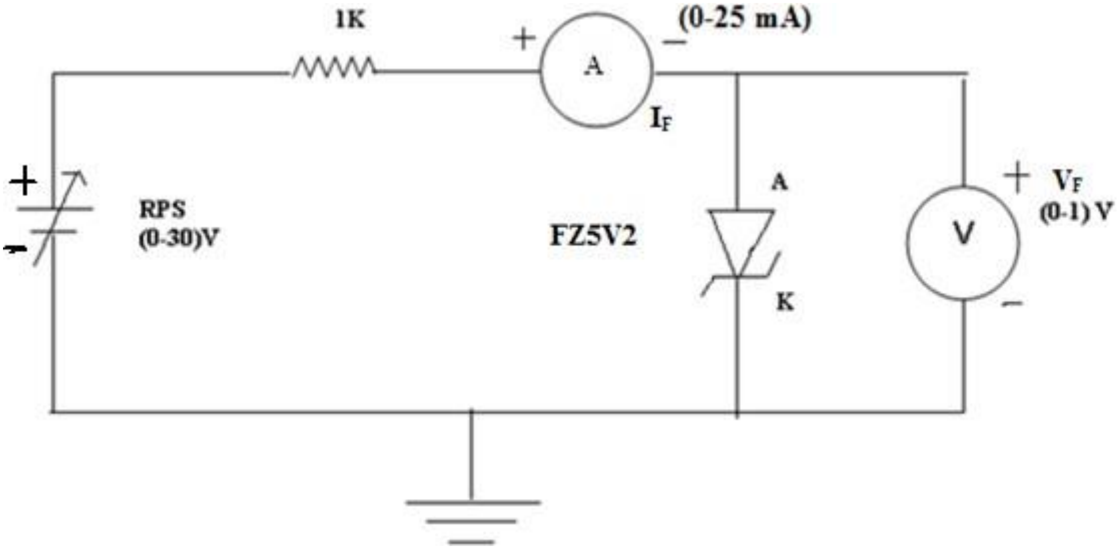
In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

PIN DIAGRAM:

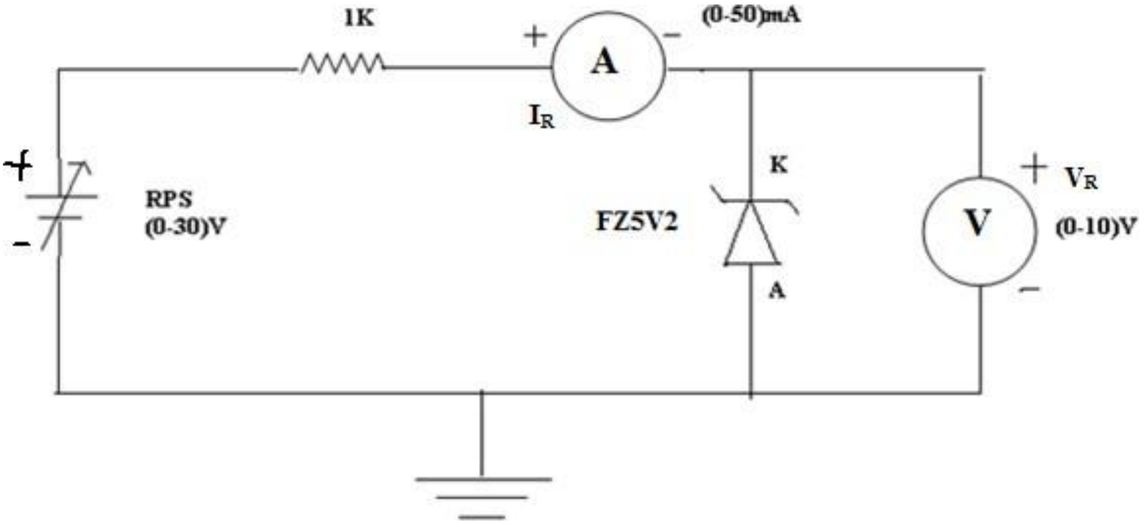


CIRCUIT DIAGRAM:

FORWARD BIAS:



REVERSE BIAS:



PROCEDURE:

FORWARD BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

REVERSE BIAS:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

TABULAR COLUMN:

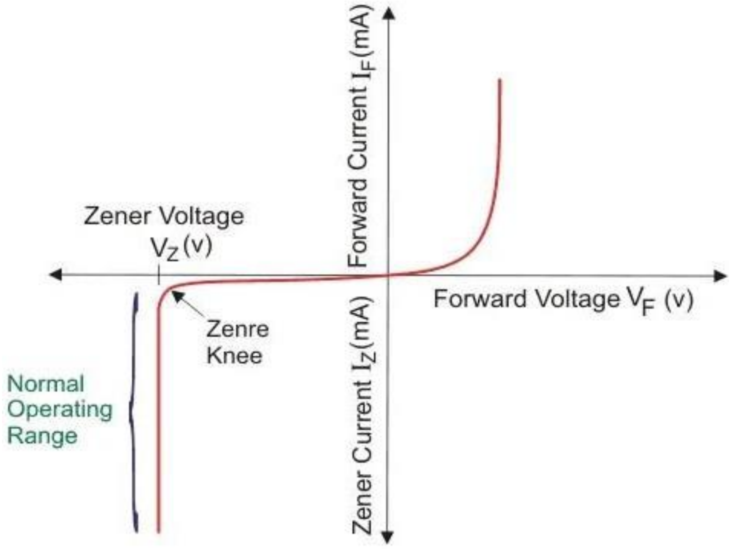
FORWARD BIAS:

V_f(volts)	I_f(mA)

REVERSE BIAS:

V_r(volts)	I_r(mA)

MODEL GRAPH



Review Questions:

1. How the name of the Zener came?
2. What is cause of reverse breakdown?
3. What is zener voltage?
4. Write the Symbol for the Zener diode.
5. What are the different types of breakdowns in semiconductor junctions?
6. What is the difference between p-n Junction diode and zener diode?
7. Can we use Zener diode as a switch?
8. Explain working of a Zener Diode.
9. What is the max value of voltage of Zener breakdown devices?
10. What is cause of reverse breakdown?

RESULT:

Thus the characteristics of Zener diode were drawn**.**

Exp.No:2 FULL WAVE RECTIFIER

AIM:

To construct full wave rectifier and to calculate ripple factor and regulation.

APPARATUS REQUIRED:

S,No	Name of the Component	Specification/Rating	Quantity(in number)
1.	Transformer	230 V / (9-0-9)	1
2.	Diode	IN4007	2
3.	Decade Resistance Box	(1KΩ-10 KΩ)	1
4.	Capacitor	100µF	1
5.	Voltmeter	(0-20V)MC	2
6	Multimeter	-	1
7.	Bread board, connecting wires	-	1, few

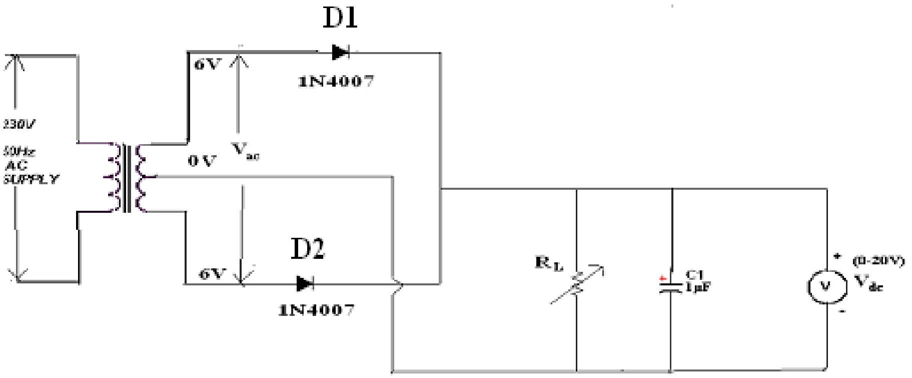
THEORY:

The full wave rectifier conducts for both the positive and negative half cycles of the input AC supply. In order to rectify both the half cycles of the AC input, two diodes are usedin this circuit. The diodes feed a common load resistance with the help of a centre tapped transformer. The rectifier's DC output is obtained across the load. The DC load current for the full wave rectifier is twice that of the half wave rectifier. The efficiency of full wave rectification is twice that of half wave rectification. The ripple factor for the full wave rectifieris less compared to the half wave rectifier**.**

PROCEDURE:

1. Connect the circuit as per the circuit diagram. For full wave rectifier without filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input. Switch on the supply.
3. Vary the DRB and note down the corresponding voltmeter and ammeter reading.
4. Calculate the ripple factor and regulation.
5. Repeat the above steps for full wave rectifier with filter.

FULLWAVE RECTIFIER WITH CAPACITIVE FILTER:



FULL WAVE RECTIFIER WITH CAPACITIVE FILTER

S.No.	V_{pp}	Time period	V_m	V_{ripple}	V_{dc}

FORMULA USED:

Ripple Factor = $\frac{V_{ac}}{V_{dc}}$ and % Regulation = $\frac{V_{NL}-V_{FL}}{V_{NL}} \times 100\%$

Review Questions:

1. What is a Rectifier?
2. What are types and its difference?
3. What is ripple factor?
4. What is meant by regulation?
5. What is a filter?
6. What is a full wave rectifier?
7. What is the value of the ripple factor of a full wave rectifier?
8. What is the maximum efficiency that can be obtained in a full wave rectifier?
9. What is the advantage of full wave rectifier over half wave rectifier?
10. Define Transformer utilization factor.

RESULT:

Thus the full wave rectifier was constructed and the ripple factor and percentage regulation were calculated

Ripple factor:

% Regulation:

Exp.No.3 DESIGN OF VOLTAGE REGULATOR USING ZENER DIODE

AIM:

To study the Zener Diode as Voltage Regulator.

APPARATUS REQUIRED:

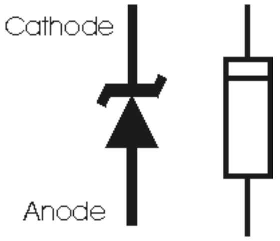
S.No	Name	Range	Qty
1	RPS (Regulated power supply)	(0-30)V	1
2	Ammeter	(0-30) mA	1
3	Voltmeter	(0-10)V (0-1)V	1 1
4	Connecting wires		As Required
5	Bread Board		1
6	Resistors	1KΩ	1
7	Diode- Zener	FZ 5V6/ FZ 6V2	1

THEORY:

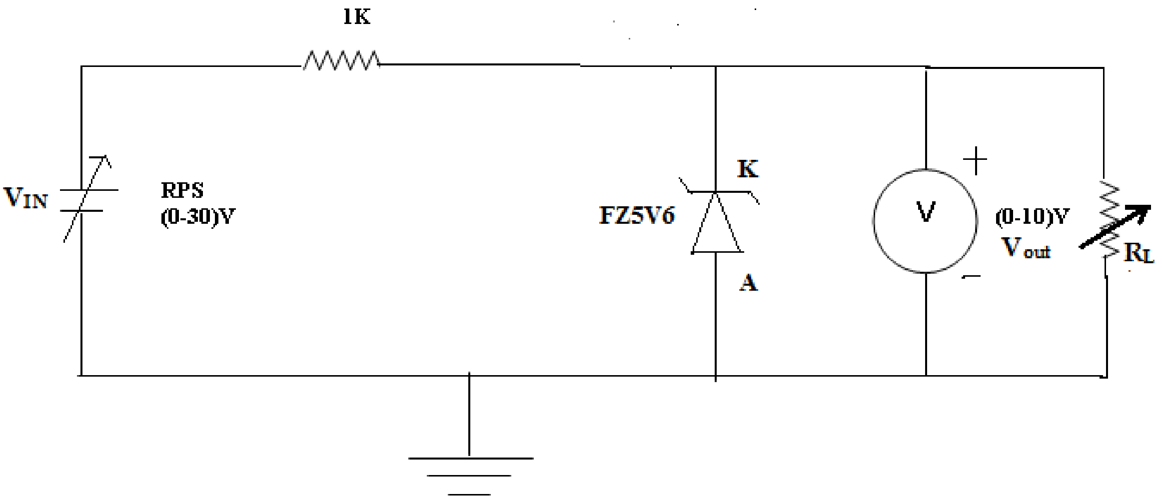
Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased,they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.In the reverse direction, the operation of a Zener diode is quite different to an ordinarydiode.

For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curvesfor a Zener diode, it can be seen that the voltage is almost constant regardless of the currentcarried. This means that a Zener diode provides a stable and known reference voltage. Hencethey are used as Voltage regulators.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



PROCEDURE:

1. The connections are made as per the circuit diagram.
2. Keep Load resistance R_L constant.
3. Vary the Input voltage and note down the corresponding output voltage.
4. Now keep voltage constant vary the $R_L$and note down the voltmeter corresponding reading.
5. Plot the respective regulations graph.

TABULAR COLUMN:

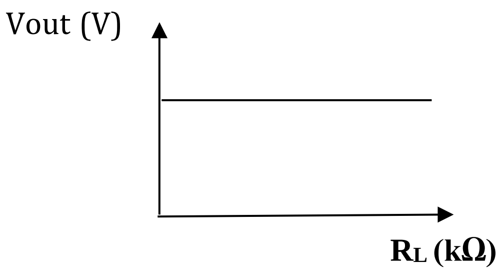
LOAD REGULATION:

R_L (kΩ)	Vout (V)

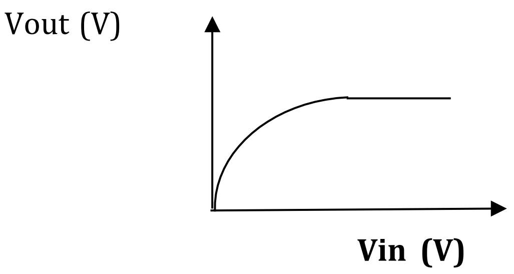
LINE REGULATION:

Vin (V)	Vout (V)

MODEL GRAPH



LOAD REGULATION



LINE REGULATION

Review Questions:

1. How Zener diode acts as a voltage regulator?
2. Explain working of a Zener Diode.
3. Explain Zener Breakdown.
4. Explain avalanche breakdown.
5. Compare Zener and avalanche Breakdown.
6. What are the applications of Zener diode?
7. What is voltage regulator?
8. What is cut-in-voltage?
9. What is break down voltage?
10. Draw characteristics of Zener Diode under Forward & Reverse Bias Conditions

RESULT:

Thus the Zener diode as a Voltage Regulator were studied**.**

Exp.No.4 BJT COMMON EMITTER INPUT-OUTPUT CHARACTERISTICS

AIM:

To plot the transistor characteristics (INPUT & OUTPUT) of CE configuration.

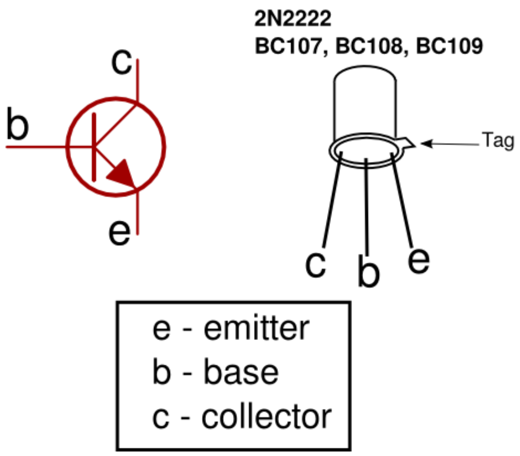
APPARATUS REQUIRED:

S.No.	COMPONENTS	SPECIFICATION	QTY
1	Transistor BC 107	Max Rating : 50V 1A, 3W	1
2	Resistors	10KΩ,100Ω	2
3	RPS (Regulated power supply)	(0-30) V	1
4	Voltmeters	(0-10) V (0-1) V	1 1
5	Ammeters	(0-30) mA (0-100)µA	1 1
6	Bread board		1
7	Connecting wires		Required

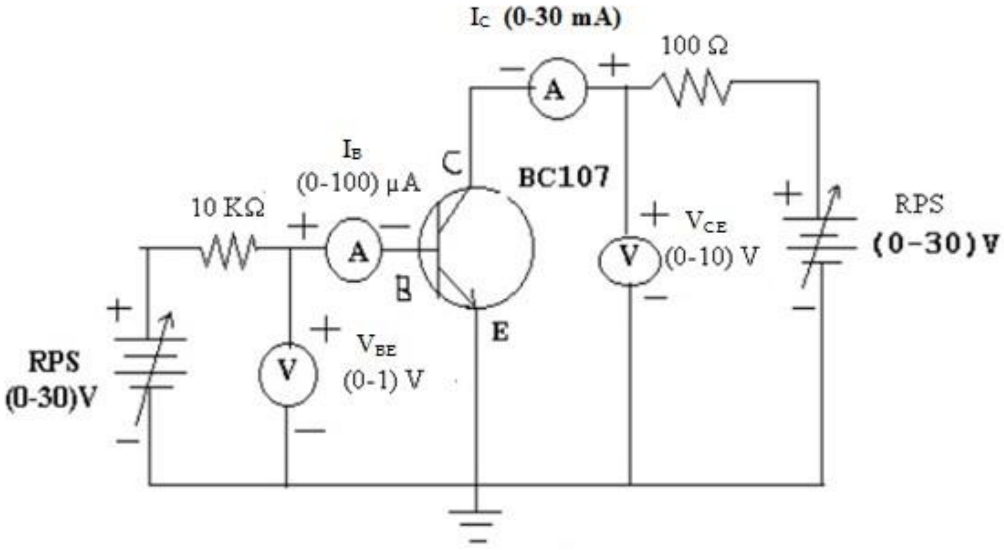
THEORY:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layerof p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majorityand minority carriers it is called bipolar device. In CE configuration, Emitter is common toboth the Emitter and Base.

PIN DIAGRAM OF BC107



CIRCUIT DIAGRAM:



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_B, where V_{CE} is constant

Output Characteristics:

Voltage across Collector Emitter junction V_{CE} vs I_C where I_B is constant.

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CE} is kept constant (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_B values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_B, where V_{CE} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_B is kept constant, V_{CE} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{CE} and Ic for a constant I_B.

TABULATION:

Input Characteristics:

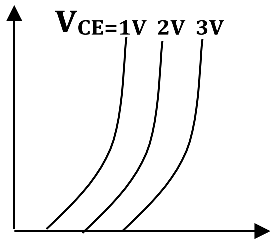
V_{CE} = V		V_{CE} = V	
V_{BE}(V)	I_B (μA)	V_{BE}(V)	I_B(μA)

Output characteristics:

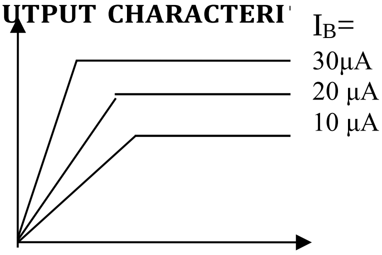
I_B = μA		I_B = μA	
V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C(mA)

MODEL GRAPH:

INPUT CHARACTERISTICS



OUTPUT CHARACTERI



Review Questions:

1. Explain the operation of CE configuration
2. Determine the output resistance and input resistance
3. What is the relation between α, β and γ?
4. Define current gain in CE configuration?
5. Why CE configuration is preferred for amplification?
6. List the current components of BJT in CE configuration
7. What is Early Effect?
8. Why the doping of collector is less compared to emitter?
9. What do you mean by “reverse active”?
10. What is the difference between CE and Emitter follower circuit?

RESULT:

Thus the input and output characteristic of BJT in Common Emitter mode is drawn.

EXP.NO.5 FET DRAIN CURRENT AND TRANSFER CHARACTERISTICS

AIM:

To plot the drain and transfer characteristics of JFET & to find drain resistance, transconductance, amplification factor, drain saturation current I_{DSS} and Pinch off voltage.

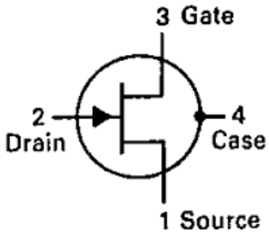
APPARATUS REQUIRED:

S.No.	Components	Specification	Qty
1	FET	BFW10 I_{dss}> 8 mA, Vp<8V	1
2	Resistors	1KΩ	1
3	RPS (Regulated dual power supply)	(0-30)V	1
4	Voltmeters	(0-10)V, (0-25)V	1
5	Ammeters	(0-25) mA	1
6	Bread board		1
7	Connecting wires		Required

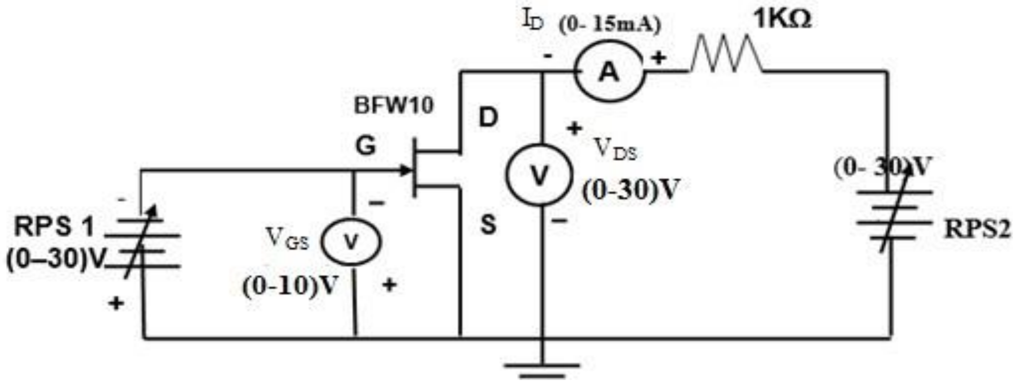
THEORY:

Field effect transistor is a semiconductor device that depends for its operation on the control of current by an electric field. Its operation depends on the flow of majority carriers only. It is therefore a unipolar device. It exhibits a high input resistance. An N- channel JFET consists of a N-type bar is sandwiched between two heavily doped Persians. Due to the concentration gradient, the depletion region formed. On both sides of the semiconductor bar the ohmic contacts are made. One terminal is called source & other is called drain. Both the p-type regions are connected together.

PIN DIAGRAM OF BFW10



CIRCUIT DIAGRAM



DESCRIPTION:

DRAIN CHARACTERISTICS

INPUT: Drain voltage V_{DS} is varied insteps of 1V, V_{GS} is kept

constantOUTPUT: Drain current I_D

TRANSFER CHARACTERISTICS

INPUT: Gate – source voltage V_{GS} is varied, Drain –source voltage V_{DS} is kept constant

OUTPUT**:** Drain current I_D

PROCEDURE:

Drain Characteristics:

1. Connections are made as per the circuit diagram.
2. Gate –source voltage V_{GS} is kept constant (say –1v), drain voltage V_{DS} is varied insteps of 1v and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{GS}= -2v, 0v.
4. The graph is plotted V_{DS} and I_D for a constant V_{GS}.
5. The drain resistance is found from the graph

$$r_d = \Delta V_{DS} / \Delta I_D$$

Transfer Characteristics:

1. Connections are made as per the circuit diagram.
2. Drain –source voltage V_{DS} is kept constant (say 5v), the gate – source voltage V_{GS} is varied insteps of 1v (-VE voltage) and the corresponding drain current I_D valuesare tabulated.
3. The above procedure is repeated for V_{DS} = 10v, 15v,
4. Graph is plotted between V_{GS} and I_D for a constant V_{DS}.
5. The trans conductance is found from the graph

$$g_m = \Delta I_D/\Delta V_G$$

TABULAR COLUMN:

Drain characteristics

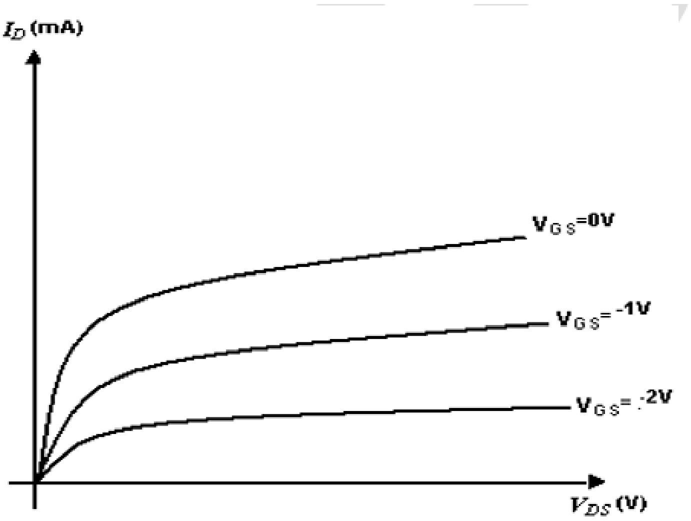
V_{GS} = V		**V_{GS} = V**	
V_{DS} (V)	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**

Transfer characteristics

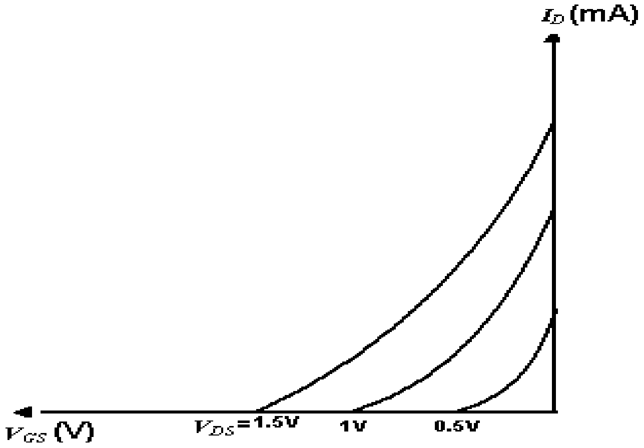
V_{DS} = V		**V_{DS}** =V	
V_{GS} (V)	**I_D (mA)**	**V_{GS} (V)**	**I_D (mA)**

MODEL GRAPH:

DRAIN CHARACTERISTICS:



TRANSFER CHARACTERISTI



CALCULATION

Transconductance g_m = $\Delta I_D / \Delta V_G$

Drain resistance r_d = $\Delta V_{DS} / \Delta I_D$

Amplification factor μ = $g_m r_d$

Review Questions:

1. Why it is called by name “field effect transistor”?
2. What are the advantage of FET OVER BJT?
3. What are the disadvantages of FET?
4. What is the significance of arrowhead in FET symbol?
5. Why FET is called unipolar device?
6. Define VVR.
7. Why MOSFET is preferred than FET?
8. What are the differences between FET & MOSFET?
9. What are the applications of FET?
10. Why FET is called us voltage-controlled device?

RESULT:

Thus the drain and transfer for characteristics of JFET is drawn.

Drain resistance r_d =

Trans conductance g_m =

Amplification factor =

Exp. No: (6a) FREQUENCY RESPONSE OF CE AMPLIFIER

AIM:

To design a BJT Common Emitter (CE) Amplifier using voltage divider bias (self-bias) bypassed emitter resistor to

- Measurement of gain
- Plot the frequency response & Determination of Gain Bandwidth Product.

COMPONENTS REQUIRED:

S.NO	Name of the Component	Specification/Range	Quantity
1.	Transistor	(BC547)	01
2.	Resister	180KΩ, 39KΩ, 1KΩ, 3.9KΩ, 120Ω, 470 Ω, 2.2 KΩ, DRB	Each 1
3.	Capacitor	4.7μF, 10 μF	01,02
4.	Function Generator	2MHz	01
5.	RPS	(0-30)V	01
6.	CRO	30MHz	01
7.	Bread Board		01
8.	Connecting Wires	Single stand	few

THEORY:

In CE amplifier, the input is applied between Base & Emitter and the output is taken between Collector & Emitter. As Emitter is common to both input & output, hence the name Common Emitter amplifier.

When V_{in} goes +ve, V_b increases. This increases I_b and hence I_c. This increases the voltage drop at Rc & Vc decreases. Thus whenever there is a +ve swing at the input, there is a – ve swing at the Collector. Similarly, whenever there is a -ve swing at the input, there is a +ve swing at the Collector. Or, there is 180 degree phase difference between input & output voltages. A small change at the input gives a large change at the output resulting in amplification.

In RC coupled CE amplifier, Resistances R_1, R_2 and R_E set the proper operating point for the CE amplifier. Input Capacitor C1Couples the signal to the base of the transistor blocks DC and allows only AC Signal for Amplification & thereby ensures Constant biasing conditions.

DESIGN

Given $A_V = 10$, $h_{fe} = 300$, $V_{CC} = 10V$,
$I_{CQ} = 2mA$ and $f = 200Hz$

R_1=180KΩ, R_2=39KΩ, R_E=470Ω, R_C=2.2KΩ, R_L=120Ω, R_S=0Ω, C_1=10µF, C_2= 4.7µF, C_E=10µF.Use BC547

Emitter Bypass Capacitor, C_E

– Provides a Low reactance path to the amplified AC signal

– If it is absent, the amplified signal passing through RE will cause a voltage drop across it & hence output voltage and Gain of the Amplifier will reduce

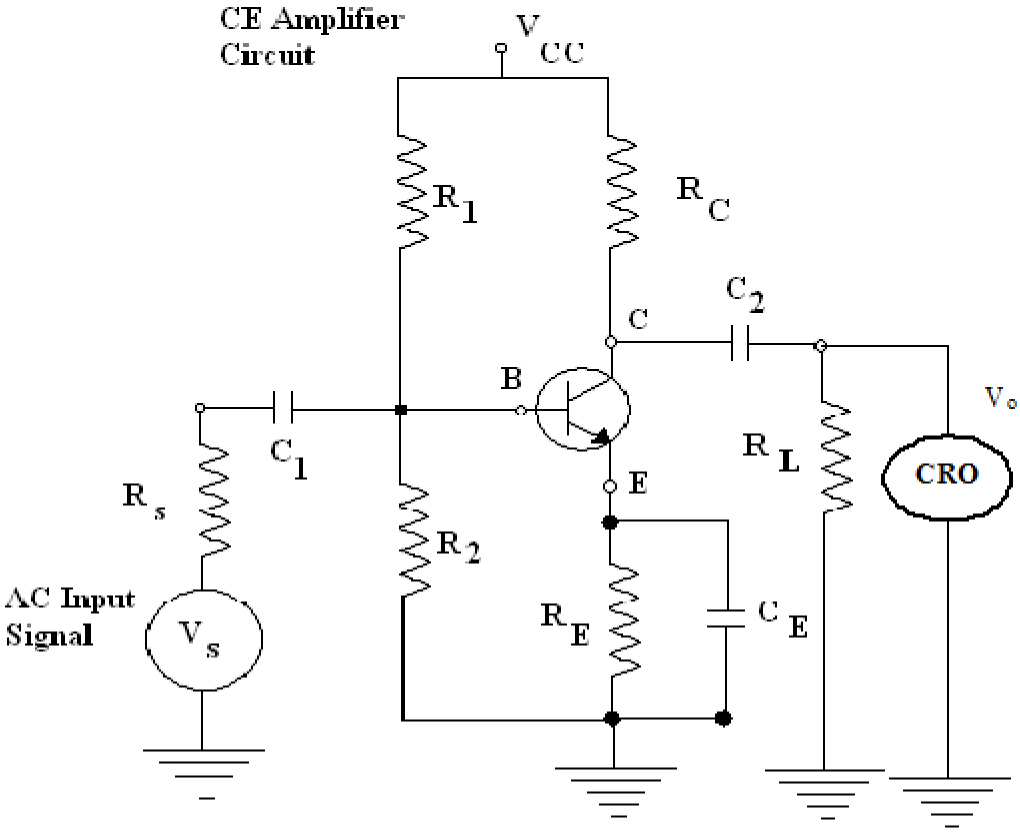
Output Coupling Capacitor, C_2

– Couples the output signal to the Load or to the next stage of the Amplifier

– Blocks DC and allows only the amplified AC Signal

RC coupling scheme finds application in Audio small signal amplifiers which are used in Record players, Tape recorders, Public address system, Radio & TV receivers etc.,

CIRCUIT DIAGRAM:



PROCEDURE:

Measurement of gain and plotting of frequency response curve

1. The circuit connection is made as per the circuit diagram using Bread board with Rs being a Decade Resistance Box (DRB). Set Rs=0.
2. The RPS is adjusted to the value of Vcc needed.
3. The voltage level of AO is adjusted to be suitable value V_s. This level was maintained constant through out the experiment.
4. The frequency of the oscillator was varied over its working range in suitable steps. For each frequency setting, the corresponding value of output voltage Vo is noted.
5. The voltage gain Av in dB is given by 20 log (Vo/Vi) is computed for each frequency setting.
6. The frequency response curve is plotted on semi log graph sheet. The bandwidth is calculated from the graph by drawing the 3dB line.

BW = f_2-f_1 Hz Where BW is the bandwidth

f_1 is the lower cutoff frequency.

f_2 is the lower and upper cutoff frequency

Determination of gain band width product

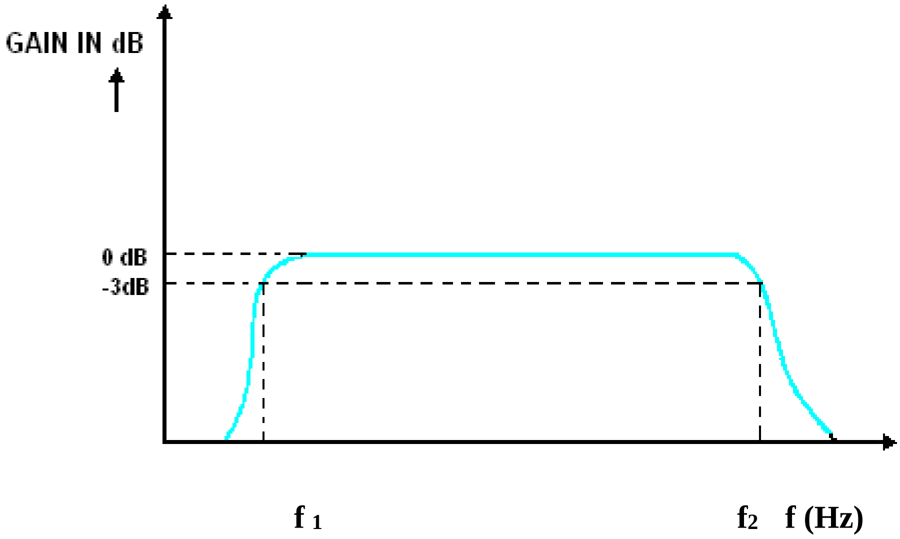
1. Find the mid band gain or maximum gain (Av) from the table.
2. Find the band width BW= f2-f1
3. Gain bandwidth product =|Av|BW

TABULATION 1

Input Voltage (V_s) =__mV

S.No	**Frequency f(Hz)**	**Output voltage V_o(Volt)**	**Gain in dB= ($20\log V_0/V_s$) dB**

MODEL GRAPH: FREQUENCY RESPONSE CURVE



Review Questions

1. What type of biasing used in this amplifier?
2. What are the advantages & disadvantages of RC coupled or CE amplifier?
3. Compare RC Coupled amplifier with Transformer coupled amplifier and Direct coupled amplifier.
4. Define Bandwidth.
5. Why bandwidth is measured at 3 dB points?
6. What is Stability factor?
7. What is the expression of Stability factor S, S’ & S’’ of Self biased BJT circuit?
8. Why is Voltage divider bias frequently used?
9. Based on operating point, Is Voltage divider bias circuit, a class A or class B or class AB amplifier?
10. What are the types of bias compensation techniques?

RESULT:

The BJT Common Emitter Amplifier using voltage divider bias (self-bias) with bypassed emitter resistor is designed & constructed and the frequency response of the amplifier is plotted.

- Bandwidth of the bypassed CE amplifier = f_2-f_1= _____________
- Mid band gain of bypassed CE amplifier=_____________
- Gain bandwidth product bypassed CE amplifier =_____________

Exp. No. (6b) FREQUENCY RESPONSE OF CS AMPLIFIERS

AIM:

1. To obtain the frequency response of the common source FET Amplifier
2. To find the Bandwidth.

APPRATUS:

N-channel FET (BFW11)	-1No.
Resistors (6.8KΩ, 1MΩ, 1.5KΩ)	-1No.Each
Capacitors 0.1µF,	-2Nos
47µF	-1No.
Regulated power Supply (0-30V)	-1No.
Function generator	-1No.
CRO	-1No.
CRO probes Bread board Connecting wires	-1pair

THEORY:

A field-effect transistor (FET) is a type of transistor commonly used for weak-signal amplification (for example, for amplifying wireless (signals). The device can amplify analog or digital signals. It can also switch DC or function as an oscillator. In the FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Field-effect transistors exist in two major classifications.

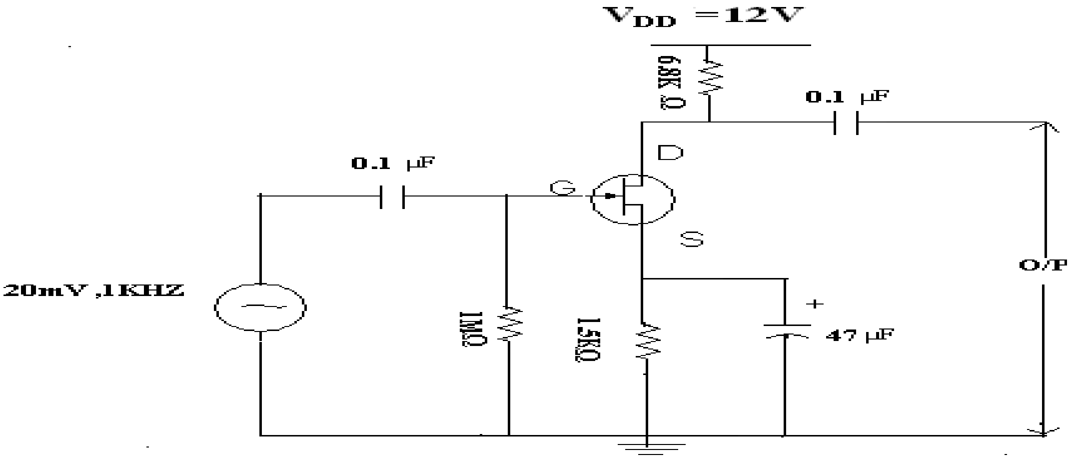
These are known as the junction FET (JFET) and the metal-oxide- semiconductor FET (MOSFET). The junction FET has a channel consisting of N-type semiconductor (N- channel) or P-type semiconductor (P-channel) material; the gate is made of the opposite semiconductor type. In P-type material, electric charges are carried mainly in the form of electron deficiencies called holes. In N-type material, the charge carriers are primarily electrons. In a JFET, the junction is the boundary between the channel and the gate. Normally, this P-N junction is reverse-biased (a DC voltage is applied to it) so that no current flows between the channel and the gate.

However, under some conditions there is a small current through the junction during part of the input signal cycle. The FET has some advantages and some disadvantages relative to the bipolar transistor. Field-effect transistors are preferred for weak-signal work, for example in wireless, communications and broadcast receivers. They are also preferred in circuits and systems requiring high impedance. The FET is not, in general, used for high-power amplification, such as is required in large wireless communications and broadcast transmitters.

Field-effect transistors are fabricated onto silicon integrated circuit (IC) chips. A single IC can contain many thousands of FETs, along with other components such as resistors, capacitors, and diodes.

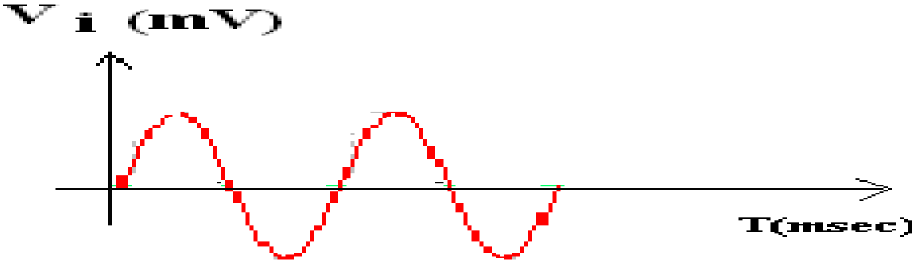
A common source amplifier FET amplifier has high input impedance and a moderate voltage gain. Also, the input and output voltages are 180 degrees out of Phase.

CIRCUIT DIAGRAM:

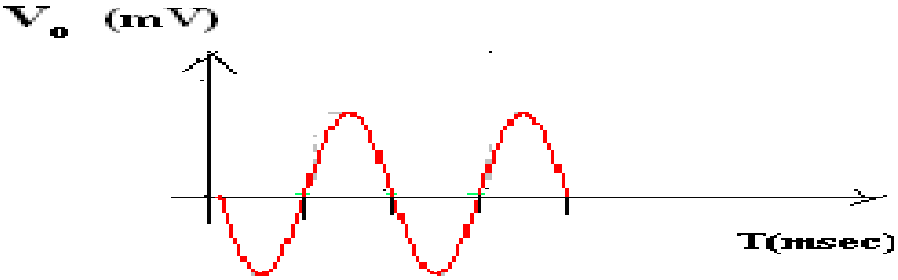


MODEL GRAPH:

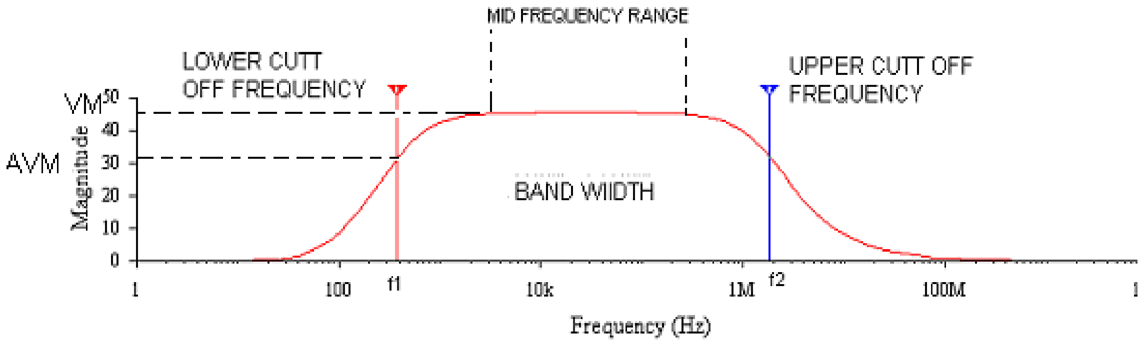
A) INPUT WAVEFORM



B) OUTPUT WAVEFORM



FREQUENCY RESPONSE PLOT



OBSERVATIONS:

INPUT VOLTAGE (V_i) =20mA

S.NO	Output Voltage(Vo)	Voltage gain=V0/Vin	Gain in dB=20log$_{10}$(V0/Vin)

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A signal of 1 KHz frequency and 20mV peak-to-peak is applied at the Input of amplifier.
3. Output is taken at drain and gain is calculated by using the expression,

$$A_V=V0/Vi$$

4. Voltage gain in dB is calculated by using the expression,

$$A_V=20\log 10(V0/V_i)$$

5. Repeat the above steps for various input voltages.
6. Plot A_V in dB Versus Frequency
7. The Bandwidth of the amplifier is calculated from the graph using the Expression,

$$\text{Bandwidth BW}=f_2-f_1$$

Where f_1 is lower 3 dB frequency f_2 is upper 3 dB frequency

Review Questions:

1. What is the difference between FET and BJT?
2. FET is unipolar or bipolar?
3. Draw the symbol of FET?
4. What are the applications of FET?
5. FET is voltage controlled or current controlled?
6. Draw the equivalent circuit of common source FET amplifier?
7. What is the voltage gain of the FET amplifier?
8. What is the input impedance of FET amplifier?
9. What is the output impedance of FET amplifier?
10. What are the FET parameters?
11. What is the applications of FET?

RESULT:

Thus, frequency response and bandwidth of common source FET is studied.

Exp.No. (7a) FREQUENCY RESPONSE OF CC AMPLIFIERS

AIM:

1. To measure the voltage gain of a CC amplifier
2. To draw the frequency response of the CC amplifier

APPARATUS:

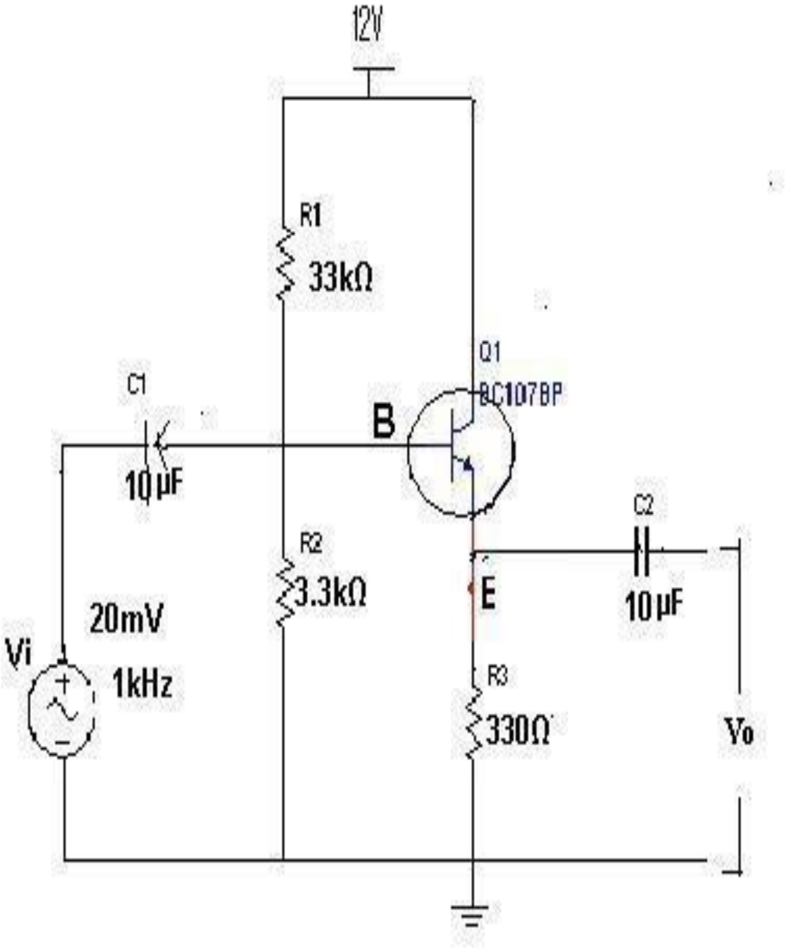
Transistor BC 107	-1No. Regulated
Power Supply (0-30V)	-1No. Function
Generator	-1No.
CRO	-1No.
Resistors 33KΩ, 3.3KΩ, 330Ω, 1.5KΩ, 1KΩ, 2.2KΩ & 4.7KΩ	-1No.Each
Capacitors 10µF	-2Nos
100µF	-1No.
Breadboard Connecting wires	

THEORY:

In common-collector amplifier the input is given at the base and the output is taken at the emitter. In this amplifier, there is no phase inversion between input and output. The input impedance of the CC amplifier is very high and output impedance is low. The voltage gain is less than unity. Here the collector is at ac ground and the capacitors used must have a negligible reactance at the frequency of operation.

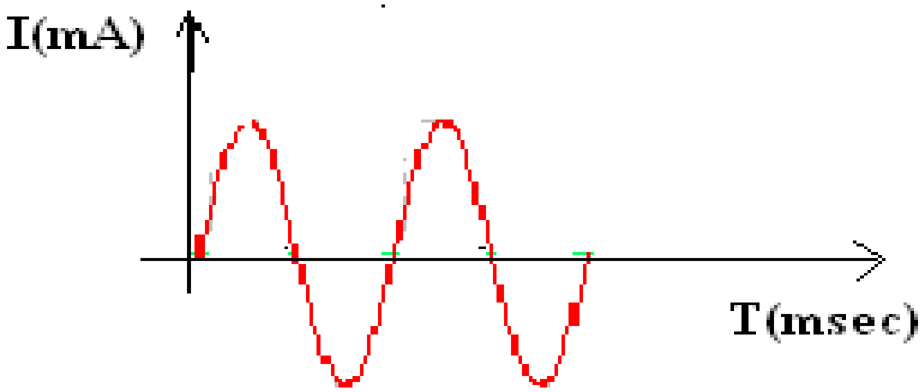
This amplifier is used for impedance matching and as a buffer amplifier. This circuit is also known as emitter follower. The most common use of the emitter follower is as a circuit, which performs the function of impedance transformation over a wide range of frequency.

CIRCUIT DIAGRAM:

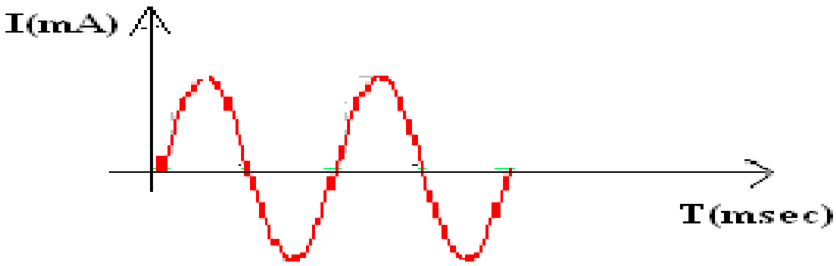


MODEL WAVEFORM:

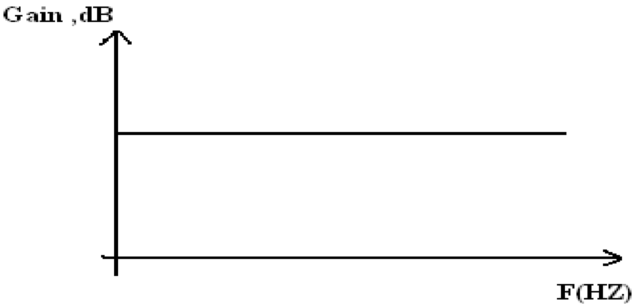
A) INPUT WAVEFORM:



B) OUTPUT WAVEFORM



FREQUENCY RESPONSE



OBSERVATIONS

A) FREQUENCY RESPONSE, V_i =

Frequency(HZ)	**Output Voltage(Vo)**	**Gain in dB A_v=20log 10(V0/V_i)**

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. The voltage gain calculated by using the expression A_V=V0/V_i
3. For plotting the frequency response the input voltage is kept constant a 20mV peak-to- peak and the frequency is varied from 100Hzto 1MHz.
4. Note down the values of output voltage for each frequency.
5. The voltage gain in dB is calculated by using the expression,
   A_V=20log 10(V0/V_i)
6. A graph is drawn by taking frequency on X-axis and gain in dB on y-axis on semi-log graph sheet.

7. The Bandwidth of the amplifier is calculated from the graph using the Expression,

   Bandwidth $BW=f_2-f_1$

   Where f_1 is lower cut-off frequency of CE amplifier f_2 is upper cut-off frequency of CE amplifier

8. The gain Bandwidth product of the amplifier is calculated using the Expression,

   Gain -Bandwidth product=3-dB midband gain X Bandwidth

Review Questions:

1. What are the applications of CC amplifier?
2. What is the voltage gain of CC amplifier?
3. What are the values of input and output impedances of the CC amplifier?
4. To which ground the collector terminal is connected in the circuit?
5. Identify the type of biasing used in the circuit?
6. Give the relation between α, β and γ.
7. Write the other name of CC amplifier?
8. What are the differences between CE, CB and CC?
9. When compared to CE, CC is not used for amplification. Justify your answer?

RESULT:

Exp.No. (7b) FREQUENCY RESPONSE OF CB AMPLIFIERS

AIM:

To design and construct a Common Base amplifier circuit using and to calculate its bandwidth and cut off frequency.

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	1
2	RPS	(0-30)V	1
3	Resistor	22 K	1
4	Resistor	4.7 K	1
5	Resistor	330 Ω	1
6	Resistor	1.2 K	1
7	Capacitor	1 uf	3
8	Bread Board	-	1
9	Single strand Wires	-	-
10	CRO	30 MHz	1
11	CRO Probes	-	3
12	Function Generator	(0 - 3) MHz	1

THEORY

An amplifier is used to increase the signal level; the amplifier is use to get a larger signal output from a small signal input The transistor can be used as a amplifier, if it is biased to operate in the active region, i.e. base-emitter junction is to be forward biased, while the base –collector junction to be reverse biased. Common-Base amplifier is constructed using self-bias circuit. The resistors R_1, R_2 and R_E are biasing resistors. Acts as a potential divider. Due to the change in the temperature or β, the base current increases so this makes to increase the collector current $I_{C,}$ therefore a Reverse Leakage

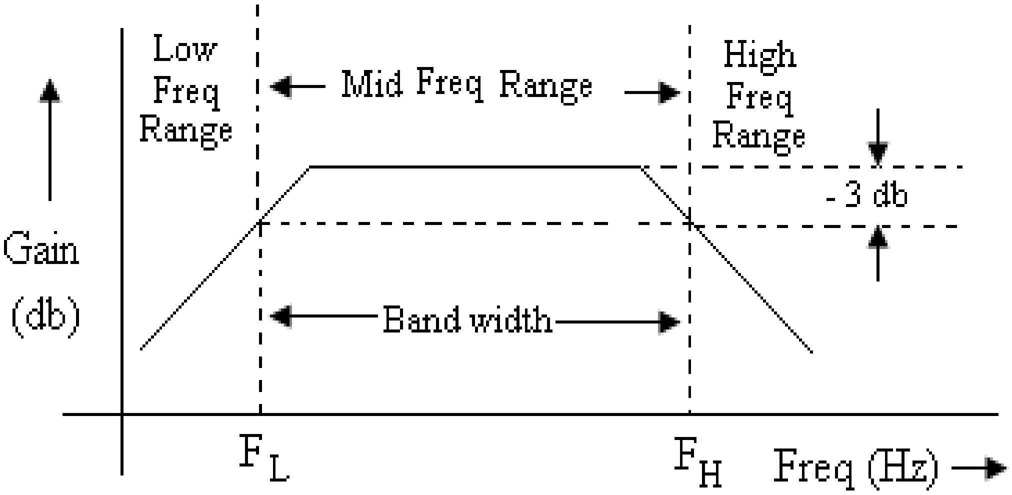
Current I_{CO} increases hence this affects the stability of transistor. By providing an emitter resistor R_E, it creates a voltage drop across R_E therefore the increased emitter current due to I_C starts to flow through R_E to ground and this makes in the reduction of Base Emitter Voltage V_{BE}. Due to reduction in V_{BE}, base current I_B reduces and hence collector Current I_C also reduces and the output remains constant.

For the common base amplifier the AC Input resistance is typically low from 10 to 100Ω. The output resistance of CB amplifier is typically high from 50KΩ to 1MΩ. Typical values of voltage amplification (Av) for CB amplifier vary from 50 to 300. The current amplification is always less than 1. The basic CB amplifying action was proposed for transferring the current from low resistance to high resistance circuit.

PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 3 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.
6. Calculate the bandwidth from the graph.

Model Graph



DESIGN OF COMMON BASE AMPLIFIER

Design parameters

Vcc=12V, Ic =Ie=4mA, h_{fe} (β) =100, Vbe =0.7V, S=10

Design specifications $V_{cc} = 12V$
$V_{RE} = 10\%$ of V_{cc} $V_{RC} = 40\%$ of V_{cc} $V_{CE} = 50\%$ of V_{cc} $I_c = I_e$
$I_b = I_c / \beta$

$V_{RE} = 10\%$ of V_{cc} $V_{RE} = 0.1 * 12 = 1.2$ V

$V_{RC} = 40\%$ of V_{cc} $V_{RC} = 0.4 * 12 = 4.8$ V

$V_{CE} = 50\%$ of V_{cc} $V_{CE} = 0.5 * 12 = 6$ V
<u>To find R_E</u>

$R_E = V_{RE} / I_e$
$R_E = 1.2 / 4x10^{-3}$ $R_E = 300\ \Omega$

TABULATION

Vin = __

SL.NO	**Frequency (Hz)**	**Output Voltage (Vo)**	**Gain = 20 log (Vo / Vi) (db)**

RESULT

Hence designed and constructed the Common Base Amplifier and calculated the band width and cut-off frequency.

Exp.No. (8) FREQUENCY RESPONSE OF CASCADED AMPLIFIERS

AIM:

To Design and Construct a Cascade Amplifier and to determine its:

a. DC Characteristics
b. Maximum Signal Handling Capacity
c. Gain of the amplifier
d. Bandwidth of the amplifier
e. Gain -Bandwidth Product

REQUIREMENTS:

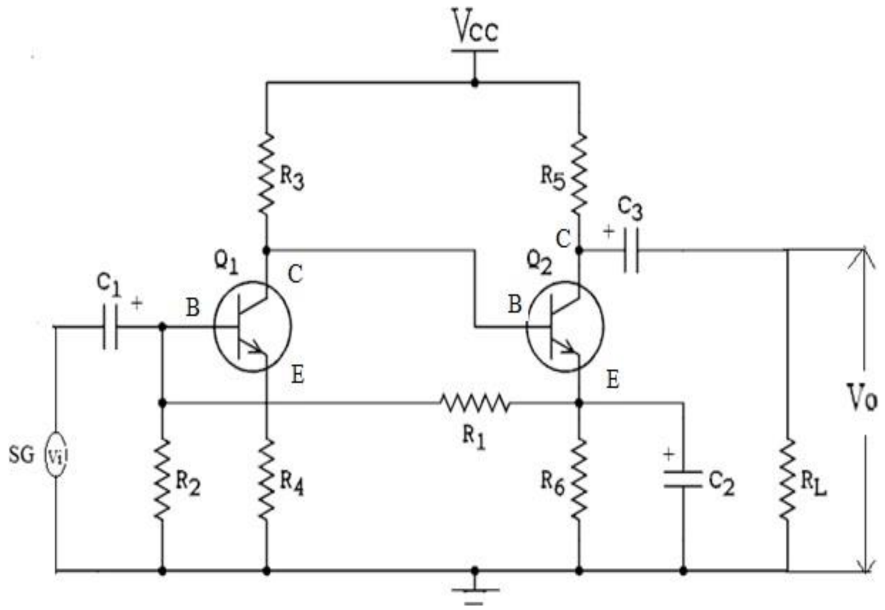
S.NO	REQUIREMENT	NAME	RANGE	QUANTITY
1	**COMPONENTS**	Transistor [Active]	BFW10	1
2		Resistor [Passive]		
3		Capacitor [Passive]		
4	**EQUIPMENTS**	Signal Generator	(0-3)MHz	1
5		CRO	30MHz	1
6		Regulated power supply	(0-30)V	1
7	**ACESSORIES**	Bread Board	-	1
8		Connecting Wires	Single strand	as required

THEORY:

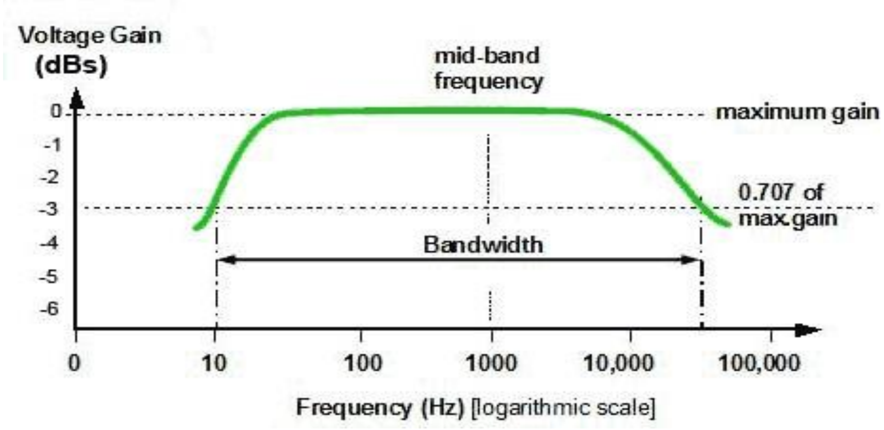
A cascade is type of multistage amplifier where two or more single stage amplifiers are connected serially. Many times the primary requirement of the amplifier cannot be achieved with single stage amplifier, because Of the limitation of the transistor parameters. In such situations more than one amplifier stages are cascaded such that input and output stages provide impedance

matching requirements with some amplification and remaining middle stages provide most of the amplification. These types of amplifier circuits are employed in designing microphone and loudspeaker.

CASCADE AMPLIFIER CIRCUIT DIAGRAM:



MODEL GRAPH:



PROCEDURE:

1. Connect the circuit as per the circuit diagram
2. Determine the Q-point of the amplifier using DC analysis.
3. Determine Maximum input voltage that can be applied to amplifier using AC analysis.
4. Set the input voltage Vin=V MSH /2 and vary the input signal frequency from 0Hz to 1MHz in incremental steps and note down the corresponding output voltage Vo for atleast 20 different values for the considered range.
5. The voltage gain is calculated as Av = 20log (V0/Vi)
6. Find the Bandwidth and Gain-Bandwidth Product from Semi-log graph taking frequency on x-axis and gain in dB on y-axis.,

Bandwidth, BW = f2-f1

where f1 - lower cut-off frequency f2 - upper cut-off frequency

a. DC ANALYSIS:

It is the procedure to find the operating region of transistor

Steps:

I) Set Vin = 0 by reducing the amplitude of the input signal from signal generator

II) Open circuit the capacitors since it blocks DC voltage

III) Set V_{CC}= +10v and measure the voltage drop across the Resistor V_{RC}, voltage across Collector- Emitter Junction V_{CE} and Voltage drop across base emitter junction. V_{BE}

IV) Find the Q-point of the transistor and draw the DC load line.

To verify dc condition

1. V_{BE} : (forward bias)
2. V_{RC} = ___
3. V_{CE} = ________(REVERSE BIAS)
4. Ic(Ic = (Vcc – V_{CE}) / Rc) =_________

Q point analysis:

It is the procedure to choose the opearating point of transistor

Q-point: (I_{CQ} =______; V_{CEQ} =_______)

b. Maximum signal handling capacity:

It is the process to find the maximum input voltage that can be handled by the amplifier, so that it amplifies the input signal without any distortion.

Procedure:

i. Apply input signal Vin = 20 mV of 1Khz frequency to the amplifier using the signal generator between base emitter junction of the transistor. Find the sinusoidal output using CRO across RL.

ii. By increasing the amplitude of the input signal find maximum input voltage V_{MSH} across V_{BE} at which the sinusoidal signal gets distorted during the process which can be seen in the CRO. The amplitude obtained at this point is maximum voltage that can be applied to the transistor for efficient operating of transistor.

V_{MSH} = __________volts

TABULATION

Input voltage (Vin=V_{MSH}/2) =_____________volts

S. NO	FREQUENCY [Hz]	OUTPUT VOLTAGE [VO] in Volts	GAIN= 20 log vo/vin dB
1	0		
2	100		
3	500		
4	600		
5	800		
6	900		
7	1KHz		
8	100 KHz		
9	500 KHz		
10	600 KHz		
11	700 KHz		
12	800 KHz		
13	900 KHz		
14	1MHz		
15	1.1 MHz		
16	1.5 MHz		

RESULT:

The Cascade amplifier was constructed and input resistance and gain were determined. The results are found to be as given below

a) Gain of the amplifier:

b) Bandwidth of the amplifier:

c) Gain-Bandwidth product:

Exp.No. (9) CMRR MEASUREMENT OF DIFFERENTIAL AMPLIFIERS

AIM

To construct a differential amplifier circuit for single input balanced output in the common mode and differential mode configuration and study the output waveform and to find Common Mode Rejection Ratio (CMRR).

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 107	2
2	Dual trace Regulated power supply	(0-30)V	1
3	Resistor	10 K	2
4	Resistor	4.7 k	1
5	Function Generator	(0-3)MHz	1
6	Bread Board	-	1
7	Single strand Wires	-	-
8	CRO	(0-30)MHz	1
9	CRO Probes	-	4

THEORY

The Differential amplifier amplifies the difference between two input signals. The transistorized differential amplifier consists of two ideal emitter biased circuits. The differential amplifier circuit is obtained by connecting the two emitter terminals E_1 and E_2. Hence RE is the parallel combination of R_{E1} and R_{E2}. The output is taken between the two collector terminals C_1 and C_2.Hence we say this connection as balanced output or double ended output. It works in two modes of operation.

Differential mode operation

In the differential mode operation two input signals (V_1 and V_2) are different in magnitudes and opposite in phase and it produces the difference between the two input signals ($V_1 \sim V_2$).The differential mode gain (A_D) can be calculated by $A_D = Rc * \beta / 2 * h_{ie.}$

Common mode operation

In the common mode operation two input signals are same in magnitude and phase. At emitter resistance R_E both the input signal appears across R_E and adds together since it just acts like an emitter follower .Therefore R_E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of the differential amplifier. The Common mode gain Ac can be calculated by

$|Ac| = Rc * \beta / h_{ie} + (2Re [1+$
$\beta])$ CMRR

CMRR (Common Mode Rejection Ratio) is defined as the ratio of differential gain to common mode gain. Ideally the CMRR should be infinity. CMRR = 20 log (A_D / Ac)

PROCEDURE

Differential mode configuration :

1. Connections are given as per circuit diagram
2. Set Vs =50 mV, using signal generator
3. Keeping the input voltage constant vary the frequency from 50Hz to1MHz in regular steps
4. Observe both input and output on the CRO (sine wave)
5. The differential gain is calculated at mid frequency range where the magnitude of the sine wave is maximum.
6. The differential gain is calculated by Ad = Vo / Vi

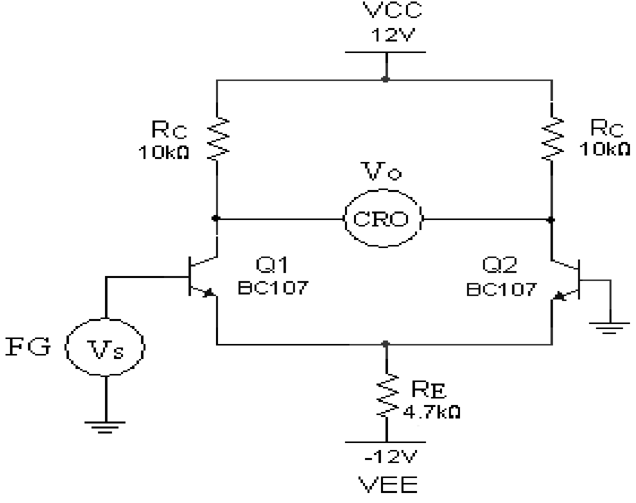
Common mode configuration

1. Connections are given as per circuit diagram
2. Set Vs =50 mV, using signal generator
3. Keeping the input voltage constant vary the frequency from 50Hz to1MHz in regular steps
4. Observe both input and output on the CRO (sine wave)
5. The common mode gain is calculated at mid frequency range where the magnitude of the sine wave is maximum
6. The Common mode gain is calculated by Ac = Vo / Vi CMRR

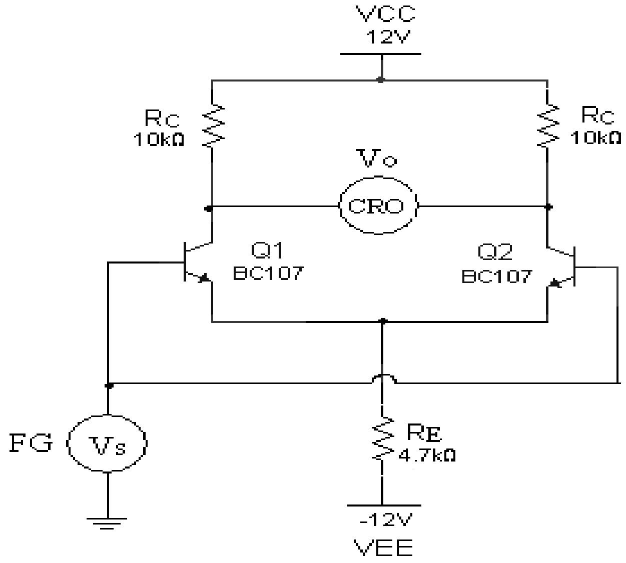
CMRR is calculated by substituting the practical values of Ad and Ac in the formula CMRR = 20 log (A_D / Ac)

Single input Balanced output Differential Amplifier

Differential mode



Common mode



TABULATION: DIFFERENTIAL MODE

S.NO	**Input Amplitude (Vi) (Volts)**	**Output Amplitude (Vo) (Volts)**	**Theoretical Differential gain (Ad)**	**Practical Differential gain (Vo / Vi) (Ad)**

COMMON MODE

S.NO	Input Amplitude (Vi) (Volts)	Output Amplitude (Vo) (Volts)	Theoretical Differential gain (Ac)	Practical Differential gain (Vo / Vi) (Ac)

CMRR

S.NO	Theoretical CMRR	**Practical CMRR** = 20 log (A_D / Ac)

Differential gain

A_D =Rc * β / 2* h_{ie}

A_D =8.7x10^3 * 300 / 2* 4.7

x10^3 A_D = 265

Common mode gain

|Ac| = Rc * β / h_{ie} + (2Re [1+ β])

Ac = 8.7kΩ * 300 / 4.7 kΩ + (2 * 3.3 kΩ [1+ 300])

Ac = 1.2

CMRR

Theoretical CMRR

$= 20 \log (A_D / A_c)$

$= 20 \log (265 / 1.2)$

$= 46$

RESULT

Thus constructed a differential amplifier circuit for single input balanced output in the common mode and differential mode configuration and studied the output waveform, also its CMRR has been determined and verified practically.

Differential mode : ________________

Common mode : ________________

CMRR : ________________

Exp.No. 10 CLASS A POWER AMPLIFIER

AIM: To design and test the class A power amplifier

APPARATUS:

1. Class A power amplifier trainer kit
2. Function Generator
3. CRO
4. BNC Probes and connecting wires

THEORY:

The amplifier is said to be class A power amplifier if the q point and the input signal are selected such that the output signal is obtained for a full input cycle. For this class the position of q point is approximately y at the midpoint of the load line. For all the values of input signal the transistor remains in the active region and never entire into the cutoff or saturation region. The collector current flows for 3600 (life cycle) of the input signal in other words the angle of the collector current flow is 3600 the class a amplifiers or furthers classified as directly coupled and transformer coupled and transformer coupled amplifiers in directly coupled type. The load is directly connected in the collector circuit while in the transformer coupled type, the load is coupled to the collector using the transformer.

Advantages:

1. Distortion analysis is very important

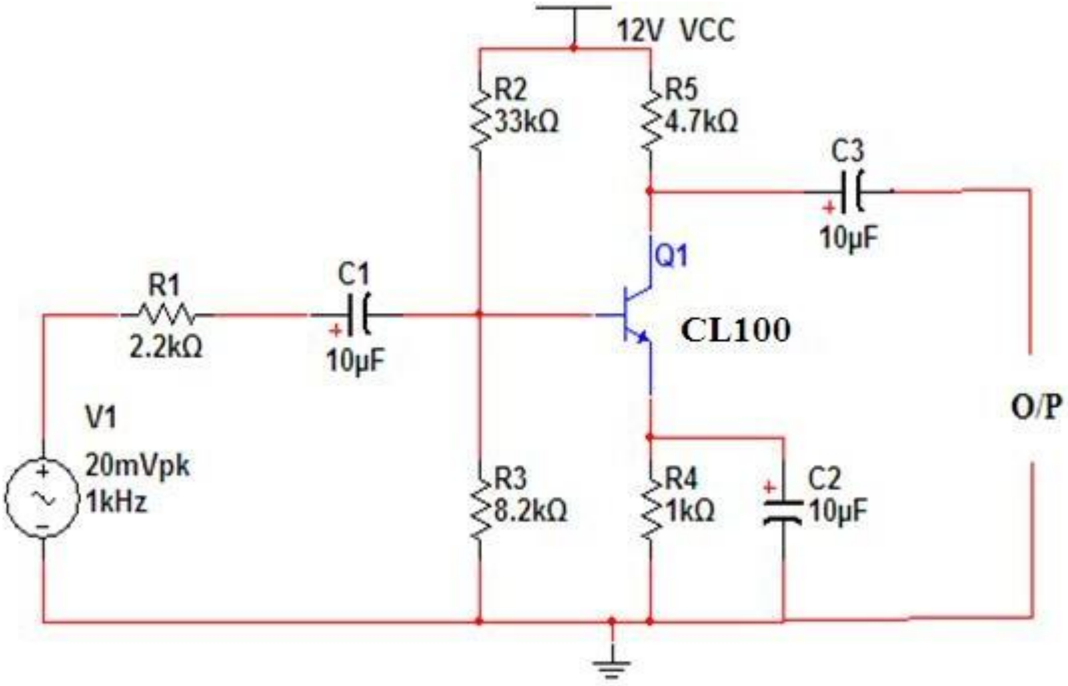
2. It amplifies audio frequency signals faithfully hence they are called as audio amplifiers

Disadvantages:

1. H parameter analysis is not applicable

2. Due to large power handling the transistor is used power transistor which is large in size and having large power rating.

CIRCUIT DIAGRAM:



PROCEDURE:

1. Switch ON Class –A power amplifier trainer
2. Set Vs (say 250 to 300 mV), at 10 KHz using signal generator.
3. Connect milli ammeter to the ammeter terminals
4. By keeping the input voltage constant, vary the frequency from 0 to 1MHz in regular steps .
5. Note down the corresponding output voltage from CRO
6. Calculate the DC input power using the formula $Pdc= V_{cc}I_c$
7. Calculate the AC output power using the formula $Pac = V_O^2/8R_L$
8. Calculate the efficiency $\eta = Pac /Pdc$
9. Plot the graph between Gain (db) and frequency.
10. Calculate bandwidth from the graph.

CALCULATIONS:

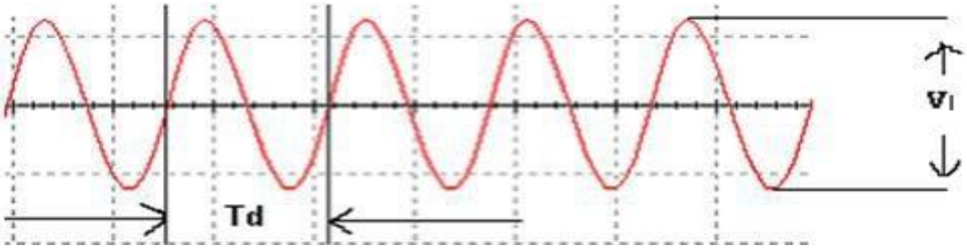
Input power: $Pdc = V_{cc}I_c$

Outpower: $Pac = VPP^2/8R_L$

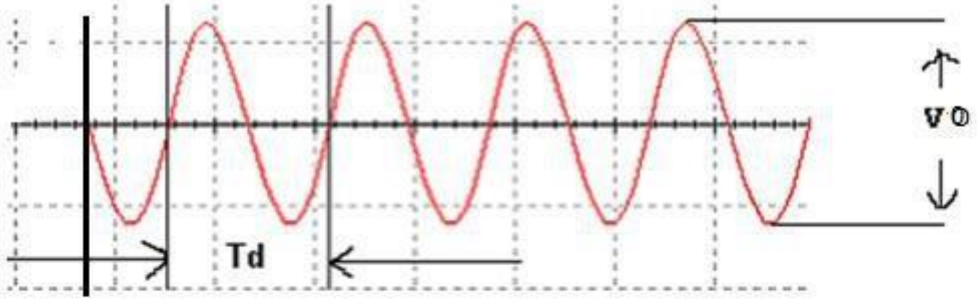
η = Efficiency=output power/input power*100 = Pac /Pdc*100

EXPECTED GRAPH:

I/P:



O/P:



Review Questions:

1. On which criteria based the power amplifiers are classified?

2. what is the operating point of class-A power ampliier?

3. what is meant by efficiency?

4. How much efficiency will b obtained in classs-A power amplifier?

5. what are the applications of power amplifier?

RESULT:

Gain and frequency as observed of Class A power amplifier.

η = Efficiency=output power/input power*100 = Pac /Pdc*100

Exp.No. 11 CLASS C POWER AMPLIFIER

AIM: To design the class C power amplifier

APPARATUS:

1. Class C power amplifier trainer kit
2. Function Generator
3. CRO
4. BNC Probes and connecting wires

THEORY:

The class C power amplifier is one kind of amplifier where the transistor conduct for less than 180° (one-half cycle of the input signal) and its typical value is 80° to 120°. The reduced conduction angle progresses the efficiency to a great expand, but roots a lot of distortion. The maximum theoretical efficiency of a Class-C amplifier is around 90%. This type of amplifier is not used in audio amplifiers because of the vast amounts of distortion. The applications of the class c amplifier mainly involve in radio frequency circuits like RF amplifier, RF oscillator, etc. Where there are extra tuned circuits for regaining the original i/p signal from the pulsed o/p of the amplifier. So the distortion which is caused by the class c amplifier has little effect on the final o/p.

Advantages of class c amplifier

- Efficiency is high
- Used in RF applications
- Physical size is low for a given power o/p

Disadvantages of class c amplifier

- Linearity is low
- Not fit in audio applications.
- It creates a lot of RF interference.
- It is difficult to obtain coupling transformers and ideal inductors.
- The dynamic range will be reduced.

CIRCUIT DIAGRAM:

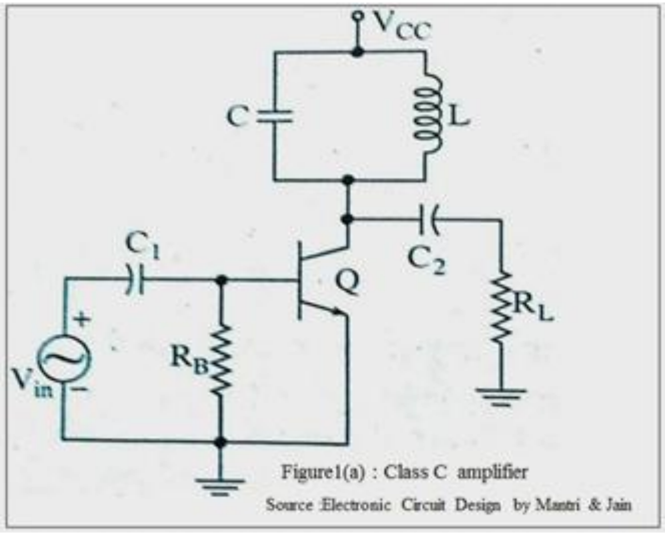


Figure1(a) : Class C amplifier

Source Electronic Circuit Design by Mantri & Jain

PROCEDURE:

1. Switch ON Class –C power amplifier trainer
2. Set Vs (say 250 to 300 mV), at 10 KHz using signal generator.
3. Connect milli ammeter to the ammeter terminals
4. By keeping the input voltage constant, vary the frequency from 0 to 1MHz in regular steps.
5. Note down the corresponding output voltage from CRO
6. Calculate the efficiency η
7. Plot the graph between Gain (db) and frequency.
8. Calculate bandwidth from the graph.

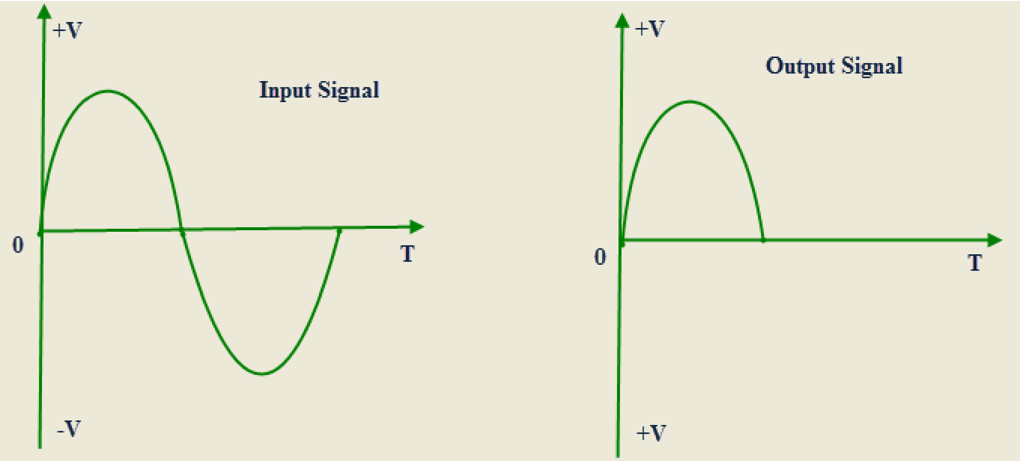
CALCULATION:

$$V_{out}=V_{supply}+(kV_{supply}\times\sin(2\pi f_1 t+\pi)).$$

Efficiency,

$$I_{CM} = \frac{g_m \times V_I}{1 - \cos\delta}$$

MODEL GRAPH:



RESULT:

Gain and frequency as observed of Class C power amplifier

Exp.No. 12 DARLINGTON AMPLIFIERS

AIM:

To design and construct a darlington amplifier and to calculate the bandwidth and cut off frequency.

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	2
2	RPS	(0-30)V	1
3	Resistor	150 K Ω	2
4	Resistor	10 K Ω	1
5	Resistor	4.7K Ω	1
6	Capacitor	1 uf	2
7	Bread Board	-	1
8	Single strand Wires	-	-
9	CRO	(0 - 30) MHz	1
10	CRO Probes	-	3
11	Function Generator	(0 - 3) MHz	1

THEORY

In Darlington connection of transistors, emitter of the first transistor is directly connected to the base of the second transistor. Because of direct coupling dc output current of the first stage is $(1+h_{fe})I_{b1}$.If Darlington connection for n transitor is considered, then due to direct coupling the DC output current foe last stage is $(1+h_{fe})^n$ times I_{b1} .Due to very large amplification factor even two stage Darlington connection has large output current and output stage may have to be a power stage. As the power amplifiers are not used in the amplifier circuits it is not possible to use more than two transistors in the Darlington connection.

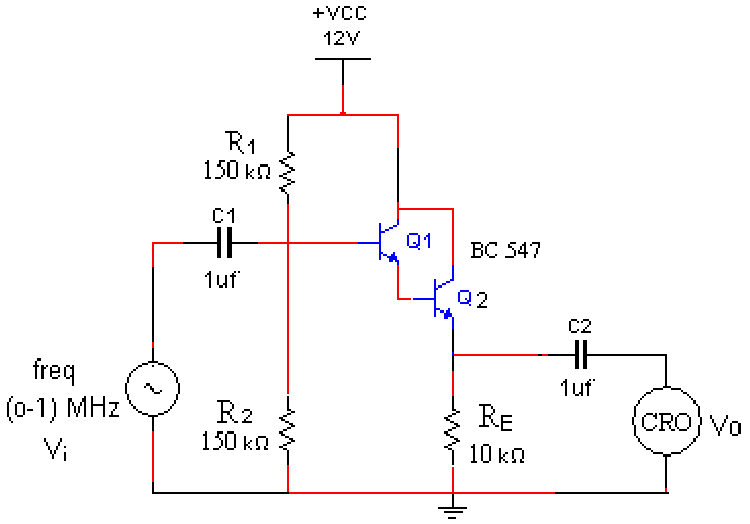
In Darlington transistor connection, the leakage current of the first transistor is amplified by the second transistor and overall leakage current may be high, Which is not desired.

PROCEDURE

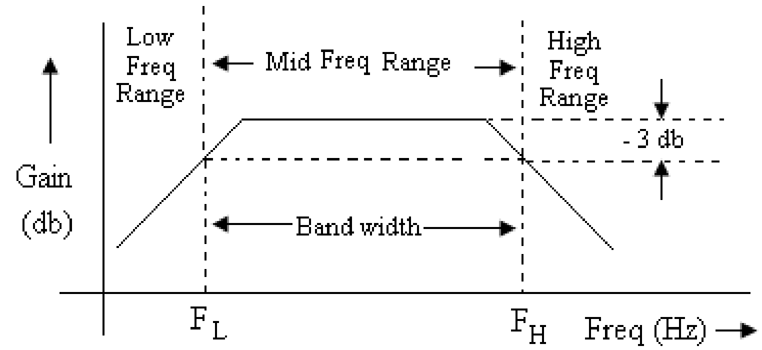
1. Connect the circuit as per the circuit diagram
2. Set Vs = 2V using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency.
6. Calculate the bandwidth from the graph.

CIRCUIT DIAGRAM:

Darlington Amplifier



Model Graph



TABULATION

Vin = __

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

RESULT

Hence designed and constructed the darlington Amplifier and calculated the band width and cut- off frequency

Exp No 13 DETERMINATION OF BANDWIDTH OF SINGLE STAGE AND MULTISTAGE AMPLIFIERS USING BJT

AIM:

To determine the bandwidth of single stage and multistage amplifier circuit using BJT and to plot its frequency response.

EQUIPMENTS REQUIRED

S.NO	EQUIPMENT	RANGE	QUANTITY
1	Transistor	BC 547	2
2	RPS	(0-30)V	1
3	Resistor	22 K	2
4	Resistor	4.7 K	2
5	Resistor	330 Ω	2
6	Resistor	1.2 K	2
7	Capacitor	1 uf, 4.7uf	3 2
8	Bread Board	-	1
9	Single strand Wires	-	-
10	CRO	30 MHz	1
11	CRO Probes	-	3
12	Function Generator	(0 - 3) MHz	1

THEORY:

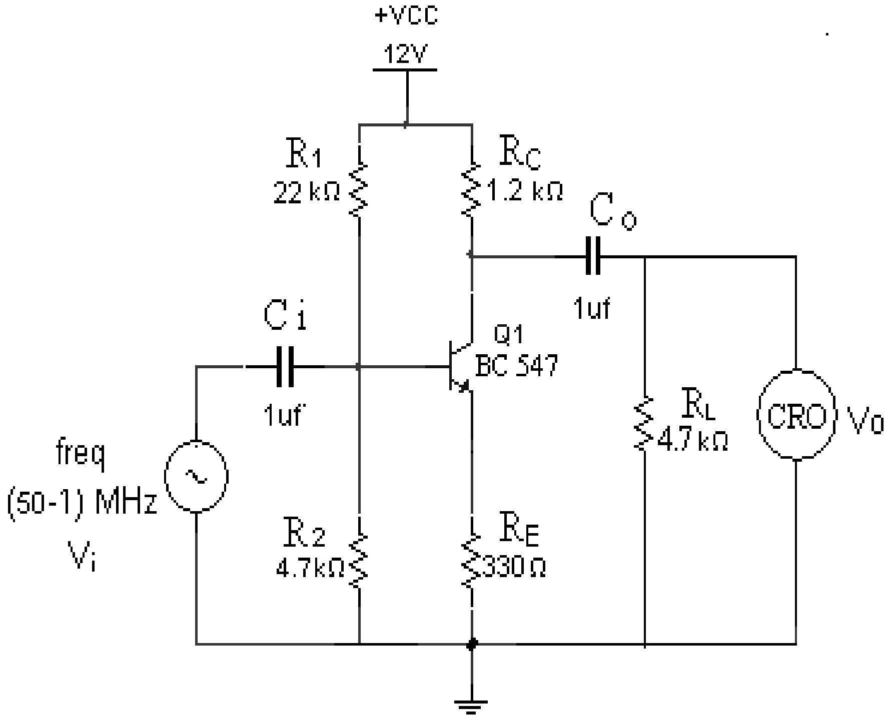
Single Stage amplifier

An amplifier is used to increase the signal level; the amplifier is use to get a larger signal output from a small signal input The transistor can be used as a amplifier, if it is biased to operate in the active

region, i.e. base-emitter junction is to be forward biased, while the base –collector junction to be reverse biased. Common-emitter amplifier is constructed using self bias circuit. The resistors R_1, R_2 and R_E are biasing resistors.

The resistors R_1 and R_2 act as a potential divider giving a fixed voltage to the base of the transistor. Due to the change in the temperature or β, the base current increases so this makes to increase the collector current $I_{C,}$ therefore a Reverse Leakage Current I_{CO} increases hence this affects the stability of transistor. By providing an emitter resistor R_E, it creates a voltage drop across R_E therefore the increased emitter current due to I_C starts to flow through R_E to ground and this makes in the reduction of Base Emitter Voltage V_{BE}. Due to reduction in V_{BE}, base current I_B reduces and hence collector Current I_C also reduces and the output remains constant.

SINGLE STAGE AMPLIFIER CIRCUIT USING BJT

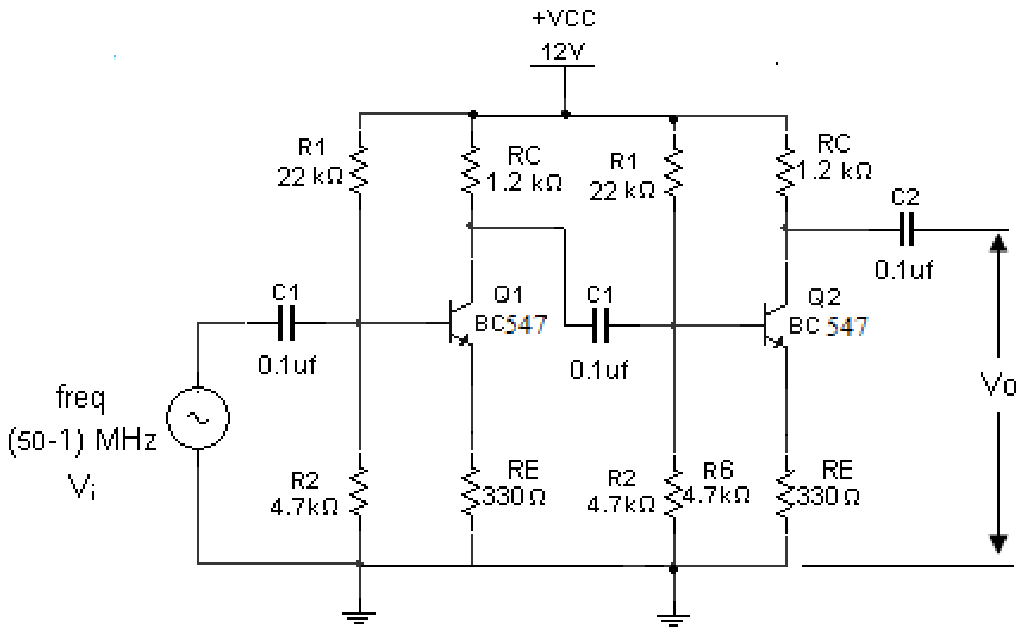


Multistage amplifier

Rc coupled amplifier usually employed for voltage amplification. It consists of a coupling capacitor which is used to connect the output of the first stage to the base (ie input) of the next stage. The resistors R1, R2, RE forms the biasing and stabilizing network. The emitter bypass capacitor offers low resistance path to the signal. Without it, the voltage gain of the each stage would be lost. The coupling capacitor blocks DC and allows AC therefore this prevents the DC interference between the various stages and the shifting of operating point.

When AC signal is applied to the base of the first transistor, it appears in the amplified form across its collector load Rc. the amplified signal developed across Rc is given to the next stage through coupling capacitor. The second stage does further amplification of the signal, in this way the cascaded stages amplify the signal and the overall gain is considerably increased and the bandwidth decreases.

MULTISTAGE AMPLIFIER CIRCUIT (CASCADE AMPLIFIER CIRCUIT)



PROCEDURE

1. Connect the circuit as per the circuit diagram
2. Set Vs = 50mV using signal generator.
3. Keep the input voltage constant; vary the frequency from 50 Hz to 1 MHz in steps.
4. Note down the corresponding output voltage.
5. Plot the graph gain Vs frequency
6. Calculate the bandwidth from the graph

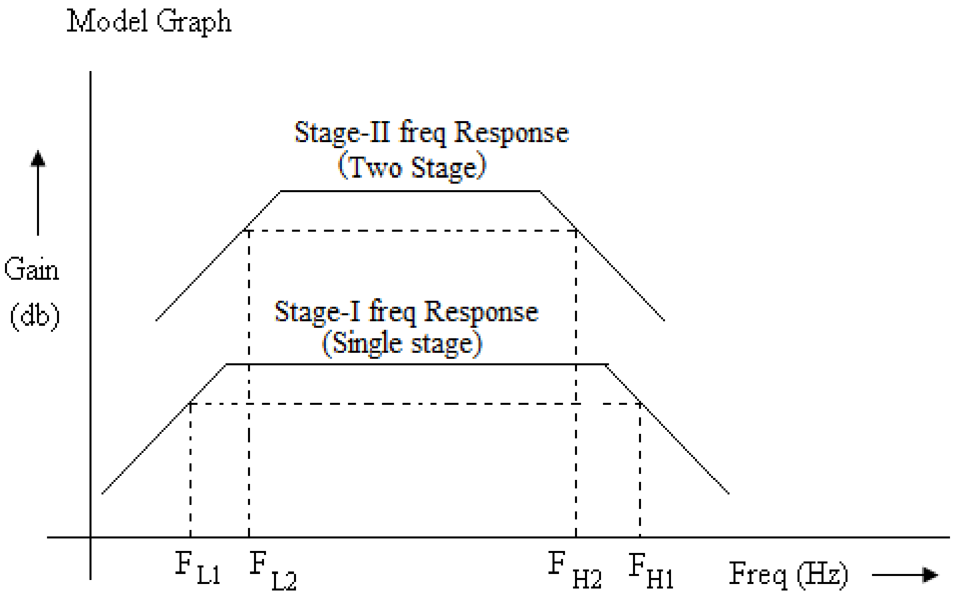
TABULATION

SINGLE STAGE AMPLIFIER

Vin = __

SL.NO	Frequency (Hz)	Output Voltage (Vo)	Gain = 20 log (Vo / Vi) (db)

FREQUENCY RESPONSE BETWEEN SINGLE STAGE AND MULTISTAGE AMPLIFIER



RESULT

Hence designed and constructed the single stage and multistage Amplifier and calculated its band width and cut-off frequency.