SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

V SEMESTER

EC3563 – VLSI and Chip Design

Regulation – 2023

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SUBJECT : EC3563 - VLSI and Chip Design

SEM / YEAR: V / III

UNIT I - MOS TRANSISTOR PRINCIPLES				
MOS logic families (NMOS and CMOS), Ideal and Non-Ideal IV Characteristics, CMOS devices. MOS(FET) Transistor Characteristic under Static and Dynamic Conditions, Technology Scaling, power consumption.				
PART – A				
Q. No	**Questions**	**CO**	**BTL**	**Competence**
1.	Name the different operating modes and regions of MOS transistor.	CO1	BTL1	Remembering
2.	Why nMOS devices conduct strong zero and weak one?	CO1	BTL1	Remembering
3.	How does MOSFET act as a switch?	CO1	BTL1	Remembering
4.	Differentiate Enhancement and Depletion mode devices.	CO1	BTL2	Understanding
5.	Define Subthreshold Conduction.	CO1	BTL1	Understanding
6.	Draw the structure and symbol of MOS transistor.	CO1	BTL2	Understanding
7.	Determine the rise time of a CMOS inverter drives a load capacitance C_L=40 fF through an effective pull-up resistance R_P=10 kΩ.	CO1	BTL2	Understanding
8.	Define propagation delay of CMOS Inverter.	CO1	BTL1	Remembering
9.	A clock at f=50MHz drives 200 identical nodes, each with C_l=8fF, toggling on 25% of cycles. if V_{DD}=1.0V. Calculate the total dynamic power.	CO1	BTL2	Understanding
10.	What are the functions of gate terminal in MOS transistor?	CO1	BTL1	Remembering
11.	Write the equation for describing the effective channel length modulation of nMOS transistor.	CO1	BTL2	Understanding
12.	List the Non ideal I-V effects of MOS transistor.	CO1	BTL1	Remembering
13.	Draw the DC transfer characteristics of CMOS inverter.	CO1	BTL2	Understanding
14.	Why pMOS transistors are wider than nMOS transistors?	CO1	BTL2	Understanding
15.	Write the threshold equation including the body effect.	CO1	BTL2	Understanding
16.	Define body effect.	CO1	BTL1	Remembering
17.	Mention the effects of channel length modulation on I-V behaviour.	CO1	BTL2	Understanding
18.	Identify the regions of operation in a CMOS inverter.	CO1	BTL1	Remembering
19.	Compare constant field scaling and constant voltage scaling.	CO1	BTL2	Understanding

20.	Name the major sources of power consumption in a CMOS circuit.		CO1	BTL2	Understanding
21.	Sketch a complementary CMOS gate computing W=(XY+YZ)'		CO1	BTL2	Understanding
22.	Describe the static behaviour of a MOSFET when gate voltage is below threshold.		CO1	BTL2	Understanding
23.	State Moore's Law with respect to MOS technology scaling.		CO1	BTL1	Remembering
24.	Determine whether an NMOS transistor with a threshold voltage of 0.7V is operating in the saturation region if V_{GS} = 2V and V_{DS} = 3V.		CO1	BTL2	Understanding
	PART – B				
1.	Explain the operation of NMOS enhancement transistor with necessary diagram.	(16)	CO1	BTL3	Applying
2.	Explain about the modes of operation in MOS transistor with neat diagram.	(16)	CO1	BTL3	Applying
3.	Describe the equation for source to drain current in the three regions of operation of a MOS transistor.	(16)	CO1	BTL3	Applying
4.	Discuss about the Non ideal I-V effects of MOS transistors with neat diagram.	(16)	CO1	BTL4	Analyzing
5.	Explain in detail about Long-Channel I-V Characteristics of MOS transistor.	(16)	CO1	BTL4	Analyzing
6.	Consider the nMOS transistor in a 0.6 µm process with gate oxide thickness of 100 Å. The doping level is $N_A = 2 \times 1017$ cm^{-3} and the nominal threshold voltage is 0.7V. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4 V instead of 0?	(16)	CO1	BTL4	Analyzing
7.	Describe the second order effects in MOS transistor with neat diagram.	(16)	CO1	BTL4	Analyzing
8.	Explain in detail about the DC transfer characteristics of CMOS inverter.	(16)	CO1	BTL3	Applying
9.	Write about the following MOS model with necessary equations. (i) Simple MOS capacitance model. (ii) Detailed MOS gate capacitance and diffusion capacitance model.	 (8) (8)	CO1	BTL4	Analyzing
10.	(i) Consider an nMOS transistor in a 0.6 µm process with W/L = 4/2 λ (i.e., 1.2/0.6 µm). In this process, the gate oxide thickness is 100 Å and the mobility of electrons is 350 $cm^2/V \cdot s$. The threshold voltage is 0.7 V. Plot Ids vs. Vds for Vgs = 0, 1, 2, 3, 4, and 5 V. (ii) Find the subthreshold leakage current of an inverter at room temperature if the input A = 0. Let $\beta n = 2\beta p$ = 1 mA/V^2, n = 1.0, and $\|Vt\|$ = 0.4 V. Assume the body effect and DIBL coefficients are $\gamma = \eta = 0$.	(8) (8)	CO1	BTL4	Analyzing

11.	Describe in detail about various regions of current versus input characteristics of CMOS inverter.	(16)	CO1	BTL4	Analyzing
12.	Write short notes on: (i) Transistor scaling (ii) Interconnect scaling.	 (8) (8)	CO1	BTL4	Analyzing
13.	Elaborate about the CV characteristics of MOS transistor along with neat sketches.	(16)	CO1	BTL4	Analyzing
14.	**(i)** Obtain the drain current in three different regionss of operation. **(ii)** Show how channel length modulation affects the drain current and body effect affects the threshold voltage?	(8) (8)	CO1	BTL3	Applying
15.	(i) Discuss the velocity saturation and mobility degradation of an nMOS transistor under non-deal I-V effects. (ii) Analyze the switching characteristics of a CMOS inverter. Derive rise time, fall time and propagation delay.	(8) (8)	CO1	BTL3	Applying
16.	Explain the operation of PMOS enhancement transistor with necessary diagram.	(16)	CO1	BTL3	Applying
17.	An NMOS transistor has a nominal threshold voltage of 0.16V. Determine the shift in threshold voltage caused by body effect using the following data. The NMOS transistor is operating at a temperature of 300ºK with the following parameters: gate oxide thickness (t_{ox}) = 0.2 * 10^{-5} cm, relative permittivity of gate oxide (ε_{ox}) = 3.9, relative permittivity of silicon (ε_{si}) = 11.7, substrate bias voltage = 2.5V, intrinsic electron concentration (N_i) = 1.5 * 10^{10}/cm^3, impurity concentration in substrate (N_A) = 3 * 10^{16} /cm^3. Given Boltzmann's constant = 1.38 * 10^{-23} J/ºK, electron charge = 1.6 * 10^{-19} Columb and permittivity of free space = 8.85 * 10^{-14} F/cm.	(16)	CO1	BTL3	Applying

UNIT II – COMBINATIONAL LOGIC CIRCUITS

Propagation Delays, stick diagram, Layout diagrams, Examples of combinational logic design, Elmore's constant, Static Logic Gates, Dynamic Logic Gates, Pass Transistor Logic, Power Dissipation, Low Power Design principles.

PART – A

Q. No	Questions	CO	BTL	Competence
1.	Explain the difference between rise time and fall time delays.	CO2	BTL1	Remembering
2.	Plot the precharge and evaluation modes of dynamic gates timing diagram.	CO2	BTL1	Remembering
3.	Clarify how fan-out influences delay in logic circuits.	CO2	BTL2	Understanding
4.	Define propagation delay and contamination delay.	CO2	BTL1	Remembering
5.	Draw the design process for an XOR gate using CMOS logic.	CO2	BTL2	Understanding
6.	Draw the stick diagram for 3-input NOR gate.	CO2	BTL2	Understanding
7.	Differentiate between pass transistor logic and transmission gate logic.	CO2	BTL2	Understanding

8.	Explain the trade-off between power and performance in VLSI.		CO2	BTL2	Understanding
9.	What is stick diagram? Draw the stick diagram for two input NAND gate.		CO2	BTL1	Remembering
10.	Compare the static CMOS, Pseudo-nMOS inverters.		CO2	BTL2	Understanding
11.	Mention the design rules associated with layout diagram.		CO2	BTL1	Remembering
12.	Design a 2-input CMOS NAND gate with its truth table.		CO2	BTL2	Understanding
13.	State the formula for Elmore's delay in an RC network.		CO2	BTL1	Remembering
14.	Realize the two input NAND gate using Pass transistor logic.		CO2	BTL2	Understanding
15.	How logic levels are degraded in pass transistor logic.		CO2	BTL2	Understanding
16.	A CMOS gate at V_{DD}=1.0V exhibits a subthreshold leakage current I_{leak}=50nA. calculate its static power dissipation.		CO2	BTL1	Remembering
17.	Write the static dissipation equation in CMOS inverter.		CO2	BTL2	Understanding
18.	Mention the methods used for dynamic power reduction.		CO2	BTL1	Remembering
19.	How to calculate the average dynamic power dissipation?		CO2	BTL1	Remembering
20.	List any two factors influencing leakage power.		CO2	BTL1	Remembering
21.	Draw the layout diagram for CMOS inverter.		CO2	BTL2	Understanding
22.	Define pass transistor logic.		CO2	BTL1	Remembering
23.	What is the influence of voltage scaling on power and delay?		CO2	BTL1	Remembering
24.	What is mean by PDP?		CO2	BTL2	Understanding
	PART – B				
1.	(i) Find the Elmore's constant of the 4-inputNAND gate. (ii) Realize the AND gate using pass transistor logic and explain the operation circuit.	(8) (8)	CO2	BTL4	Analyzing
2.	What are the sources of power dissipation in CMOS and discuss various design techniques to reduce power dissipation in CMOS?	(16)	CO2	BTL4	Analyzing
3.	(i) Draw the CMOS logic circuit for the Boolean expression $Z = \overline{(A+B)(A+C)(B+D)}$. (ii) Realize the function $F = (A+B+C)D$ using static CMOS logic.	(8) (8)	CO2	BTL3	Applying
4.	Realize a 2-input NOR gate using static CMOS logic, Domino Logic and complementary pass transistor logic. Analyze the hardware complexity in terms of transistor count.	(16)	CO2	BTL4	Analyzing
5.	Explain in detail about the working of Cascode Voltage Switch Logic (CVSL) with neat diagram.	(16)	CO2	BTL3	Applying
6.	Discuss the structure and working of pass transistor logic with neat diagram.	(16)	CO2	BTL3	Applying
7.	Demonstrate about the structure and working of CMOS with transmission gates.	(16)	CO2	BTL3	Applying
8.	Summarize about the working of Complementary pass transistor logic (CPL) with neat diagram.	(16)	CO2	BTL4	Analyzing

9.	Explain in detail about the working of Differential pass transistor logic (DPL) with neat diagram.	(16)	CO2	BTL4	Analyzing
10.	Describe the properties and operation of dynamic CMOS logic with neat diagram.	(16)	CO2	BTL4	Analyzing
11.	Examine about the cascading of 2 dynamic gates with neat diagram.	(16)	CO2	BTL4	Analyzing
12.	Describe the basic principle of operation of Domino logic with neat diagrams.	(16)	CO2	BTL4	Analyzing
13.	Classify the types of power dissipation and derive the equation each parameter.	(16)	CO2	BTL4	Analyzing
14.	Discuss the following power dissipation techniques and its impact in CMOS inverter circuits. (i) Static dissipation, (ii) Dynamic dissipation.	(8) (8)	CO2	BTL4	Analyzing
15.	Design a CMOS compound gate(or) static gate for the Boolean expression $F = \overline{DE + A \bullet (B + C)}$.	(16)	CO2	BTL3	Applying
16.	Implement the Boolean function using CMOS logic gates $Z = \overline{AB + AC + BD}$.	(16)	CO2	BTL3	Applying
17.	Sketch a combinational function Y= (AB+CD) (i) Pseudo nMOS logic (ii) Domino Logic.	(16)	CO2	BTL4	Analyzing

UNIT III - SEQUENTIAL LOGIC CIRCUITS AND CLOCKING STRATEGIES

Static Latches and Registers, Dynamic Latches and Registers, Pipelines, Nonbistable Sequential Circuits. Clocking strategies of Digital Systems, Synchronous Design, Self-Timed Circuit Design.

PART – A

Q. No	Questions	CO	BTL	Competence
1.	Identify the primary difference between a latch and a register.	CO3	BTL1	Remembering
2.	State the approaches used to accomplish the bistable circuit.	CO3	BTL1	Remembering
3.	Differentiate between D-latch and D-flip-flop.	CO3	BTL2	Understanding
4.	Define Bistability principle.	CO3	BTL1	Remembering
5.	Outline the working of dynamic positive edge-triggered register when Clk = 0.	CO3	BTL1	Remembering
6.	Interpret how charge storage is used in dynamic latches.	CO3	BTL2	Understanding
7.	Explain how pipelining improves system throughput.	CO3	BTL2	Understanding
8.	Compare synchronous and asynchronous clocking.	CO3	BTL2	Understanding
9.	List the different types of clocking strategies.	CO3	BTL1	Remembering
10.	Mention the advantages of pipelined operation.	CO3	BTL1	Remembering
11.	What is meant by sense-amplifier based registers?	CO3	BTL2	Understanding
12.	Sketch the circuit of latch-based pipeline using C^2MOS latches.	CO3	BTL1	Remembering
13.	Compare & contrast synchronous design and asynchronous	CO3	BTL1	Remembering

	design.				
14.	List out the timing parameters of the sequential circuit in synchronous design.		CO3	BTL1	Remembering
15.	Explain how a master-slave flip-flop works.		CO3	BTL2	Understanding
16.	What is clock skew? How to overcome the clock skew?		CO3	BTL2	Understanding
17.	Interpret how charge sharing affects dynamic register performance.		CO3	BTL2	Understanding
18.	How signal propagation is handled in non-bistable designs.		CO3	BTL2	Understanding
19.	Highlight the role of setup and hold time in synchronous circuits.		CO3	BTL2	Understanding
20.	Interpret the concept of completion detection in self-timed circuits.		CO3	BTL2	Understanding
21.	Write the role of a precharge phase in dynamic circuits.		CO3	BTL1	Remembering
22.	Describe how handshaking works in self-timed circuit design.		CO3	BTL2	Understanding
23.	Mention two problems caused by skew in clock distribution.		CO3	BTL1	Remembering
24.	State two advantages of using pipelining in processors.		CO3	BTL1	Remembering
PART-B					
1.	Explain in detail about static latches and registers.	(16)	CO3	BTL3	Applying
2.	State Bistability principle and explain in detail about the two different approaches used in this.	(16)	CO3	BTL4	Analyzing
3.	Summarize about Multiplexer-Based Latches with neat diagram.	(16)	CO3	BTL4	Analyzing
4.	Explain in detail about the synchronous pipelining approaches to optimize sequential circuits.	(16)	CO3	BTL4	Analyzing
5.	Explain in detail about dynamic latches and registers.	(16)	CO3	BTL4	Analyzing
6.	Draw and explain about Master-Slave Edge-Triggered register with its timing properties and non-ideal clock signals.	(16)	CO3	BTL3	Applying
7.	Explain about True Single-Phase Clocked (TSPC) latches.	(16)	CO3	BTL3	Applying
8.	(i) Compare the data path for computation of log(|a+b|) in pipelined and nonpipelined design. (ii) Explain the clock distribution techniques in synchronous design in detail.	(8) (8)	CO3	BTL3	Applying
9.	(i) Apply the concept of 3-stage pipelining to log(|an+bn|) and find the number of clock period for n = 3 to get the output. (ii) What are clocking strategies of Digital Systems.	(10) (6)	CO3	BTL3	Applying
10.	(i) Illustrate the combined effect of skew and jitter in sequential logic circuit and find the time period of the clock. (ii) Design the sequential logic circuit based on self-timed approach.	(8) (8)	CO3	BTL3	Applying
11.	Explain the concept of timing issues and pipelining in sequential circuits.	(16)	CO3	BTL3	Applying
12.	Analyse the basics of synchronous timing, clock skew,	(16)	CO3	BTL4	Analyzing

	clock jitter and combined impact of skew and jitter.				
13.	With necessary diagram, explain the Monostable sequential circuits.	(16)	CO3	BTL4	Analyzing
14.	Evaluate the various sources of skew and jitter and explain it.	(16)	CO3	BTL3	Applying
15.	Explain the operation of Astable Circuits with a neat diagram.	(16)	CO3	BTL3	Applying
16.	Derive the equation for Min and Max – Delay Constraints for sequential circuits.	(16)	CO3	BTL4	Analyzing
17.	Design a C^2MOS Register with CLK-$\overline{CLK}$ clocking approach.	(16)	CO3	BTL4	Analyzing

UNIT IV - INTERCONNECT, MEMORY ARCHITECTURE AND ARITHMETIC CIRCUITS

Interconnect Parameters – Capacitance, Resistance, and Inductance, Electrical Wire Models, Sequential digital circuits: adders, multipliers, comparators, shift registers. Logic Implementation using Programmable Devices (ROM, PLA, FPGA), Memory Architecture and Building Blocks, Memory Core and Memory Peripherals Circuitry.

PART-A

Q. No	Questions	CO	BTL	Competence
1.	Describe how interconnect delay is influenced by wire dimensions.	CO4	BTL2	Understanding
2.	Write about carry propagation delay and its effect in circuits.	CO4	BTL2	Understanding
3.	List out the components of Data path.	CO4	BTL1	Remembering
4.	Why is barrel Shifters very useful in the designing of arithmetic circuits?	CO4	BTL2	Understanding
5.	Define parasitic capacitance in an interconnect line.	CO4	BTL1	Remembering
6.	Obtain the critical path delay of 4-bit ripple carry adder,	CO4	BTL2	Understanding
7.	Draw the structure of 6- transistor SRAM cell.	CO4	BTL1	Remembering
8.	List the types of wire models used in digital VLSI design.	CO4	BTL1	Remembering
9.	Compare SRAM and DRAM.	CO4	BTL1	Remembering
10.	Explain the difference between serial and parallel multipliers.	CO4	BTL1	Remembering
11.	Define memory hierarchy.	CO4	BTL1	Remembering
12.	Interpret how logic functions are realized using a ROM.	CO4	BTL2	Understanding
13.	Distinguish between combinational and sequential logic in FPGA implementations.	CO4	BTL2	Understanding
14.	How configuration is achieved in an SRAM-based FPGA.	CO4	BTL2	Understanding
15.	Clarify the role of sense amplifiers in memory design.	CO4	BTL2	Understanding
16.	Write the full adder output in terms of propagate and generate.	CO4	BTL2	Understanding
17.	State the use of row and column decoders in memory arrays.	CO4	BTL1	Remembering
18.	Write the charge-share equation for DRAM.	CO4	BTL1	Remembering

19.	Draw a one transistor DRAM cell.		CO4	BTL2	Understanding
20.	Outline the basic structure of a memory cell array.		CO4	BTL2	Understanding
21.	What is meant by bit sliced data path organisation?		CO4	BTL2	Understanding
22.	Which factors determine the performance of a programmable shifter?		CO4	BTL2	Understanding
23.	Determine the propagation delay of a n – bit carry select adder.		CO4	BTL2	Understanding
24.	Define Clock-skew and clock-jitter.		CO4	BTL1	Remembering
	PART-B				
1.	Illustrate the hierarchal memory architecture and explain the building blocks of memory architecture.	(16)	CO4	BTL4	Analyzing
2.	(i) Explain the operation of a basic 4-bit binary adder. (ii) Describe the different approaches of improving the speed of the adder.	(10) (6)	CO4	BTL3	Applying
3.	Describe the working of ripple carry adder and derive the expression for worst case delay.	(16)	CO4	BTL3	Applying
4.	(i) Write the design techniques in dealing with capacitive cross talk. (ii) Describe the design techniques available to the designer to address the voltage drop over the inductor problem.	(8) (8)	CO4	BTL3	Applying
5.	Write short notes on Static CMOS adders.	(16)	CO4	BTL4	Analyzing
6.	Explain the operation of Carry Bypass adders with neat diagram.	(16)	CO4	BTL4	Analyzing
7.	(i) Realize the combinational function with PLA Y1 = ∑m(2,3,4,6) and Y2= ∑m(1,2,3,4). (ii) Elucidate the basic architecture of FPGA.	(8) (8)	CO4	BTL3	Applying
8.	Write the equations governing the design of carry skip adder and explain its working.	(16)	CO4	BTL3	Applying
9.	Construct 4 X 4 array type multiplier and find its critical path delay.	(16)	CO4	BTL4	Analyzing
10.	(i) Implement the 2 to 4 decoder using ROM. (ii) Discuss the types of FPGA routing techniques.	(8) (8)	CO4	BTL3	Applying
11.	Draw and explain the building blocks of FPGA with different fusing technologies.	(16)	CO4	BTL4	Analyzing
12.	Realize the function $F_1=X_0X_1+X_1'X_2'$; $F_2= X_0'X_1'+X_1X_2$ using Programmable Logic Array.	(16)	CO4	BTL3	Applying
13.	Examine the working of Multi-ported SRAM and Register file CMOS logic circuit.	(16)	CO4	BTL3	Applying
14.	Explain about the DRAM sub array and open bit lines architecture.	(16)	CO4	BTL4	Analyzing
15.	Draw and explain the architecture of large memory array with sub array memory circuitry.	(16)	CO4	BTL4	Analyzing
16.	(i) Design a 4 bit Binary to Excess-3 code converter using ROM. (ii) Implement Full adder using PLA.	(8) (8)	CO4	BTL4	Analyzing

17.	Describe the operation of Carry Select Adder with a block diagram.	(16)	CO4	BTL3	Applying

UNIT V - ASIC DESIGN AND TESTING				
Microchip design process & issues in testing and verification of complex chips. ASIC Design Flow, need for test benches, Writing test benches in Verilog HDL, Automatic test pattern generation, Design for testability, Scan design: Test interface and boundary scan.				
PART-A				
Q. No	**Questions**	**CO**	**BT Level**	**Competence**
1.	List the major stages involved in the microchip design process.	CO5	BTL 1	Remembering
2.	State any two common verification methods used in chip design.	CO5	BTL 1	Remembering
3.	Write Verilog system tasks commonly used in test benches.	CO5	BTL 1	Remembering
4.	Interpret the purpose of *initial* and *always* blocks in test benches.	CO5	BTL 2	Understanding
5.	Define the term ASIC.	CO5	BTL 2	Understanding
6.	Describe how a clock signal can be generated in a test bench.	CO5	BTL 2	Understanding
7.	State the features of boundary scan method.	CO5	BTL 1	Remembering
8.	Differentiate between observability and controllability.	CO5	BTL 2	Understanding
9.	How ATPG improves fault coverage.	CO5	BTL 1	Remembering
10.	Name any two faults commonly targeted in ATPG.	CO5	BTL 1	Remembering
11.	Define functional verification.	CO5	BTL 1	Remembering
12.	Identify different types of ASIC Design Methodology.	CO5	BTL 2	Understanding
13.	Infer the role of TAP (Test Access Port) in boundary scan.	CO5	BTL 2	Understanding
14.	Identify the ways to optimize the manufacturability, to increase yield.	CO5	BTL 2	Understanding
15.	Outline the significance of test benches in simulation-based testing.	CO5	BTL 2	Understanding
16.	Interpret the role of *$display* and *$monitor* in test benches.	CO5	BTL 2	Understanding
17.	Distinguish between standard cell-based ASICs and full custom ASIC.	CO5	BTL 1	Remembering
18.	Differentiate between ad-hoc and structured DFT techniques.	CO5	BTL 1	Remembering
19.	Summarize the role of place and route in ASIC design.	CO5	BTL 2	Understanding
20.	How boundary scan improves test accessibility.	CO5	BTL 1	Remembering
21.	Differentiate between channelled and channel less gate array.	CO5	BTL 1	Remembering
22.	Distinguish between front-end and back-end ASIC design processes.	CO5	BTL 2	Understanding
23.	What is DFT?	CO5	BTL 2	Understanding
24.	Describe the function of logic synthesis in ASIC design.	CO5	BTL 1	Remembering
PART-B				

1.	Illustrate the microchip design process and identify the issues in test.	(16)	CO5	BTL3	Applying
2.	Explain the automatic test pattern generation with a suitable example.	(16)	CO5	BTL4	Analyzing
3.	Explain the ASIC design flow with a neat diagram.	(16)	CO5	BTL3	Applying
4.	Generate the test vector for the combinational function F=(AB+BC+CD) using Automatic test pattern generation for the stuck-at-0 fault at node B.	(16)	CO5	BTL3	Applying
5.	Explain the architecture of parallel scan testing method.	(16)	CO5	BTL4	Analyzing
6.	Examine the boundary scan architectures and explain how to test the circuit board level and system level.	(16)	CO5	BTL4	Analyzing
7.	Describe briefly about the BIST block structure along its components.	(16)	CO5	BTL4	Analyzing
8.	Define an ASIC? Explain different types of ASIC's.	(16)	CO5	BTL3	Applying
9.	Write the goals and objectives of following terms a) Floor planning b) Placement c) Routing.	(16)	CO5	BTL4	Analyzing
10.	Explain the ASIC design flow with a neat diagram and write the difference between custom IC and standard IC.	(16)	CO5	BTL4	Analyzing
11.	Write the testbench in Verilog HDL for a combinational circuit.	(16)	CO5	BTL3	Applying
12.	Explain three main approaches commonly used for Design for Testability.	(16)	CO5	BTL3	Applying
13.	Evaluate the steps involved in design for manufacturability to increase the yield of optimized circuit.	(16)	CO5	BTL3	Applying
14.	Write short notes on TAP controller of Boundary Scan Technique.	(16)	CO5	BTL3	Applying
15.	Explain the test interface and boundary scan suitable for scan design.	(16)	CO5	BTL3	Applying
16.	Write short notes on the following terms (i) Design Rule Checks (DRC) (ii) Electrical Rules Checks (ERC) (iii)Layout versus Schematic (LVS)	(16)	CO5	BTL3	Applying
17.	Describe about the Boundary Scan in detail with supporting diagrams.	(16)	CO5	BTL4	Analyzing