SRM VALLIAMMAI ENGINEERING COLLEGE
S.R.M NAGAR, KATTANKULATHUR-603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LABORATORY MANUAL

EE3369 CIRCUIT THEORY AND ELECTRONIC DEVICES LABORATORY

ACADEMIC YEAR: 2025-2026 (Even)

II YEAR - III SEMESTER

Prepared by

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EE3369 CIRCUIT THEORY AND ELECTRONIC DEVICES LABORATORY L T P C

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OBJECTIVES:

To impart knowledge on the following topics

- To gain hands on experience in Kirchhoff's laws.
- To gain knowledge on basic circuit theorems
- To learn the characteristics of basic electronic devices such as Diode.
- To learn the characteristics of BJT, FET, SCR.
- To learn the characteristics Full wave and Half wave rectifier using Pspice.

LIST OF EXPERIMENTS

Sl.No.	*EXPERIMENT NAME*
1.	Experimental verification of electrical circuit problems using Kirchhoff's voltage and current laws.
2.	Experimental verification of electrical circuit problems using Thevenin's theorem.
3.	Experimental verification of electrical circuit problems using Norton's theorem.
4.	Experimental verification of electrical circuit problems using Superposition theorem.
5.	Experimental verification of Maximum Power transfer Theorem.
6.	V-I Characteristics of PN Junction Diode.
7.	V-I Characteristics of Zener diode.
8.	Experimental verification of Common Emitter input-output Characteristics.
9.	Verification of Input and Output Characteristics Common Base Configuration using Pspice
10.	Experimental verification of FET Characteristics.
11.	Experimental verification of SCR Characteristics.
12.	Half wave Rectifier and Full wave Rectifier using Pspice.

TOTAL: 60 PERIODS

PERIODS COURSE OUTCOMES:

- Ability to Understand and Kirchhoff's laws
- Ability to understand the basic circuit theorems.
- Ability to understand basic electronic devices such as Diode.
- Ability to understand concept of BJT,FET,SCR.
- Ability to concept characteristics Full wave and Half wave rectifier using Pspice.

CONTENTS

Sl.No.	Date	Name of the Experiment	Pg.No.	Marks	Faculty Sign

Ex No: 1

Experimental verification of electrical circuit problems using Kirchhoff's voltage and current laws.

Aim:

To verify the Kirchhoff's voltage and current laws.

Apparatus Required:

Sl.No.	Item	Range	Quantity
1.	Regulated Power Supply	0-30 V	1
2.	Ammeter	0-100 mA	3
3.	Voltmeter	0-30 V	3
4.	Resistors	330Ω, 220Ω, 1KΩ,	Each 1
5.	Bread Board		1
6.	Connecting wires		Required

Theory:

Kirchhoff's Voltage Law

Kirchhoff's voltage law states that the algebraic sum of all branch voltages around any closed path in a circuit is always zero at all instants of time. $\sum_{m=1}^{M} v_m = 0$ where M is the number of voltages in the loop.

Kirchhoff's Current Law

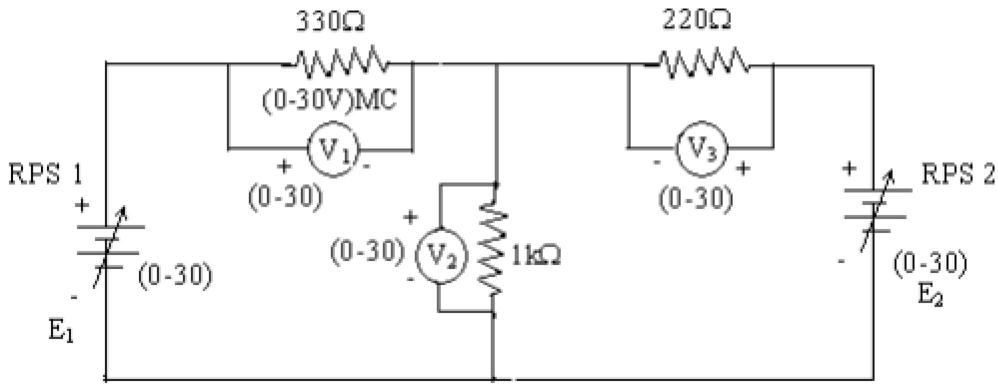
Kirchhoff's current law states that the sum of the currents entering into any node is equal to the sum of the currents leaving that node. $\sum_{n=1}^{N} i_n = 0$ where N is the number of branches connected to the node.

Procedure:

1. Connections are made as per the circuit diagram.
2. Switch on the power supply.
3. Vary the R.P.S to a specified voltage and note down the corresponding ammeter and voltmeter readings.
4. Repeat the step 3 for various R.P.S voltage and tabulate the readings.
5. **Switch off the power supply and remove the connections.**

Repeat same procedure for KCL also.

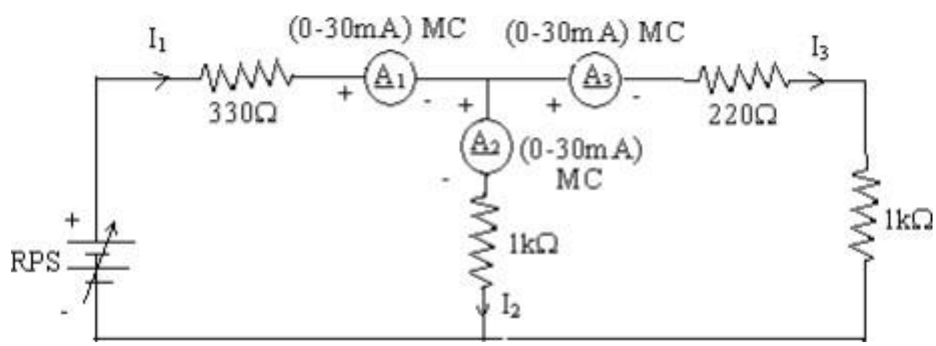
Model Circuit of KVL



Tabulation

Sl.No	RPS (V)		Voltage (V)			E_1=V1+V2(Volts)	$E_2=V_2+V_3$(Volts)
	E_1	E_2	V_1	V_2	V_3		

Model Circuit of KCL:



Tabulation:

Sl.No	Vs (volts)	I_1(A)	I_2(A)	I_3(A)	$I_1=I_2+I_3$ (A)

Review Questions:

1. Define Resistance, Inductance and capacitance.
2. Explain color coding of resistor.
3. Define active and passive elements
4. Define Unilateral and Bilateral elements.
5. Define linear and Non-Linear elements.

Result:

Thus the Kirchoff's current law and Kirchoff's voltage law are verified.

Ex No: 2

Experimental verification of electrical circuit problems using Thevenin's theorem.

Aim:

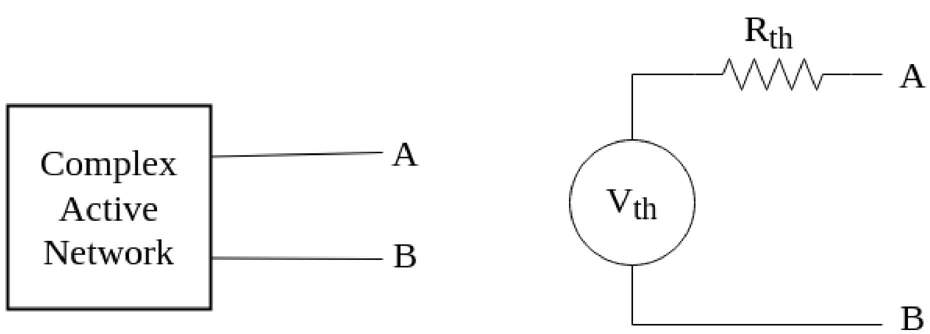
To verify the Thevenin's theorem for the given electric circuit.

Apparatus Required:

Sl.No.	Item	Range	Quantity
1.	Regulated Power Supply	(0-30) V	2
2.	Ammeter	0-10 mA	1
3.	Voltmeter	0 – 25V	2
4.	Resistors	1K Ω, 330Ω	Each 2
5.	Bread Board		1
6.	Connecting wires		Required

Theory:

A one port linear, active, resistive network which contains one or more voltage or current sources can be replaced by a single voltage source V_{th} in series with a single resistance R_{th}. V_{th} is equal to the open circuit voltage across the port terminals of the network & the resistance R_{th} is measured between the port terminals with all the energy sources replaced by their internal resistance.



R_{th}-Thevenin's resistance, V_{th} -Thevenin's voltage.

Procedure:

1. Connections are given as per the circuit diagram.
2. Set a particular value of voltage using RPS and note down the corresponding ammeter readings.

To Find V_{th}:

3. Remove the load resistance and measure the open circuit voltage using multimeter (V_{Th}).

To Find R_{th}:

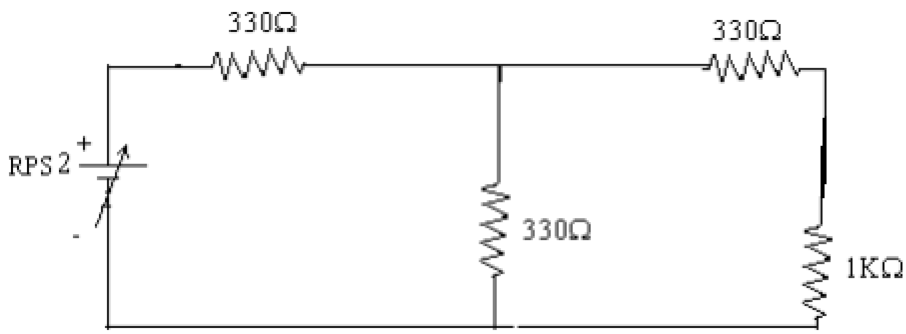
4. To find the Thevenin's resistance, remove the RPS and short circuit it and find the R_{Th} using multimeter.

5. Give the connections for equivalent circuit and set VTH and RTH and note the corresponding ammeter reading.
6. Verify Thevenins theorem.

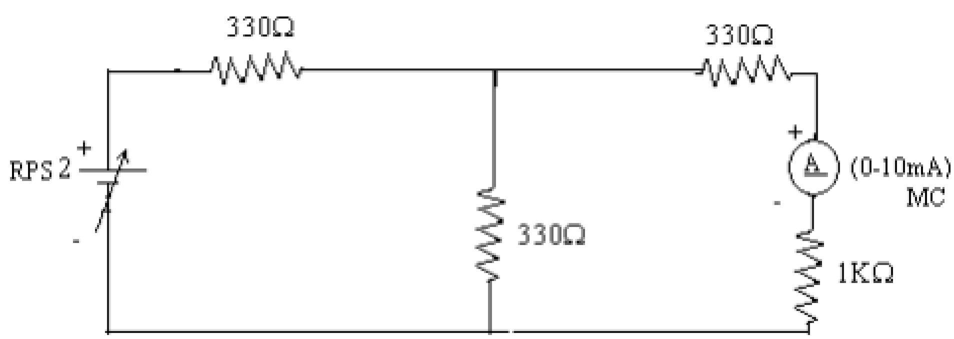
To Find I_L:

7. Vary the RPS to the particular voltage and note down the ammeter reading (I_L).

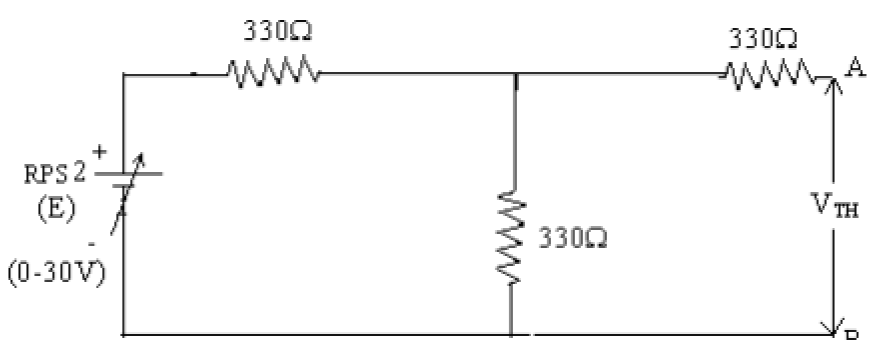
Circuit diagram:



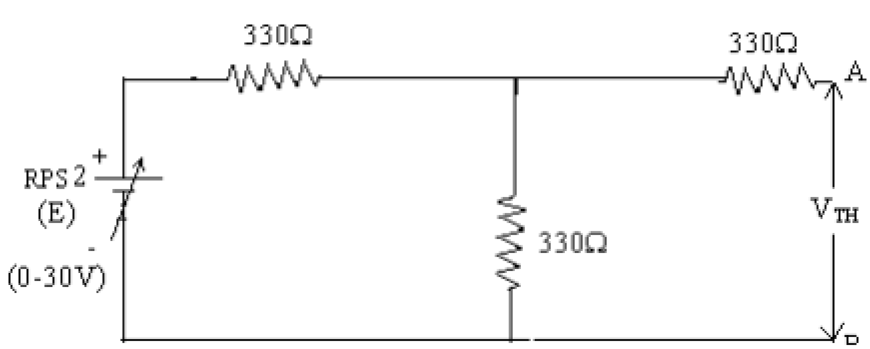
To find load current (I_L)



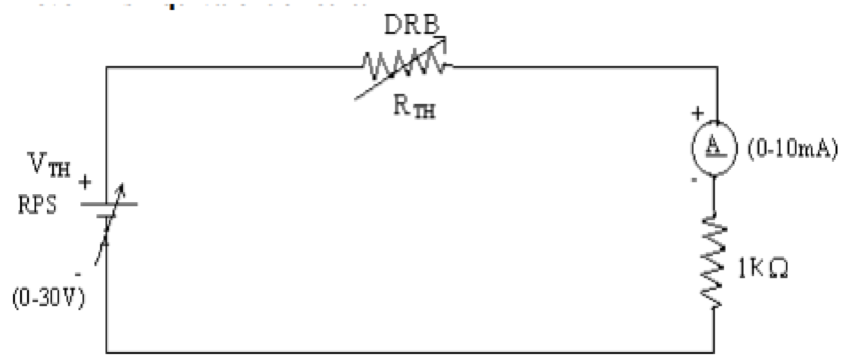
To find V_{th}



To find R_{th}



Thevenin's Equivalent circuit:

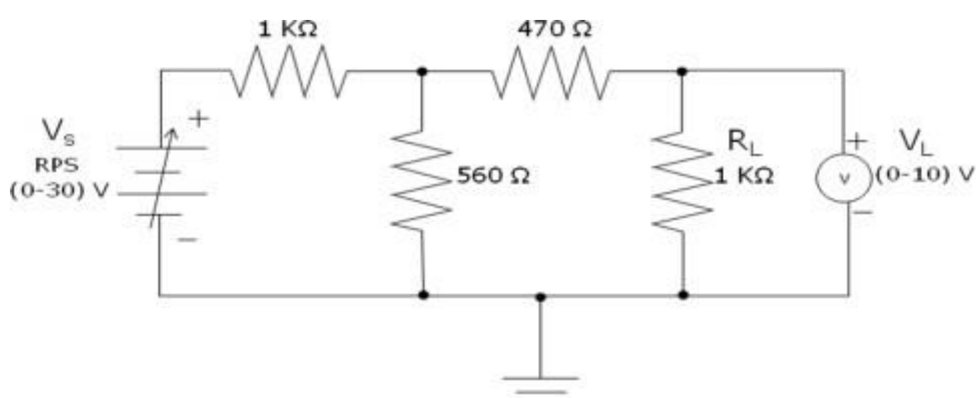


Tabulation:

Sl.No	Specified voltage E (Volts)	Theoritical			Practical		
		V_{th}	R_{th}	I_L	V_{th}	R_{th}	I_L

Review Question

1. State Thevenin's theorem.
2. Draw the Thevenin's equivalent circuit for the given below certificate.



3. What is duality theorem?
4. Explain dependent sources and sources transformation.
5. Explain Star-Delta conversion

Result:

Thus the Thevenin's theorem is verified

Ex No: 3

Experimental verification of electrical circuit problems using Norton's theorem

Aim:

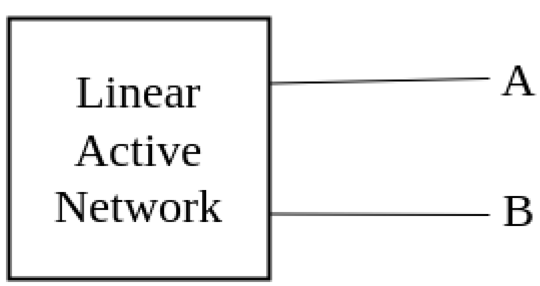
To verify the Norton's theorem for the given electric circuit.

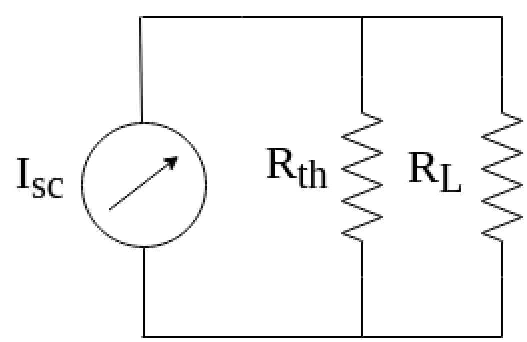
Apparatus Required:

Sl.No.	Item	Range	Quantity
1.	Regulated Power Supply	(0-30) V	2
2.	Ammeter	0-10 mA	1
3.	Voltmeter	0 – 25V	2
4.	Resistors	1K Ω, 330Ω	Each 2
5.	Bread Board		1
6.	Connecting wires		Required

Theory:

A one port linear, active, resistive network which contains one or more voltage or current sources can be replaced by a single current source I_{SC} in parallel with a single resistance R_{th}. I_{sc} is equal to the short circuit current across the port terminals of the network & the resistance R_{th} is measured between the port terminals with all the energy sources replaced by their internal resistance.





Where,

I_{SC} – Short circuit current at terminals A & B

R_{th} – Thevenin's equivalent Resistance.

Procedure

To find I_{SC} (short circuit the load resistance)

a. Connections are made as per the circuit diagram.
b. Note down the ammeter reading (I_{SC})

To find R_{th} (short circuit the voltage source)

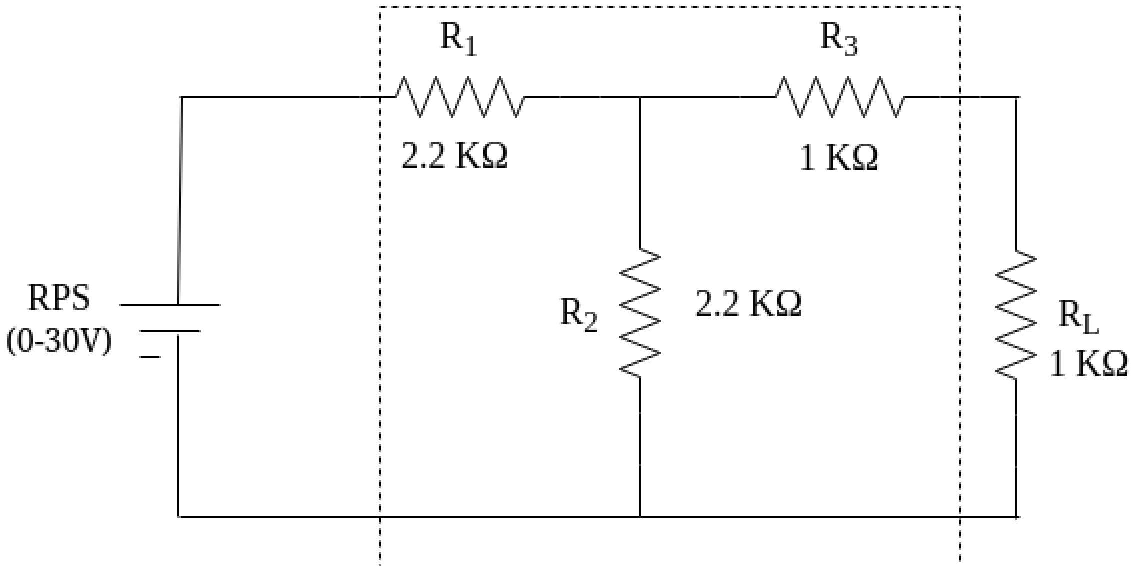
1. Connections are made as per the circuit diagrams
2. Supply is switched 'ON'

3. Vary the RPS to the specified voltage, note down the ammeter and voltmeter readings.
4. Repeat the step 3 for various R.P.S voltage and the readings are tabulated.
5. Calculate the R_{Th} using the tabulation.

To Find I_L

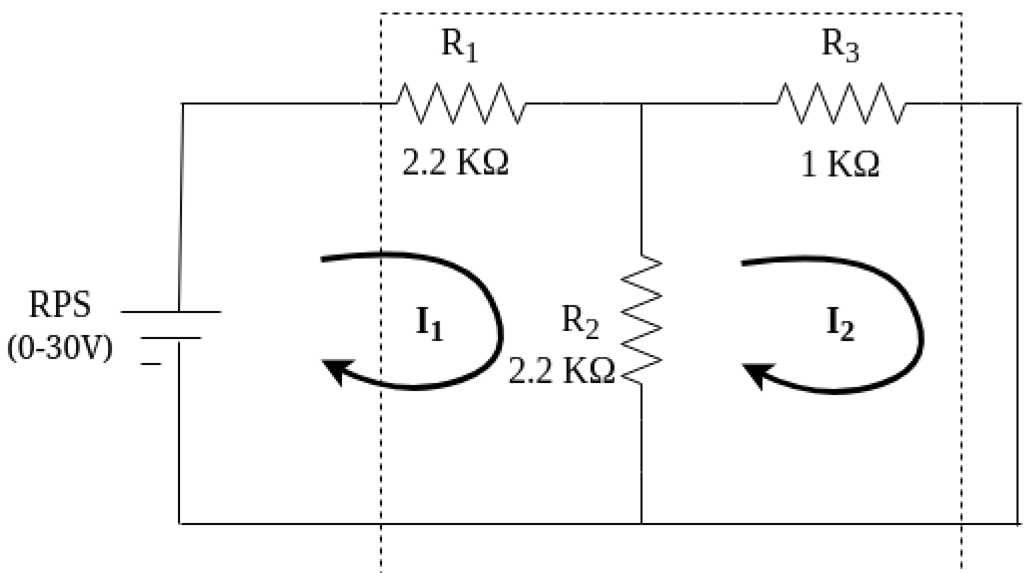
1. Connections are given as per the circuit diagram.
2. Switch ON the power supply.
3. Vary the R.P.S. to the specified voltage and note down the ammeter reading (I_L).

CIRCUIT DIAGRAM:



Theoretical Verification:

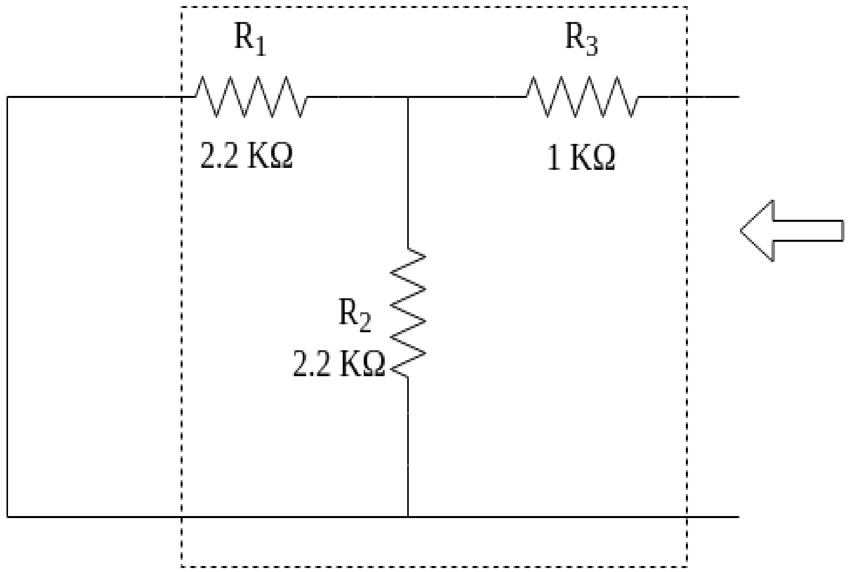
To Find I_{SC}:



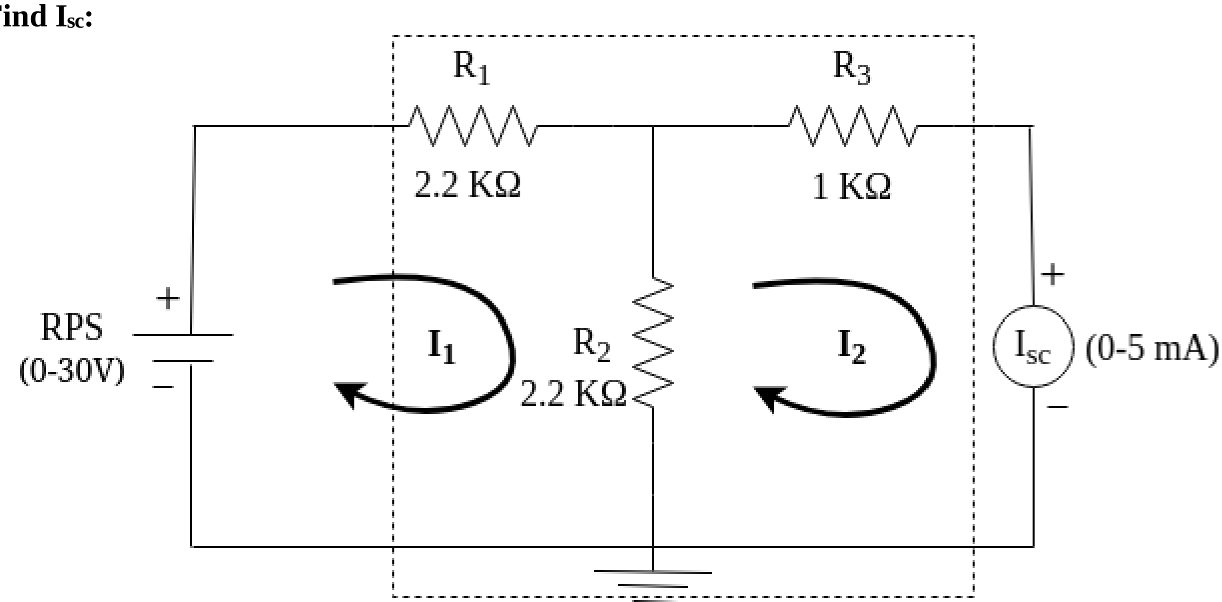
$$I_{SC} = I_2 = \frac{\Delta_2}{\Delta}$$

To Find R_{TH}:

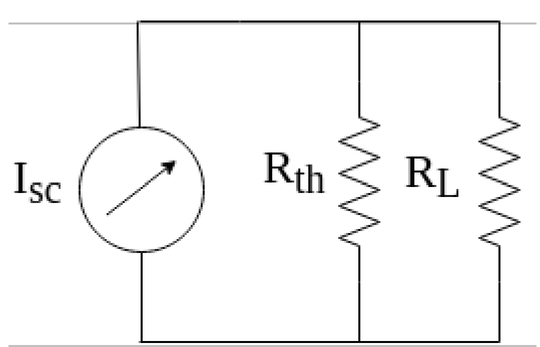
$$R_{TH} = \frac{(R_1 R_2)}{R_1 + R_2} + R_3$$



To Find I_{SC}:

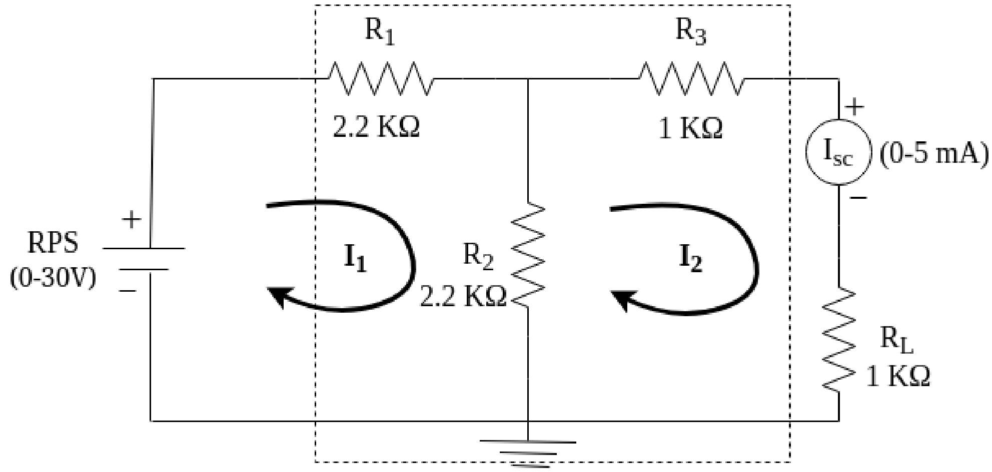


To Find I_L:



$$I_L = I_{SC} \frac{R_{TH}}{R_L + R_{TH}}$$

To Find I_L:

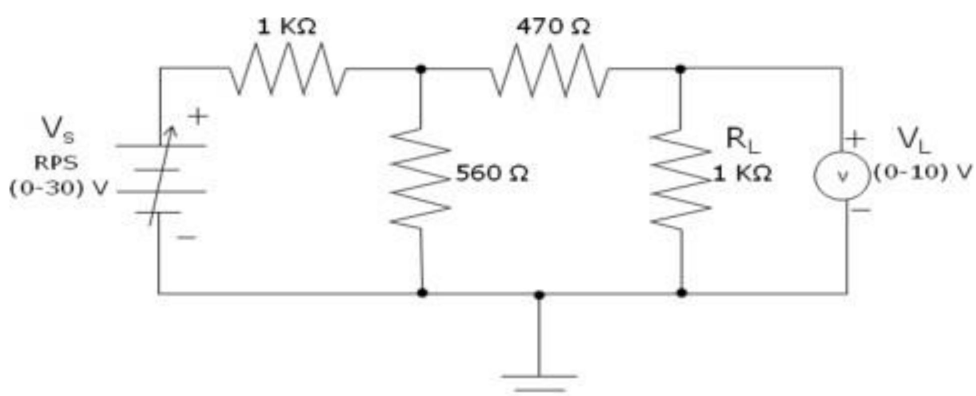


Tabulation:

Sl.No	Specified voltage (Volts)	Theoritical			Practical		
		I_{sc}	R_{th}	I_L	I_{sc}	R_{th}	I_L

Review Questions:

1. State Norton's theorem.
2. Draw the Norton's equivalent circuit for



3. What is duality theorem?
4. Explain dependent sources and sources transformation.
5. Explain Star-Delta conversion.

Result:

Thus the Norton's theorem is verified.

Ex No: 4

Experimental verification of electrical circuit problems using Superposition theorem.

Aim:

To verify the superposition theorem for the given electric circuit.

Apparatus required:

S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30) V	1
2	Ammeter	(0-1) mA	1
3	Resistors	10KΩ, 22KΩ,5.8KΩ	Each 2
4	Connecting wires		Required
5	Breadboard		1

Theory:

In a linear lumped element, bilateral electric circuit energized by two or more sources, the current in any resistor is equal to the algebraic sum of the separate currents in each resistor when each source act, separately.

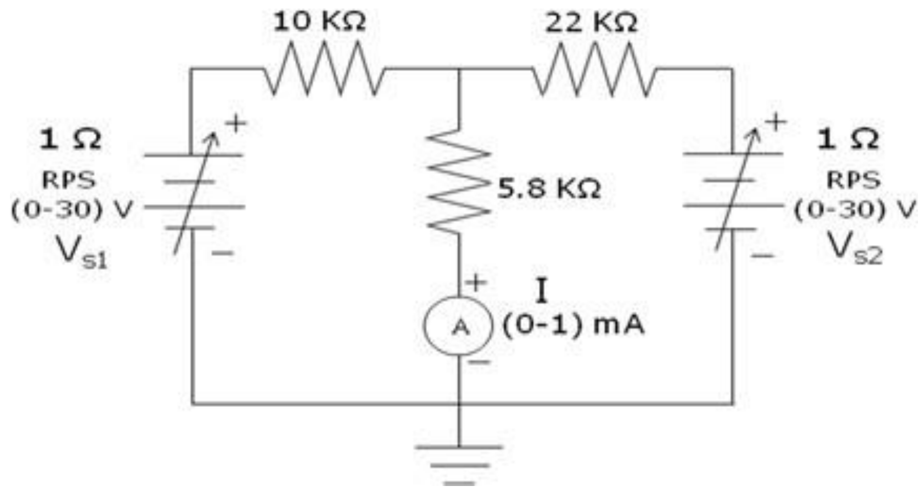
The Voltage sources are short-circuited and the current sources are open circuited in order to replace the other sources by their respective internal resistances.

Procedure:

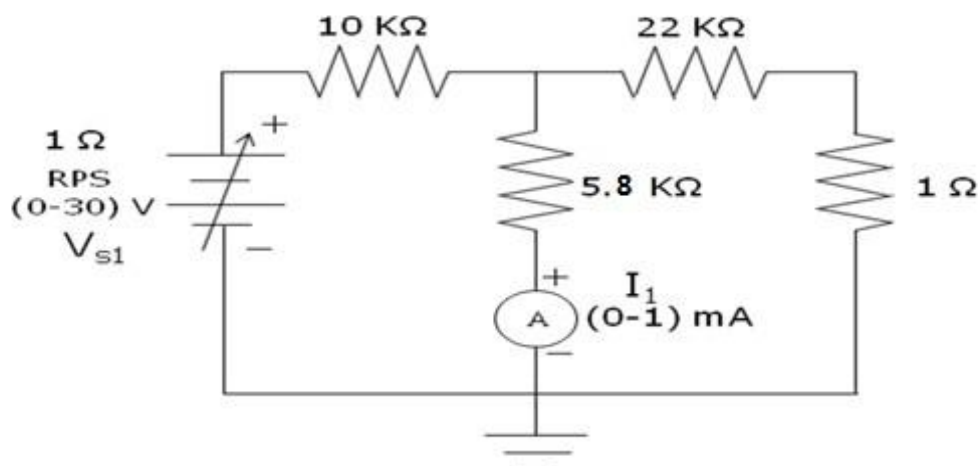
To find I, I_1 & I_2:

1. Connections are given as per the circuit diagram.
2. Switch on the power supply.
3. Set a particular voltage value using V_{S1} and V_{S2} & note down the ammeter reading.
4. Set the same voltage in using V_{S1} alone and short circuit the terminals and note the ammeter reading.
5. Set the same voltage in V_{S2} alone as in circuit I and note down the ammeter reading.
6. Verify superposition theorem.

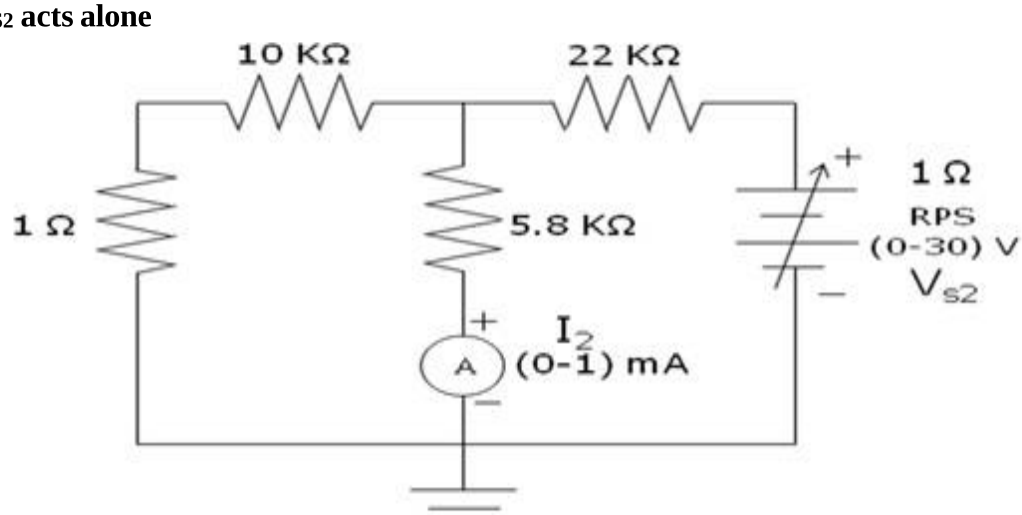
(a) When both V_{S1} & V_{S2} are active



(b) When V_{S1} acts alone



(c) When V_{S2} acts alone



Tabulation:

V_{S1} (volts)	V_{S2} (volts)	Theoretical				Practical			
		I (mA)	I_1 (mA)	I_2 (mA)	$I = I_1 + I_2$ (mA)	I (mA)	I_1 (mA)	I_2 (mA)	$I = I_1 + I_2$ (mA)

Review Questions:

1. State superposition theorem.
2. What is duality theorem?
3. Explain dependent sources and sources transformation.
4. Explain Star-Delta conversion
5. State voltage division rule & State current division rule.

Result:

Thus the superposition theorem is verified.

Ex No: 5

Experimental verification of Maximum Power transfer Theorem

Aim:

To practically verify the maximum power transfer theorem for the network with the theoretical value.

Apparatus Required:

S.No	Name	Range	Qty
1	RPS (Regulated Power Supply)	(0-30) V	1
2	DRB	(0-10)KΩ	1
3	Voltmeter	0 –5V	1
4	Connecting wires		Required
5	Resistors	1KΩ, 2.2KΩ	Each 1
6	Breadboard		1

Theory:

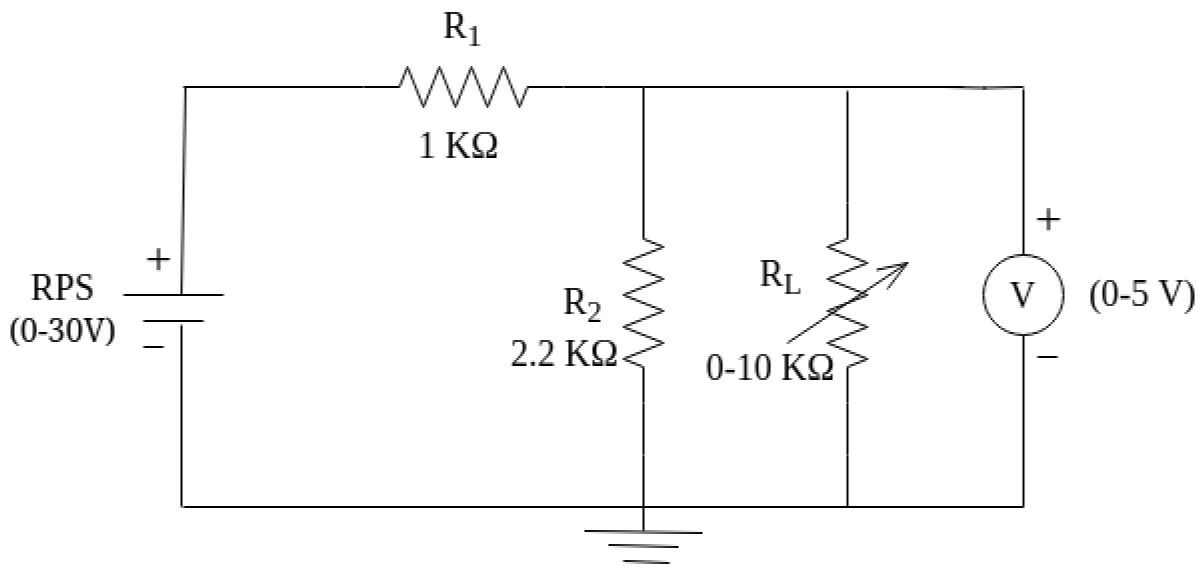
This theorem states that maximum power will be delivered from a voltage source to a load when the load resistance is equal to the internal resistance of the source.

$$\textbf{Max. Power transferred} = \frac{V^2_{th}}{4\,R_{th}}$$

Procedure:

1. Remove the portion of network through which power has to be transferred.
2. Name those terminals as A and B.
3. Calculate R_{th} by substituting all sources with internal resistance working back at network
4. Give the connections as per the circuit diagram.
5. By varying the DRB (R_L) for values of R_L, measure the current through R_L.
6. Calculate the power delivered to R_L.
7. Verify resistance (R_L) at $P_{L(max)}$ is equal to Rth.

Circuit Diagram:

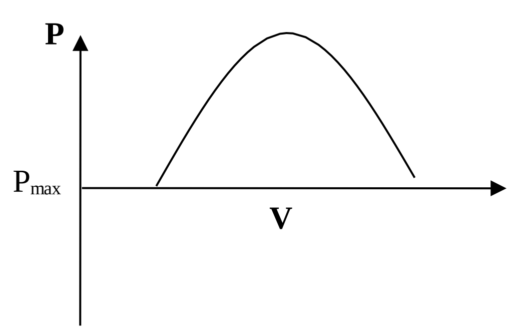


Tabulation

Experimental values:

$R_L(\Omega)$	V_{th}(v)	$P=V_{th}^2/4R_L$ (w)

Model Graph:



Review Questions:

1. State Maximum Power transfer theorem.

Result:

Hence the maximum power transfer for the given network is experimentally verified.

Ex No: 6

V-I Characteristics of PN Junction Diode

Aim:

To determine the VI characteristics of PN Diode.

Apparatus Required:

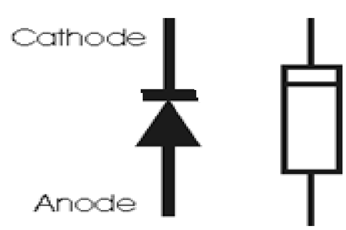
Sl.No	Item	Range	Qty
1	RPS (Regulated Power Supply)	(0-30)V	1
2	Ammeter	(0-5)mA, (0-25)mA	1 1
3	Voltmeter	(0-10)V (0-1)V	1 1
4	Connecting wires	-	Required
5	Bread Board		1
6	Resistors	1KΩ	1
7	Diode- PN	BY127	1

Apparatus Required:

A diode is a PN junction formed by a layer of P type and layer of N type Semiconductors. Once formed the free electrons in the N region diffuse across the junction and combine with holes in P region and so a depletion layer is developed. The depletion layer consists of ions, which acts like a barrier for diffusion of charged beyond a certain limit. The difference of potential across the depletion layer is called the barrier potential. The barrier potential approximately equal 0.7v for silicon diode and 0.3v for germanium diode.

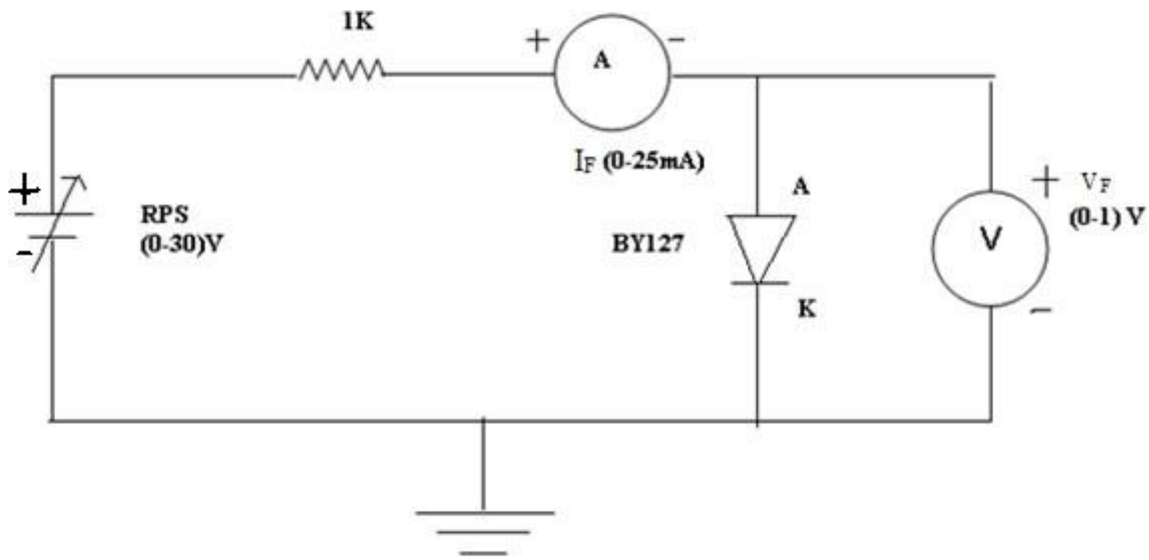
Then the junction is forward bias, the majority carrier acquired sufficient energy to overcome the barrier and the diode conducts. When the junction is reverse biased the depletion layer widens and the barrier potential increases. Hence the Majority carrier cannot cross the junction and the diode does not conduct. But there will be a leakage current due to minority carrier. When diode is forward biased, resistance offered is zero, and when reverse biased resistance offered is infinity. It acts as a perfect switch.

Pin diagram:

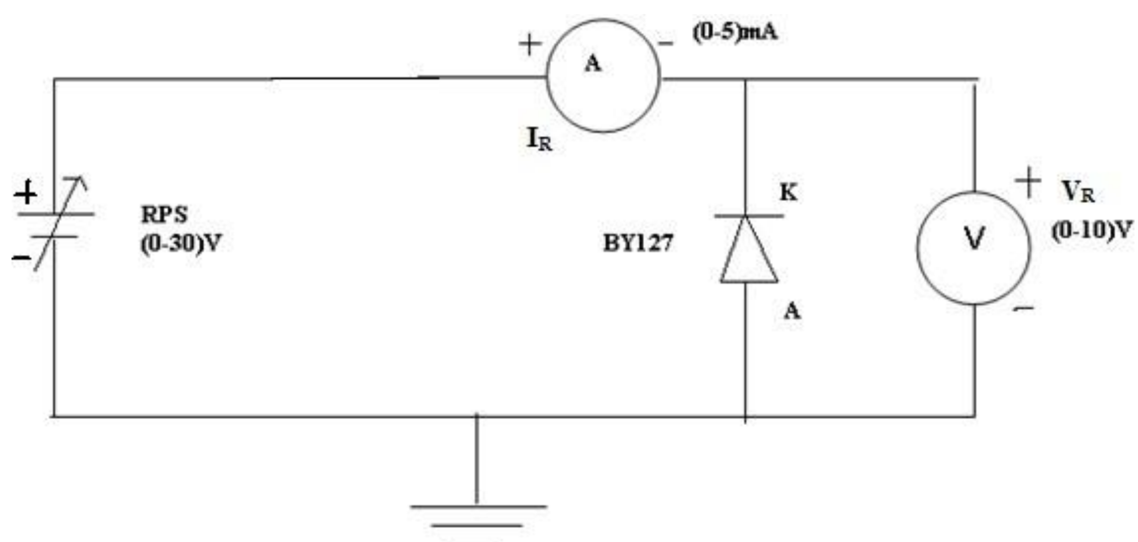


Circuit diagram:

Forward bias:



Reverse Bias:



Procedure:

Forward bias:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

Reverse Bias:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

Tabulation:

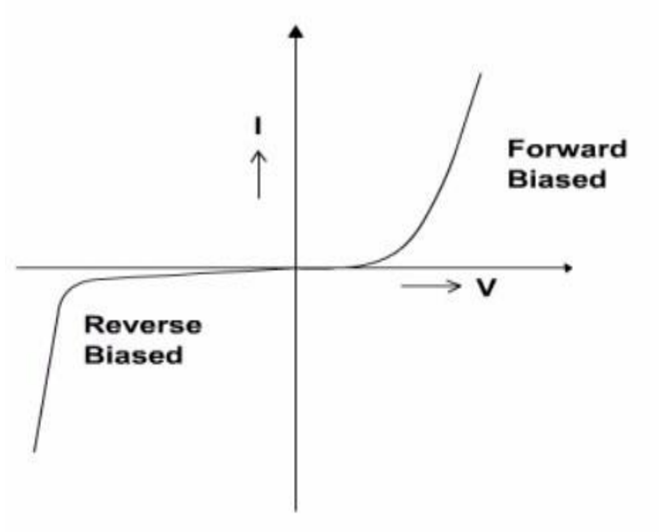
Forward bias:

V_f(volts)	**I_f(mA)**

Reverse bias:

V_r(volts)	**I_r(mA)**

Model Graph:



Review Questions:

1. How a PN junction is formed?
2. In what way the width of depletion region can be varied?
3. What is potential barrier?
4. In forward bias condition the current condition is due to_______
5. What is reverse saturation current Ico?

Result:

Thus the characteristics of PN-Junction diode were drawn**.**

Ex No: 7

V-I Characteristics of Zener Diode

Aim:

To determine the V-I characteristics of Zener Diode.

Apparatus Required:

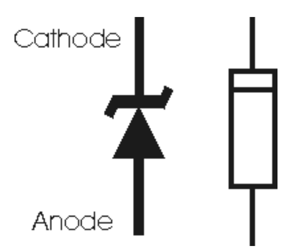
S.No	Item	Range	Qty
1	RPS	(0-30)V	1
2	Ammeter	(0-30) mA	1
3	Voltmeter	(0-10)V (0-1)V	1 1
4	Connecting wires	-	As Required
5	Bread Board		1
6	Resistors	1KΩ	1
7	Diode- Zener	FZ 5V6/ FZ 6V2	1

Theory:

Zener diodes have many of the same basic properties of ordinary semiconductor diodes. When forward biased, they conduct in the forward direction and have the same turn on voltage as ordinary diodes. For silicon this is about 0.6 volts.

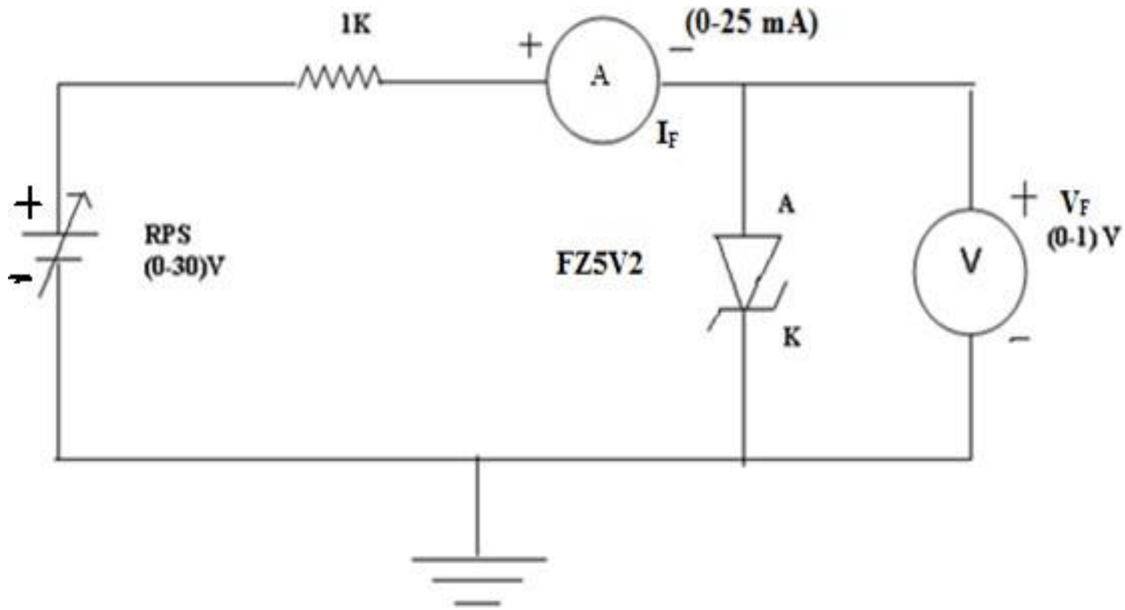
In the reverse direction, the operation of a Zener diode is quite different to an ordinary diode. For low voltages the diodes do not conduct as would be expected. However, once a certain voltage is reached the diode "breaks down" and current flows. Looking at the curves for a Zener diode, it can be seen that the voltage is almost constant regardless of the current carried. This means that a Zener diode provides a stable and known reference voltage. Hence they are used as Voltage regulators.

Pin diagram:

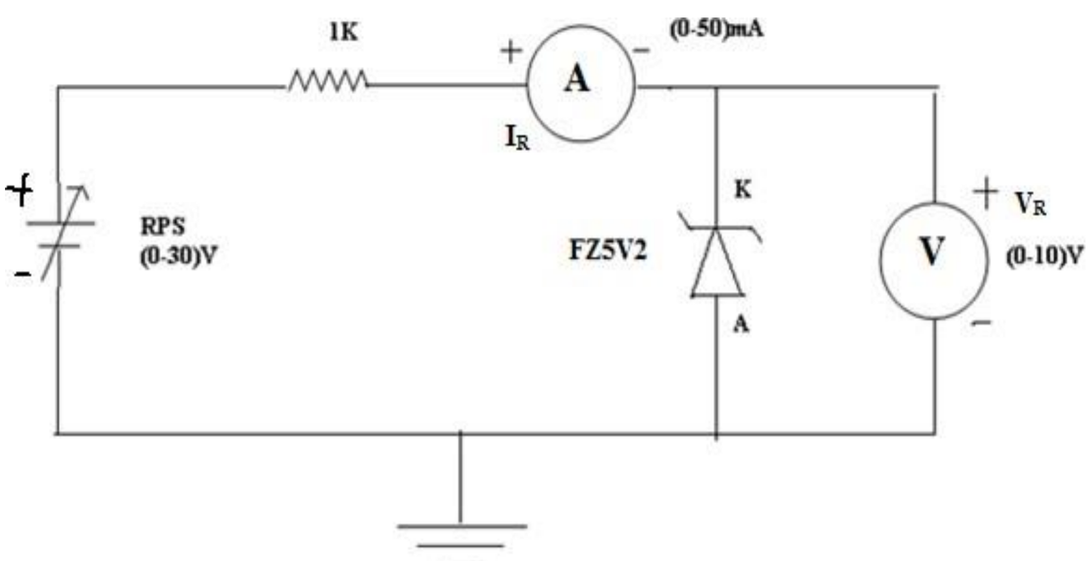


Circuit diagram:

Forward bias:



Reverse Bias:



Procedure:

Forward Bias:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to anode of the diode and negative terminal to cathode of the diode.
3. Forward voltage V_f across the diode is increased in small steps and the forward current is noted.
4. The readings are tabulated. A graph is drawn between V_f and I_f.

Reverse Bias:

1. The connections are made as per the circuit diagram.
2. The positive terminal of power supply is connected to cathode of the diode and negative terminal to anode of the diode.
3. Reverse voltage V_r across the diode is increased in small steps and the Reverse current is noted.
4. The readings are tabulated. A graph is drawn between V_r and I_r.

Tabular column:

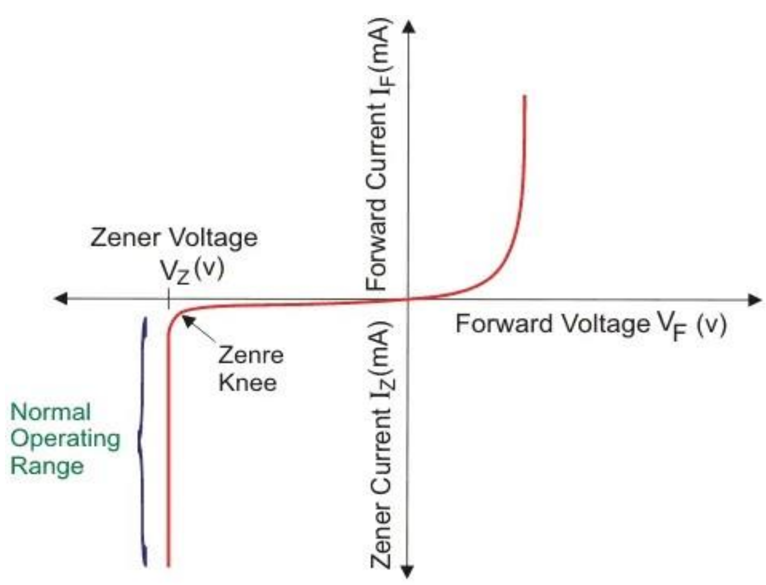
Forward bias:

V_f(volts)	I_f(mA)

Reverse bias:

V_r(volts)	I_r(mA)

Model Graph:



Review Questions:

1. What is the difference between p-n Junction diode and zener diode?
2. Can we use Zener diode as a switch?
3. Explain working of a Zener Diode.
4. What is the max value of voltage of Zener breakdown devices?
5. What is cause of reverse breakdown?

Result:

Thus the characteristics of Zener diode were drawn**.**

Ex No: 8

Experimental verification of Common Emitter input-output characteristics.

Aim:

To plot the transistor characteristics (INPUT & OUTPUT) of CE configuration.

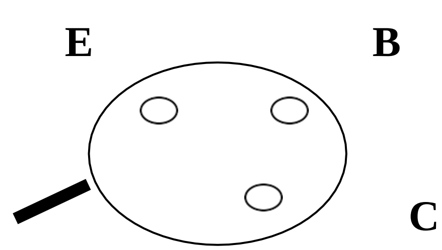
Apparatus Required:

S.No.	ITEM	SPECIFICATION	QTY
1	Transistor (BC 107)	Max Rating : 50V 1A, 3W	1
2	Resistors	10Kfi,100Ω	2
3	RPS (Regulated power supply)	(0-30) V	1
4	Voltmeters	(0-10) V (0-1) V	1 1
5	Ammeters	(0-30) mA (0-100)µA	1 1
6	Bread board		1
7	Connecting wires		Required

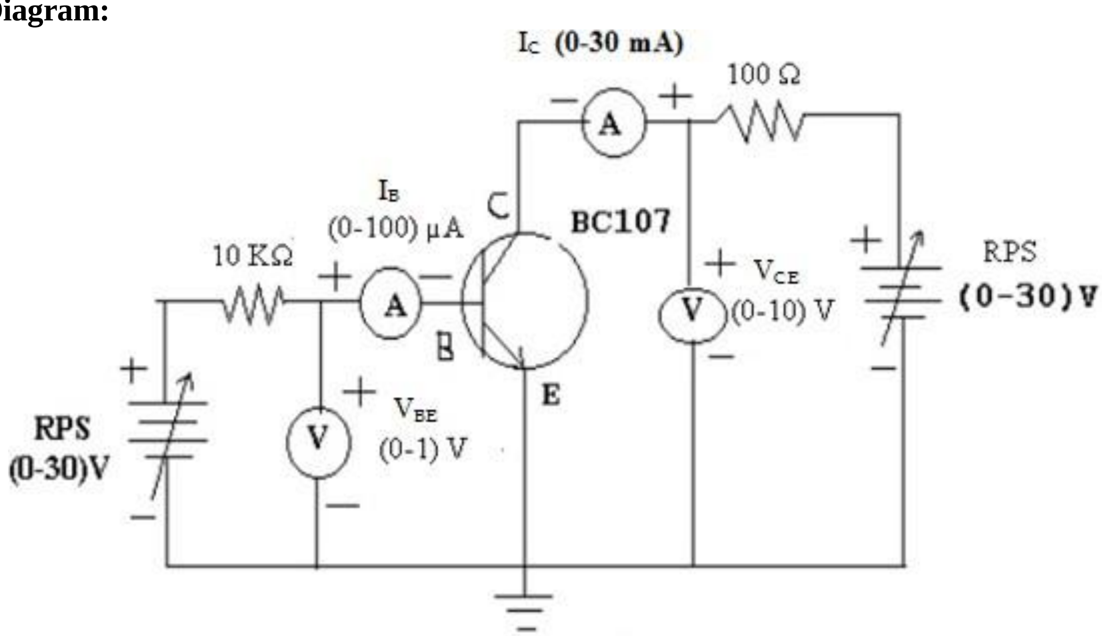
Theory:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CE configuration, Emitter is common to both the Emitter and Base.

Pin Diagram of BC107:



Circuit Diagram:



DESCRIPTION:

Input Characteristics:

Voltage across Base Emitter junction V_{BE} vs I_B, where V_{CE} is constant

Output Characteristics:

Voltage across Collector Emitter junction V_{CE} vs I_C where I_B is constant.

PROCEDURE:

Input Characteristics:

1. Connections are made as per the circuit diagram.
2. V_{CE} is kept constant (say 2v), V_{BE} is varied insteps of 0.1v and the corresponding I_B values are tabulated. The above procedure is repeated for 1V etc.
3. Graph is plotted between V_{BE} vs I_B, where V_{CE} constant.

Output Characteristics:

1. Connection are made as per the circuit diagram
2. I_B is kept constant, V_{CE} is varied in step IV the corresponding I_C values are tabulated. The above procedure is repeated for different constant values.
3. Graph is plotted between V_{CE} and Ic for a constant I_B.

Tabulation:

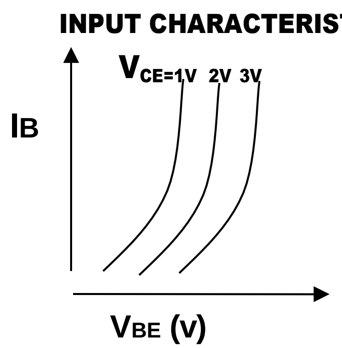
Input Characteristics:

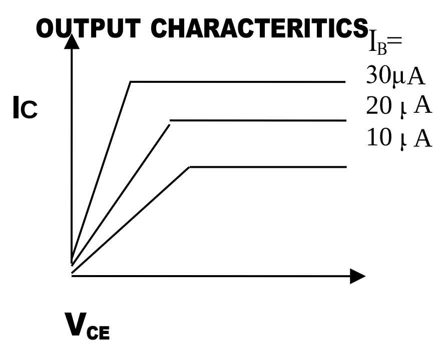
V_{CE} = V		V_{CE} = V	
V_{BE}(V)	I_B (μA)	V_{BE}(V)	I_B(μA)

Output characteristics:

I_B = μA		I_B = μA	
V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C(mA)

<u>MODEL GRAPH:</u>





<u>Review Questions:</u>

1. List the current components of BJT in CE configuration
2. What is Early Effect?
3. Why the doping of collector is less compared to emitter?
4. What do you mean by “reverse active”?
5. What is the difference between CE and Emitter follower circuit?

<u>RESULT:</u>

Thus the input and output characteristic of BJT in Common Emitter mode is drawn.

Ex No: 9

Verification of Input and Output Characteristics Common Base Configuration using PSPICE

Aim:

To plot the transistor characteristics (INPUT & OUTPUT) of CB configuration using PSPICE.

Software Tool:

PC loaded with PSPICE Tool

Theory:

A NPN function transistor consist of a silicon (or germanium) crystal in which a layer of p – type silicon is sandwiched between two layers of N – type silicon. The arrow on emitter lead specifies the direction of the current flow when the emitter – base function is biased in the forward direction since the conductivity of the BJT depends on both the majority and minority carriers it is called bipolar device. In CB configuration, base is common to both the emitter and collector. The bipolar junction transistor model in SPICE is an adaptation of the integral charge control model of Gummel and Poon. This modified Gummel-Poon model extends the original model to include several effects at high bias levels. The model will automatically simplify to the simpler Ebers-Moll model when certain parameters are not specified.

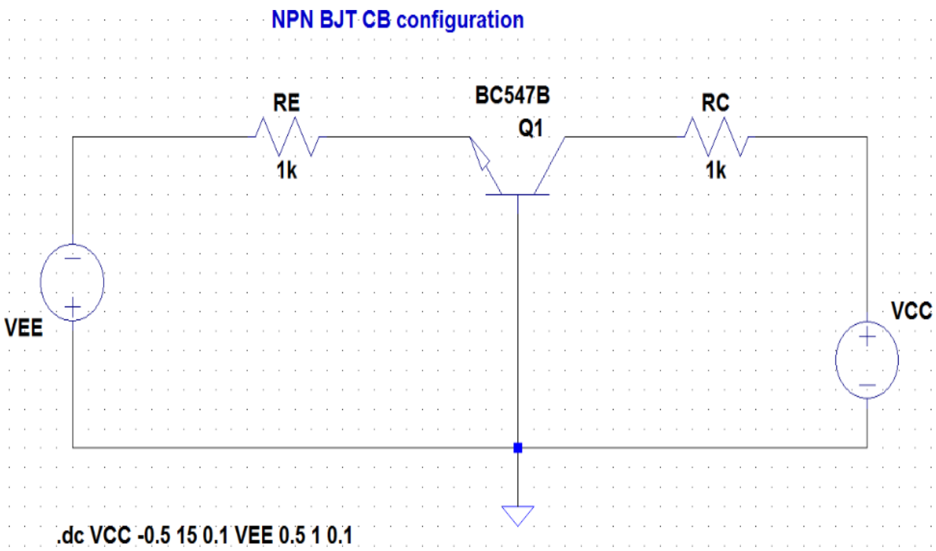
The dc model is defined by the parameters IS, BF and NE which determine the forward current gain characteristics, IS, BR and NC which determine the reverse current gain characteristics, and VAF and VAR which determine the output conductance for forward and reverse regions. Three ohmic resistances RB, RC, and RE are included, where RB can be high current dependent. Base charge storage is modeled by forward and reverse transit times, TF and TR, the forward transit time TF being bias dependent if desired, and nonlinear depletion layer capacitances which are determined by CJE and VJE for the B-E junction , CJC and VJC for the B-C junction and CJS and VJS for the C-S (Collector-Substrate) junction. The BJT parameters used in the modified Gummel-Poon model are listed below.

Modified Gummel-Poon BJT Parameters.

	name	parameter	units	default	example
	-----	----------		------	--------
1	IS	transport saturation current	A	1.0E-16	1.0E-15
2	BF	ideal maximum forward beta	-	100	100
3	VAF	forward Early voltage	V	infinite	200
4	ISE	B-E leakage saturation current	A	0	1.0E-13
5	NE	B-E leakage emission coefficient	-	1.5	2
6	BR	ideal maximum reverse beta	-	1	0.1
7	VAR	reverse Early voltage	V	infinite	200
8	ISC	B-C leakage saturation current	A	0	1.0E-13
9	NC	B-C leakage emission coefficient	-	2	1.5
10	RB	zero bias base resistance	Ohms	0	100
11	RE	emitter resistance	Ohms	0	1
12	RC	collector resistance	Ohms	0	10
13	CJE	B-E zero-bias depletion capacitance	F	0	2PF
14	VJE	B-E built-in potential	V	0.75	0.6
15	TF	ideal forward transit time	sec	0	0.1Ns

16	CJC	B-C zero-bias depletion capacitance	F	0	2PF
17	VJC	B-C built-in potential	V	0.75	0.5
18	TR	ideal reverse transit time	sec	0	10Ns
19	CJS	zero-bias collector-substrate capacitance	F	0	2PF
20	VJS	substrate junction built-in potential	V	0.75	

Circuit diagram



Simulation Results:

Review Questions:

1. Bring out the comparison of CC and CB transistor parameters
2. Give the relation of Ebers moll equation.
3. Bring out the comparison of CE and CB transistor parameters
4. Draw input and output characteristics of CB?
5. Explain Gummen poll model

RESULT:

Thus the input and output characteristic of BJT in Common Base mode using PSPICE is plotted.

Ex No: 10

Experimental verification of FET Characteristics.

Aim:

To plot the drain and transfer characteristics of JFET & to find drain resistance, transconductance, amplification factor, drain saturation current I_{DSS} and Pinch off voltage.

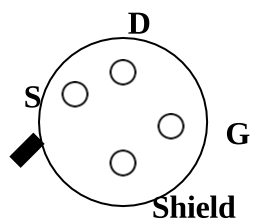
Apparatus Required:

S.No.	Item	Specification	Qty
1	FET	BFW10 I_{dss}> 8 mA, V_p<8V	1
2	Resistors	1Kfi	1
3	RPS (Regulated dual power supply)	(0-30)V	1
4	Voltmeters	(0-10)V, (0-25)V	1
5	Ammeters	(0-25) mA	1
6	Bread board		1
7	Connecting wires		Required

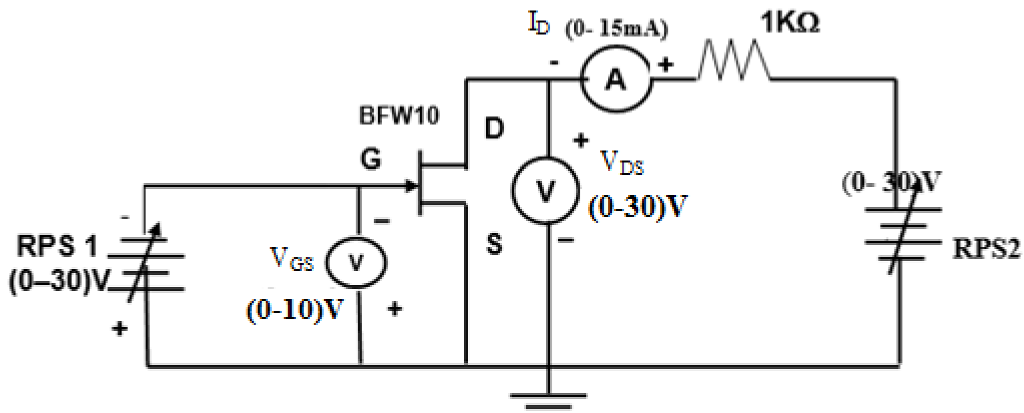
Theory:

Field effect transistor is a semiconductor device that depends for its operation on the control of current by an electric field. Its operation depends on the flow of majority carriers only. It is therefore a unipolar device. It exhibits a high input resistance. An N- channel JFET consists of a N-type bar is sandwiched between two heavily doped Persians. Due to the concentration gradient, the depletion region formed. On both sides of the semiconductor bar the ohmic contacts are made. One terminal is called source & other is called drain. Both the p-type regions are connected together.

Pin diagram of BFW10



Circuit Diagram



Description:

Drain characteristics

INPUT: Drain voltage V_{DS} is varied insteps of 1V, V_{GS} is kept constant.

OUTPUT: Drain current I_D.

Transfer characteristics

INPUT: Gate – source voltage V_{GS} is varied, Drain –source voltage V_{DS} is kept constant.

OUTPUT**:** Drain current I_D.

Procedure:

Drain Characteristics:

1. Connections are made as per the circuit diagram.
2. Gate –source voltage V_{GS} is kept constant (say –1v), drain voltage V_{DS} is varied insteps of 1v and the corresponding drain current I_D values are tabulated.
3. The above procedure is repeated for V_{GS}= -2v, 0v.
4. The graph is plotted V_{DS} and I_D for a constant V_{GS}.
5. The drain resistance is found from the graph

$$r_d = \Delta V_{DS} / \Delta I_D$$

Transfer Characteristics:

6. Connections are made as per the circuit diagram.
7. Drain –source voltage V_{DS} is kept constant (say 5v), the gate – source voltage V_{GS} is varied insteps of 1v (-VE voltage) and the corresponding drain current I_D values are tabulated.

8. The above procedure is repeated for V_{DS} = 10v, 15v,
9. Graph is plotted between V_{GS} and I_D for a constant V_{DS}.
10. The trans conductance is found from the graph

$$g_m = \Delta I_D/\Delta V_G$$

Tabulation:

Drain characteristics

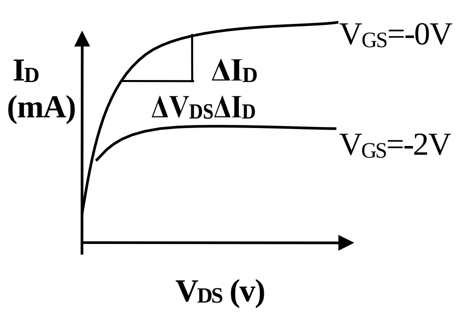
V_{GS} = V		V_{GS} = V	
V_{DS} (V)	**I_D (mA)**	**V_{DS} (V)**	**I_D (mA)**

Transfer characteristics

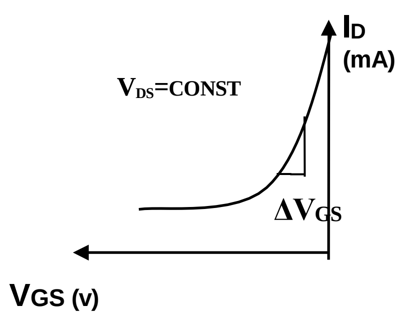
V_{DS} = V		V_{DS}= V	
V_{GS} (V)	**I_D (mA)**	**V_{GS} (V)**	**I_D (mA)**

Model Graph:

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



CALCULATION

Transconductance $g_m = \Delta I_D / \Delta V_G$

Drain resistance $r_d = \Delta V_{DS} / \Delta I_D$

Amplification factor $\mu = g_m r_d$

Review Questions:

1. Define VVR.
2. Why MOSFET is preferred than FET?
3. What are the differences between FET & MOSFET?
4. What are the applications of FET?
5. Why FET is called us voltage controlled device

RESULT:

Thus the drain and transfer for characteristics of JFET is drawn.

Drain resistance r_d =

Trans conductance g_m =

Amplification factor =

Ex No: 11

Experimental verification of SCR Characteristics

Aim:

To construct a circuit using SCR to draw its Firing Characteristics.

Apparatus required:

S.No	Components	Specification	Quantity
1	SCR	(TYN616)	1
2	Dual RPS	(0-30)V	2
3	Resistor	10KΩ, 1KΩ	1 each
4	Ammeter	(0-200)mA	2
5	Voltmeter	(0-20)V	1
6	Bread board		1

Theory:

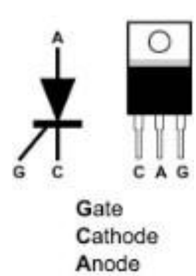
The SCR consists of four layers of semiconductor material alternatively P type and N type. It can be brought of as an ordinary rectifier with a control element .The control element is called GATE. The gate current determines the anode to cathode voltage at which the device starts to conduct.

It means that gate terminal of the SCR is controlled by the applied voltage. Once switched ON the gate has no further control. To switch the SCR the anode current has to be reduced below a certain level called HOLDING CURRENT.

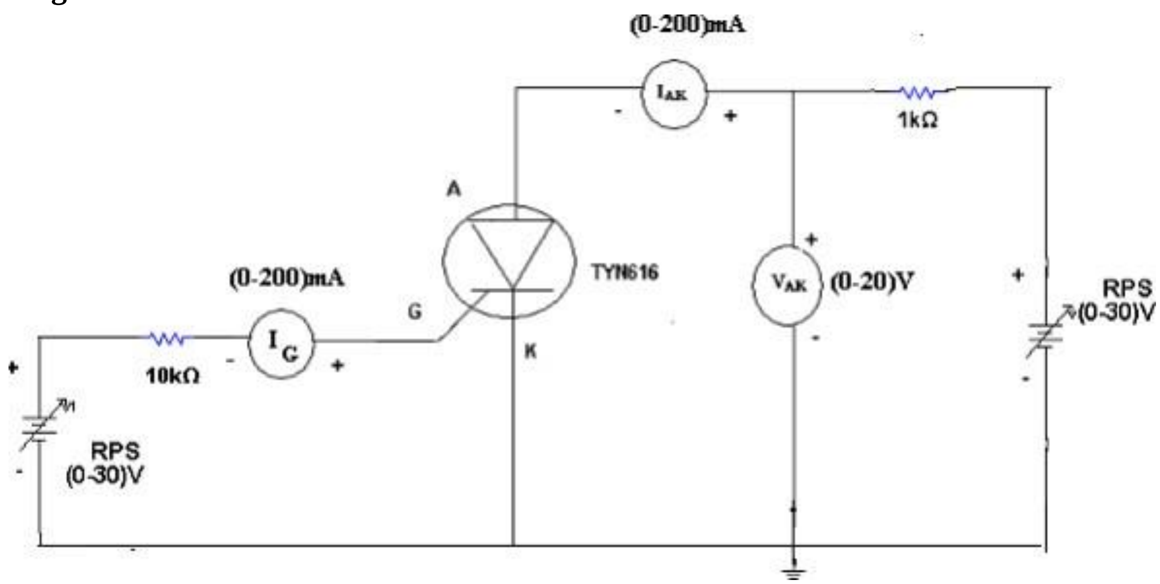
The SCR can be triggered ON with the gate or amplitude triggering, pulse triggering methods. The terms ON & OFF are used to represent the conduction and blocking mode of SCR respectively open circuited with the anode to cathode voltage made large enough .In conduction state the SCR behaves as an ordinary diode.

The anode to cathode voltage at which the SCR conducts is called BREAK OVER VOLTAGE or FORWARD BLOCKING VOLTAGE. It has great switching speed than other devices.

Pin Diagram:



Circuit Diagram:



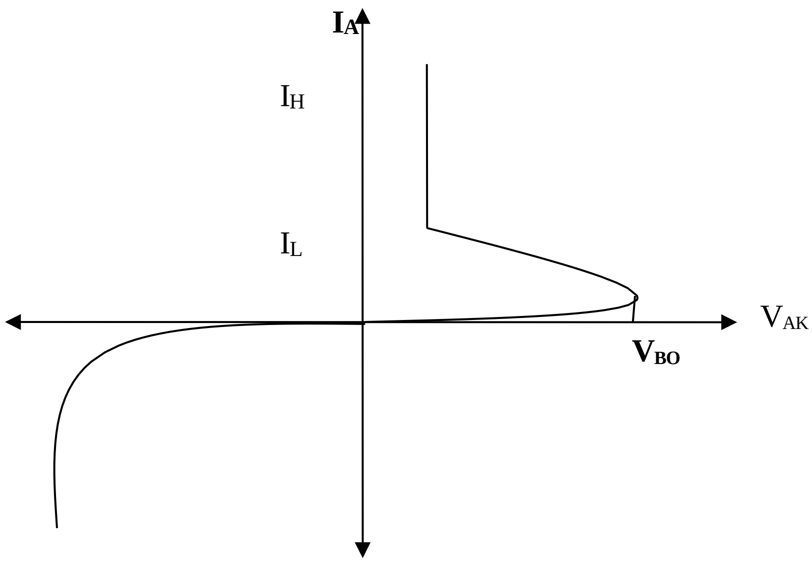
Procedure:

1. All the connections are made as per the circuit diagram.
2. Keep the gate current (I_G) open i.e. $I_G = 0$ mA.
3. Vary the anode to cathode supply voltage and note down the readings of Voltage V_{AK} (V), and Current I_{AK} (µA).
4. Now Keep the gate current (I_G) at a standard value of 10 mA i.e. $I_G = 10$ mA.
5. Again vary the anode to cathode supply voltage and note down the corresponding readings of Voltage V_{AK} (V), and Current I_{AK} (mA).
6. Plot the graph by taking V_{AK} (V) on x-axis and Current I_{AK} (mA) on y-axis.
7. Measure the Break-over voltage (V_{BO}) and Holding current (I_H) of SCR from the graph.

Tabulation:

S.No.	I_G=0mA		I_G = 10 mA	
	V_{AK} (V)	I_{AK} (µA)	V_{AK} (V)	I_{AK} (µA)

Model Graph:



Review Questions:

1. What is meant by Valley Point and Peak Point?
2. After triggering an SCR, the gate pulse is removed. What is the state (ON or OFF) of the device at this condition? Justify our answer
3. Why is Peak Reverse Voltage Important?
4. What is asymmetrical SCR?
5. What is the difference between SCR and TRIAC?

Result:PSPICE Tool

The V-I characteristics of SCR are drawn and the Break-over voltage (V_{BO}), Holding current (I_H) of SCR are found.

1. The Break-over voltage (V_{BO}) of SCR is ______________.
2. The Holding current (I_H) of SCR is __________________.

Ex No: 12

Half wave Rectifier and Full wave Rectifier using PSPICE

Aim:

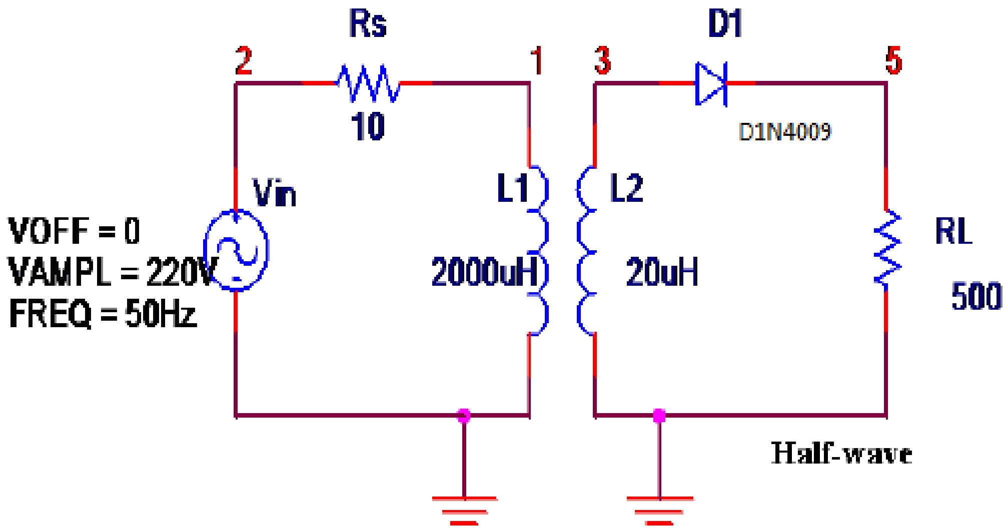
To Study the characteristics of a half and full wave Rectifiers using PSPICE windows.

Apparatus required:

PC loaded with PSPICE Tool

Circuit Diagram:

(i). Half wave rectifier



Program:

VIN 2 0 sin(0 220V 50HZ)

RL 5 0 500

RS 2 1 10

L1 1 0 2000uH

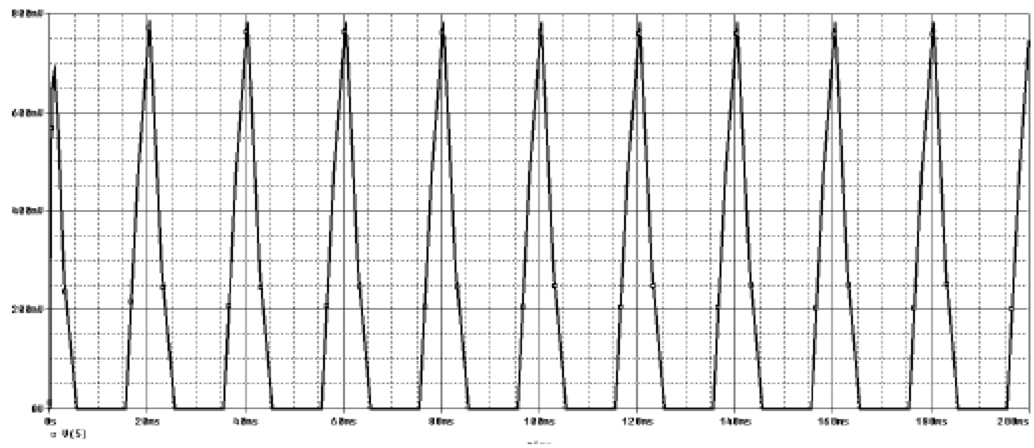
L2 3 0 20uH

K1 L1 L2 0.99999

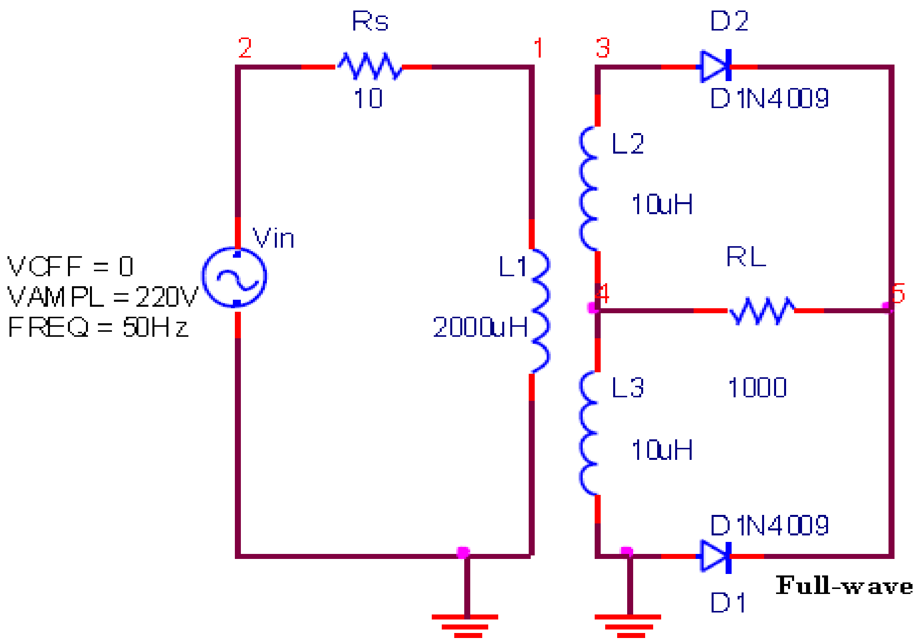
D1 3 5 D1N4009

```
.model D1N4009 D(Is=544.7E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333
+ Vj=.75 Fc=.5 Isr=30.77n Nr=2 Bv=25 Ibv=100u Tt=2.885n)
.tran 0.2m 200m
.plot tran v(3), v(5)
.probe
.end
```

Output:



(ii). Full Wave Rectifier

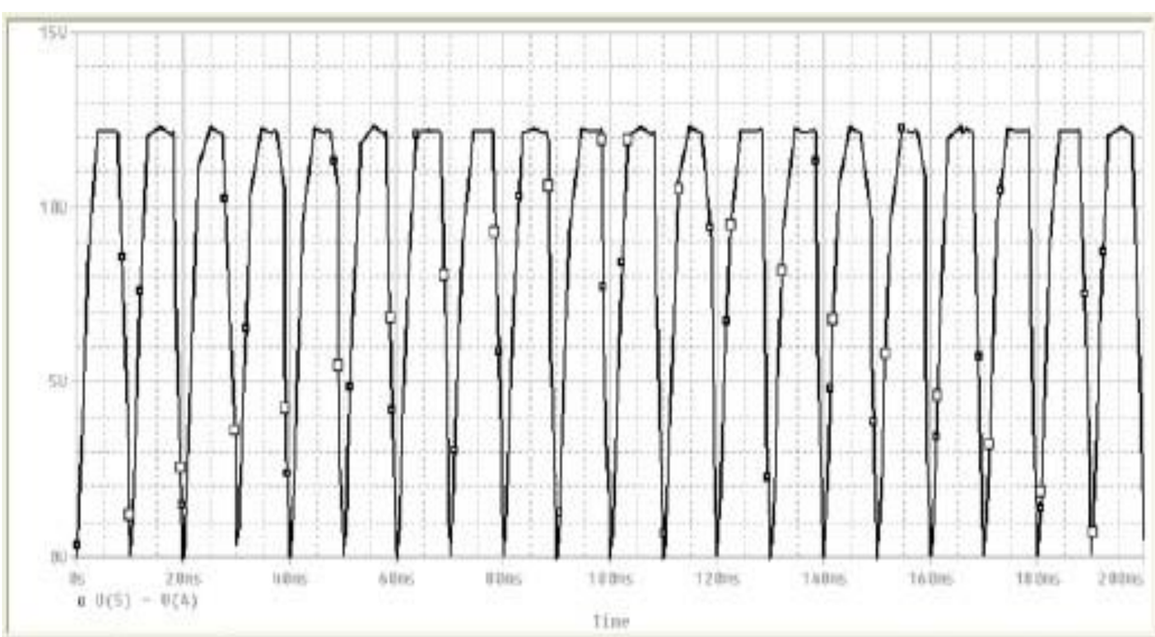


Full-wave Rectifier

Program:

```
Vin 2 0 sin(0 230V 50HZ)
RL 5 4 1000
RS 2 1 10
L1 1 0 2000
L2 3 4 10
L3 4 0 10
K1 L1 L2 L3 0.99
D1 0 5 D1N4009
D2 3 5 D1N4009
.model D1N4009
D(Is=544.7E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333
+ Vj=.75 Fc=.5 Isr=30.77n Nr=2 Bv=25 Ibv=100u Tt=2.885n)
.tran 0.2ms 200ms
.probe
.end
```

Output:



FULL WAVE RECTIFIER

Review Questions:

1. What is meant by AC and DC analysis?
2. What is meant by Transient Analysis?
3. What is use of Plot and Probe?
4. What are the uses of PSPICE?
5. List Advantages of PSPICE.

Result:

Thus the characteristics of half and full wave rectifier circuits are simulated using PSPICE.