SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)
SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

V SEMESTER

PEC102 VALIDATION AND TESTING TECHNOLOGY

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Prepared by

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UNIT I – TECHNOLOGY INTRODUCTION

Introduction to IC Technology – MOS, PMOS, NMOS, CMOS & BiCMOS Technologies. VLSI Fabrication, Oxidation, Lithography, Diffusion, Ion Implantation, Metallization, Integrated Resistors and Capacitors.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	What do you understand by Integrated Circuit?	CO1	BTL1	**Remember**
2.	Explain the advantages of Integrated Circuits over Discrete Circuits?	CO1	BTL1	**Remember**
3.	State Moore's Law?	CO1	BTL1	**Remember**
4.	Define Monolithic IC?	CO1	BTL1	**Remember**
5.	Differentiate between Monolithic and MOS integrated circuits?	CO1	BTL1	**Remember**
6.	List the classification of ICs based on fabrication techniques?	CO1	BTL1	**Remember**
7.	Describe Thin Film Technology?	CO1	BTL2	**Understand**
8.	Identify the situations where Thick Film Technology is used for IC fabrication?	CO1	BTL2	**Understand**
9.	Compare Enhancement and Depletion type MOSFETs?	CO1	BTL2	**Understand**
10.	Name the four different CMOS fabrication technologies?	CO1	BTL2	**Understand**
11.	What are the advantages of CMOS Technology?	CO1	BTL2	**Understand**
12.	Outline the disadvantages of CMOS Technology?	CO1	BTL1	**Remember**
13.	Define BiCMOS technology?	CO1	BTL1	**Remember**
14.	Explain the twin tub process?	CO1	BTL1	**Remember**
15.	Specify the applications where BiCMOS Technology is used?	CO1	BTL1	**Remember**
16.	Discuss the scenarios suitable for CMOS Technology?	CO1	BTL1	**Remember**
17.	Draw the flowchart of IC fabrication steps?	CO1	BTL1	**Remember**
18.	Describe the term oxidation in IC fabrication?	CO1	BTL2	**Understand**
19.	Mention the types of oxidation?	CO1	BTL2	**Understand**
20.	Brief about the diffusion process used in IC manufacturing?	CO1	BTL1	**Remember**
21.	Write about the concept of Ion implantation?	CO1	BTL2	**Understand**
22.	What is Chemical Vapour Deposition?	CO1	BTL2	**Understand**
23.	Describe the process of Metallization?	CO1	BTL1	**Remember**
24.	What is meant by Photolithography?	CO1	BTL2	**Understand**

PART – B

Q.No	Questions	CO	BT Level	Competence
1.	Give the classification of IC on basis of size, operation, fabrication and logic family? Describe about each type.	CO1	BTL4	**Analyze**
2.	Explain the construction and working of Enhancement NMOS Transistor?	CO1	BTL4	**Analyze**
3.	Describe the depletion mode NMOS transistor action with necessary diagrams?	CO1	BTL4	**Analyze**
4.	Compare CMOS Technology with Bipolar Technology.	CO1	BTL4	**Analyze**
5.	Explain the IC fabrication steps with a flowchart?	CO1	BTL4	**Analyze**
6.	Discuss the significance of oxidation in VLSI fabrication and how it contributes to the overall performance of the integrated circuits.	CO1	BTL3	**Apply**
7.	Describe the NMOS fabrication process with diagrams for each step?	CO1	BTL3	**Apply**
8.	Explain the CMOS fabrication process	CO1	BTL3	**Apply**

9.	Describe in detail step-by-step procedure of the p-well CMOS fabrication process and write the mask sequence	CO1	BTL3	**Apply**
10.	Describe the main steps in typical n-well CMOS process.	CO1	BTL3	**Apply**
11.	Explain the process of photolithography with neat diagram?	CO1	BTL3	**Apply**
12.	Describe Wafer Preparation and oxidation process?	CO1	BTL3	**Apply**
13.	Write short notes on Chemical vapor deposition?	CO1	BTL3	**Apply**
14.	Discuss about the BiCMOS fabrication process in detail?	CO1	BTL4	**Analyze**
15.	Draw the process flow diagram for NMOS fabrication. Explain each step involved in the process?	CO1	BTL4	**Analyze**
16.	Discuss the role of photolithography and ion implantation in NMOS fabrication.	CO1	BTL4	**Analyze**
17.	Examine the role of integrated resistors and capacitors in modern IC technology, considering their impact on circuit design and functionality.	CO1	BTL4	**Analyze**

UNIT II – MOS THEORY ANALYSIS I

Basic Electrical Properties of MOS Circuits: Ids-Vds Relationships, MOS Transistor Threshold Voltage Vth, gm, gds, Figure of Merit ωo, Short Channel and Narrow Channel Width Effects.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	List the conditions that determine different operating regions in the Ids–Vds characteristics.	CO2	BTL1	**Remember**
2.	Identify the mode of operation when Vds < (Vgs – Vth).	CO2	BTL1	**Remember**
3.	Label the axes of an Ids vs. Vds plot and identify the regions.	CO2	BTL1	**Remember**
4.	What is Saturation region?	CO2	BTL1	**Remember**
5.	What is Non Saturated reion?	CO2	BTL1	**Remember**
6.	Name the parameters that effect the magnitude of drain to source current Ids.	CO2	BTL1	**Remember**
7.	What is Threshold voltage?	CO2	BTL2	**Understand**
8.	State the mathematical expression for threshold voltage (Vth).	CO2	BTL2	**Understand**
9.	Mention the functional parameters of threshold equation?	CO2	BTL2	**Understand**
10.	How the threshold voltage can be varied?	CO2	BTL2	**Understand**
11.	What are the common methods used to adjust threshold voltage?	CO2	BTL2	**Understand**
12.	What is body effect?	CO2	BTL1	**Remember**
13.	Write the threshold voltage equation including the body effect.	CO2	BTL1	**Remember**
14.	Compare long channel and short channel behavior in MOSFETs.	CO2	BTL1	**Remember**
15.	Analyze the role of body bias in modifying threshold voltage in short-channel devices.	CO2	BTL1	**Remember**
16.	What is meant by figure of merit ω_0?	CO2	BTL1	**Remember**
17.	Summarize the role of output conductance (gds) in MOSFET modeling.	CO2	BTL1	**Remember**
18.	Define Output conductance	CO2	BTL2	**Understand**
19.	Describe the dependency of gds on channel length.	CO2	BTL2	**Understand**
20.	Write down the typical value of electron mobility at room temperature?	CO2	BTL1	**Remember**
21.	Define transconductance (gm) in MOS devices.	CO2	BTL2	**Understand**
22.	Mention the significance of gds in MOS device.	CO2	BTL2	**Understand**
23.	Outline how transconductance affects amplification in MOS circuits.	CO2	BTL1	**Remember**
24.	Illustrate how ω_0 relates to gm and gds.	CO2	BTL2	**Understand**

PART – B

1.	Illustrate the relationship between drain to source current and voltage for a MOS transistor.	CO2	BTL4	**Analyze**

2.	Apply MOS transistor equations to determine the expression for drain-to-source current in the non-saturation (linear) region. List the assumptions used in the derivation.	CO2	BTL3	**Apply**
3.	Derive the drain to source current in saturation region of a MOS transistor and draw the typical characteristics for pMOS and nMOS transistors.	CO2	BTL3	**Apply**
4.	Investigate the physical parameters influencing the threshold voltage of a MOS transistor, and derive the mathematical expression for it.	CO2	BTL4	**Analyze**
5.	Examine the effect of the body (substrate) bias on the threshold voltage, and derive the modified equation incorporating the body effect.	CO2	BTL4	**Analyze**
6.	Define and derive the transconductance of nMOS transistor	CO2	BTL3	**Apply**
7.	Derive the expression for output conductance gds of a MOS transistor?	CO2	BTL3	**Apply**
8.	Explain detail the MOS transistor Figure of merit ω_0?	CO2	BTL3	**Apply**
9.	Discuss the effects of Short channel and narrow channel widths of MOS Transistor	CO2	BTL3	**Apply**
10.	Explain the Ids – Vds relationship in MOS transistor	CO2	BTL3	**Apply**
11.	Apply MOS transistor theory to derive the expression for output conductance (gds)	CO2	BTL3	**Apply**
12.	Consider an nMOS having electron mobility of $\mu_n = 540$ cm^2/V – Sec. Calculate the process transconductance for the gate oxide thickness of 12nm and 8 nm. What did you infer on reducing gate oxide thickness?	CO2	BTL4	**Analyze**
13.	Calculate the native threshold voltage for a n-transistor at 300°K for a process with a Si substrate with $N_A = 1.80 \text{ X } 10^{16}$, a SiO_2 gate oxide with thickness 200◌A (Assume $\Phi_{ms} = -0.9V$, $Q_{fc} = 0$)	CO2	BTL3	**Apply**
14.	Determine the drain current expression for a MOS transistor in the saturation region, and analyze the differences in characteristics for pMOS and nMOS devices with supporting plots.	CO2	BTL4	**Analyze**
15.	Compute the drain-to-source current of a MOS transistor operating in the linear region, and explain the conditions under which this region is valid.	CO2	BTL4	**Analyze**
16.	Analyze the factors that influence the threshold voltage of a MOS transistor and derive the relevant equation using physical parameters.	CO2	BTL4	**Analyze**
17.	Evaluate how the body effect modifies the threshold voltage in a MOS transistor, and formulate the corresponding mathematical expression.	CO2	BTL4	**Analyze**

UNIT III – MOS THEORY ANALYSIS II

Pass Transistor, Transmission Gate, NMOS Inverter, Various Pull-ups, CMOS Inverter Analysis and Design, Bi-CMOS Inverters, Latch up in CMOS Circuits.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	Define pass transistor in digital logic.	CO3	BTL1	**Remember**
2.	How the pass transistor differs from regular CMOS switch?	CO3	BTL1	**Remember**
3.	State the function of a transmission gate	CO3	BTL1	**Remember**
4.	List two limitations of pass transistor.	CO3	BTL1	**Remember**
5.	Mention on advantage of using transmission gate over pass transistor?	CO3	BTL1	**Remember**
6.	Draw the configuration of NMOS inverter.	CO3	BTL1	**Remember**
7.	Identify the output of NMOS inverter, when the input is high	CO3	BTL2	**Understand**
8.	Describe the role of depletion-mode transistors as pull-ups in NMOS inverters.	CO3	BTL2	**Understand**

9.	Explain why resistive pull-ups are not preferred in VLSI design?	CO3	BTL2	**Understand**
10.	Classify the types of pull-up devices used in NMOS inverters.	CO3	BTL2	**Understand**
11.	Name any two advantages of CMOS over NMOS logic?	CO3	BTL2	**Understand**
12.	List the advantages of pass transistor.	CO3	BTL1	**Remember**
13.	What is the design objective of a CMOS inverter?	CO3	BTL1	**Remember**
14.	Draw the DC transfer Characteristics of CMOS Inverter?	CO3	BTL1	**Remember**
15.	Label the regions of operation in a CMOS inverter transfer characteristics?	CO3	BTL1	**Remember**
16.	Define Noise Margin in the context of CMOS inverters?	CO3	BTL1	**Remember**
17.	What is latch up condition in CMOS circuits?	CO3	BTL1	**Remember**
18.	Draw the improved version of BiCMOS inverter using MOS transistors for base current discharge?	CO3	BTL2	**Understand**
19.	State the cause of latch-up in CMOS circuits.	CO3	BTL2	**Understand**
20.	List two methods to prevent latch-up.	CO3	BTL1	**Remember**
21.	Mention the effect of latch-up on CMOS circuits.	CO3	BTL2	**Understand**
22.	What are the remedies for latch up problem?	CO3	BTL2	**Understand**
23.	Why the BiCMOS are less likely to suffer from latch up problem?	CO3	BTL1	**Remember**
24.	State one application of BiCMOS inverters.	CO3	BTL2	**Understand**
	PART – B			
1.	Explain the working principle and application of pass transistors and transmission gates.	CO3	BTL4	**Analyze**
2.	With the help of the circuit diagram, describe the working of NMOS inverter and derive its transfer characteristics?	CO3	BTL3	**Apply**
3.	Determine the pull up to pull down ratio for an nMOS inverter driven by another nMOS inverter	CO3	BTL3	**Apply**
4.	Derive the Zpu/Zpd for nMOS inverter driven through one or more pass transistors?	CO3	BTL4	**Analyze**
5.	Examine the differences in pull-up network implementation using (a) load resistor RL, (b) nMOS depletion-mode transistor, (c) nMOS enhancement-mode transistor, and (d) complementary transistors.	CO3	BTL4	**Analyze**
6.	Apply your understanding of NMOS inverters to construct its circuit diagram and examine the transfer characteristics derived from its operation.	CO3	BTL3	**Apply**
7.	Discuss the operation of NMOS inverter and to determine the gain form its transfer characteristics?	CO3	BTL3	**Apply**
8.	Compare and contrast the different types of pull up networks used in MOS inverters?	CO3	BTL3	**Apply**
9.	Explain the DC transfer characteristics of CMOS inverter?	CO3	BTL3	**Apply**
10.	Describe the BiCMOS inverter and the discharge current problems associated with it? Discuss the circuits to overcome those problems?	CO3	BTL3	**Apply**
11.	Draw and explain the DC transfer characteristics of a CMOS inverter with necessary conditions for different regions of operation?	CO3	BTL3	**Apply**
12.	Apply BiCMOS technology principles to design a BiCMOS inverter, and explain its advantages?	CO3	BTL3	**Apply**
13.	Investigate the causes of latch-up in CMOS circuits and propose techniques to prevent it?	CO3	BTL4	**Analyze**
14.	Discuss the transfer characteristics of CMOS inverter?	CO3	BTL4	**Analyze**
15.	Explain the circuit details and working of BiCMOS inverter?	CO3	BTL4	**Analyze**
16.	Discuss the latch up in CMOS circuits?	CO3	BTL4	**Analyze**
17.	Analyze the CMOS inverter transfer characteristics and identify the regions of operation?	CO3	BTL4	**Analyze**

UNIT IV – CMOS CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION

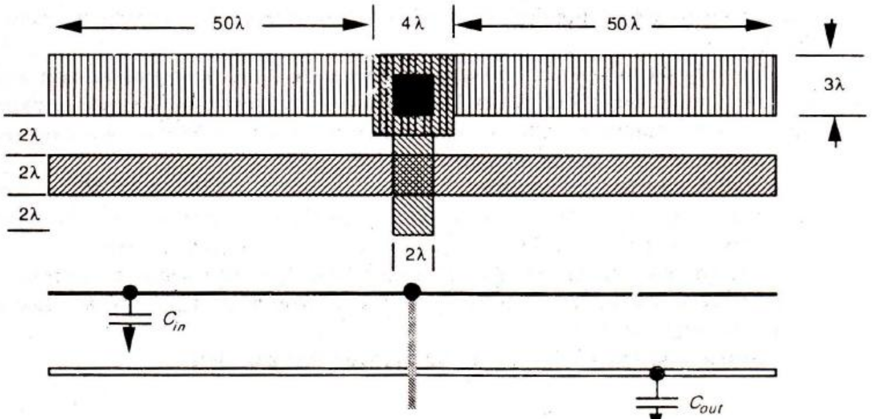
Sheet Resistance, conductivity and its Concept to MOS, Area Capacitance Units, Calculations -Delays, Driving Large Capacitive Loads, Delay Estimation, Logical Effort and Transistor Sizing, Power Dissipation, Reliability.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	Define sheet resistance Rs.	CO4	BTL1	**Remember**
2.	Explain the term silicides.	CO4	BTL1	**Remember**
3.	State the expression for capacitance when thickness is known.	CO4	BTL1	**Remember**
4.	Calculate the standard capacitance of a 2 μm MOS circuit, given gate capacitance as 8 X 10^{-4} pF/μm^2	CO4	BTL1	**Remember**
5.	Write the formula used for computing delay unit τ.	CO4	BTL1	**Remember**
6.	Draw the circuit model required to derive the delay unit τ.	CO4	BTL1	**Remember**
7.	How is delay estimated in CMOS circuits?	CO4	BTL2	**Understand**
8.	Describe the function of a super buffer.	CO4	BTL2	**Understand**
9.	List two possible layer choices used in MOS circuit fabrication.	CO4	BTL2	**Understand**
10.	Mention the purpose of the RC delay model.	CO4	BTL2	**Understand**
11.	Define the Elmore delay model.	CO4	BTL2	**Understand**
12.	Illustrate the meaning of linear delay in timing analysis.	CO4	BTL1	**Remember**
13.	Clarify the concept of effort delay in digital design.	CO4	BTL1	**Remember**
14.	Interpret the term electrical effort.	CO4	BTL1	**Remember**
15.	What is logical effort in CMOS logic design?	CO4	BTL1	**Remember**
16.	Name the techniques to reduce delay in a chain of inverters.	CO4	BTL1	**Remember**
17.	Identify the common sources contributing to power dissipation.	CO4	BTL1	**Remember**
18.	How does static power dissipation occur in CMOS circuits?	CO4	BTL2	**Understand**
19.	Discuss the cause and effect of dynamic power dissipation.	CO4	BTL2	**Understand**
20.	Suggest two methods to reduce dynamic power consumption.	CO4	BTL1	**Remember**
21.	Propose approaches to reduce static power loss.	CO4	BTL2	**Understand**
22.	Define the term reliability in VLSI systems.	CO4	BTL2	**Understand**
23.	Draw the bathtub curve and explain its significance.	CO4	BTL1	**Remember**
24.	List the key reasons for reliability failures in integrated circuits.	CO4	BTL2	**Understand**

PART – B

Q.No	Questions	CO	BT Level	Competence
1.	Derive the expression for sheet resistance and explain how it can be used to MOS transistors and inverters?	CO4	BTL4	**Analyze**
2.	A particular layer of MOS circuit has a resistivity p = 1 ohm cm. A section of this layer is 55 μm long and 5 μm wide and has a thickness of 1 μm. Calculate the resistance from one end of this section to the other (along the length). Use the concept of sheet resistance Rs. What is the value of Rs?	CO4	BTL3	**Apply**
3.	Discuss in detail on area capacitance of MOS devices?	CO4	BTL3	**Apply**
4.	Estimate the delay of formal CMOS inverter?	CO4	BTL4	**Analyze**
5.	Describe the methods used to drive large capacitive loads in IC design?	CO4	BTL4	**Analyze**
6.	Explain about the propagation delay in cascaded pass transistors chain and in long polysilicon wires?	CO4	BTL3	**Apply**
7.	Determine the input capacitance Cin and output capacitance Cout for the given structure.	CO4	BTL3	**Apply**

				
8.	Discuss in detail the concept of logical effort and its importance in CMOS circuit design.	CO4	BTL3	**Apply**
9.	Describe the Elmore Delay model to estimate the propagation delay?	CO4	BTL3	**Apply**
10.	Sketch a two input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delays in terms of R and C of the NAND gate driving h identical NAND gates using Elmore delay model.	CO4	BTL3	**Apply**
11.	Sketch a two input NOR gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter. Compute the rising and falling propagation delays of the NOR gate driving h identical NOR.	CO4	BTL3	**Apply**
12.	Describe the linear delay model with necessary expressions?	CO4	BTL3	**Apply**
13.	Determine the delay in multistage logic networks using logic effort?	CO4	BTL4	**Analyze**
14.	Calculate the logical, electrical, stage effort and capacitance transformation for the given figure	CO4	BTL4	**Analyze**
15.	Consider the path from A to B involving three two input NAND gate as shown in Figure. The input capacitance of the first gate is C, and the load capacitance is 8C. What is the least delay of this path?	CO4	BTL4	**Analyze**
16.	Explain the static and dynamic power dissipation in CMOS circuits?	CO4	BTL4	**Analyze**
17.	Explain the different reliability problems related to the design of CMOS circuits?	CO4	BTL4	**Analyze**

UNIT V – BASICS OF SILICON VALIDATION

Need for Testing, Testing at Various Levels, Objectives of Testing - VLSI Test process and Test Equipment - Types of Testing: Functionality Tests, Silicon Debug, Manufacturing Tests, Defect during manufacturing - Fault Modelling, Observability and Controllability, Fault Coverage, Fault Sampling - ATE, Test economics.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	Define the need for testing in VLSI circuits.	CO5	BTL1	**Remember**
2.	What are the different levels at which a chip is tested.	CO5	BTL1	**Remember**
3.	State the primary objectives of testing in CMOS design.	CO5	BTL1	**Remember**
4.	List the steps involved in testing during CMOS chip design.	CO5	BTL1	**Remember**
5.	Describe the role of a tester in IC validation.	CO5	BTL1	**Remember**
6.	Explain the purpose of a test fixture.	CO5	BTL1	**Remember**
7.	Summarize the concept of shmooing in test evaluation.	CO5	BTL2	**Understand**
8.	Mention the various types of testing methods used for ICs.	CO5	BTL2	**Understand**
9.	What is meant by a functionality test?	CO5	BTL2	**Understand**
10.	Define manufacturing tests.	CO5	BTL2	**Understand**
11.	Define the term 'fault model' used in testing.	CO5	BTL2	**Understand**
12.	What is a defect in the context of semiconductor testing?	CO5	BTL1	**Remember**
13.	Point out the meaning of an error in testing.	CO5	BTL1	**Remember**
14.	Describe the nature of a fault in chip design.	CO5	BTL1	**Remember**
15.	Explain about stuck-at fault.	CO5	BTL1	**Remember**
16.	What do you mean by controllability?	CO5	BTL1	**Remember**
17.	State about observability in testing?	CO5	BTL1	**Remember**
18.	Define fault coverage.	CO5	BTL2	**Understand**
19.	Summarize the use of fault sampling in test generation.	CO5	BTL2	**Understand**
20.	Describe a branch fault?	CO5	BTL1	**Remember**
21.	List all possible test vectors for a 2-input NOR gate.	CO5	BTL2	**Understand**
22.	State the full form and purpose of ATE in IC testing.	CO5	BTL2	**Understand**
23.	Define the term 'yield' in VLSI manufacturing.	CO5	BTL1	**Remember**
24.	Define the need for testing in VLSI circuits.	CO5	BTL2	**Understand**

PART – B

Q.No	Questions	CO	BT Level	Competence
1.	As a Semiconductor manufacturing manager, you’ve been tasked with improving the efficiency and reliability of the silicon validation and testing process for a cutting edge VLSI chip. Describe your over all strategy, considering the need for testing, objectives, equipment, and economic factors.	CO5	BTL4	**Analyze**
2.	With a neat diagram, describe an Automatic Test Equipment (ATE)?	CO5	BTL3	**Apply**
3.	Explain the manufacturing test principles in IC testing?	CO5	BTL3	**Apply**
4.	Describe the different types of testing in VLSI, such as functionality test, silicon debug principles and manufacturing test?	CO5	BTL3	**Apply**
5.	Explain the various levels of testing in ensuring the reliability and functionality of VLSI circuits.	CO5	BTL3	**Apply**
6.	(i) Discuss on Defects, Error and Faults (ii) Consider a digital system consisting of two inputs a and b, one output c, and one two-input AND gate. The system is assembled by connecting a wire between the terminal a and the first input of the AND gate. The output of the gate is connected to c. But the connection between b and the gate	CO5	BTL4	**Analyze**

	is incorrectly made – b is left unconnected and the second input of the gate is grounded. The functional output of this system, as implemented, is instead of the correct output. For this system, identify defect, fault and error.			
7.	Describe any five fault model with an example, in the context of IC testing?	CO5	BTL3	**Apply**
8.	Explain single stuck at fault with a relevant example?	CO5	BTL3	**Apply**
9.	Draw a 2 input XOR gate using NAND gates and identify the possible single stuck at faults?	CO5	BTL4	**Analyze**
10.	Discuss on fault sampling technique and narrate about its advantages?	CO5	BTL3	**Apply**
11.	Describe the types of fault simulation with necessary illustrations?	CO5	BTL3	**Apply**
12.	Summarize about the fault equivalence and illustrate with example?	CO5	BTL3	**Apply**
13.	Realize the function G = A.(B+C) + B.C with logic gates and compute the combinational SCOAP testability measures (both controllability and observability).	CO5	BTL4	**Analyze**
14.	Describe the combinational SCOAP measures to test for controllability and observability	CO5	BTL4	**Analyze**
15.	What is controllability and observability? Explain with an example?	CO5	BTL4	**Analyze**
16.	Differentiate Stuck at 0 and stuck at 1 faults with example.	CO5	BTL4	**Analyze**
17.	Analyze the factors that influence the economics of IC testing and explain how they impact overall test efficiency	CO5	BTL4	**Analyze**