SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

Department of Computer Science and Engineering

(Common to IT, AI & DS, CYS)

QUESTION BANK

Academic Year 2025 – 2026(ODD SEMESTER)

III SEMESTER

AD3363-DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

Regulation – 2023

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DEPARTMENT

OF

COMPUTER SCIENCE AND ENGINEERING

(Common to AI&DS, CYS, IT)

QUESTION BANK

SUBJECT: DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

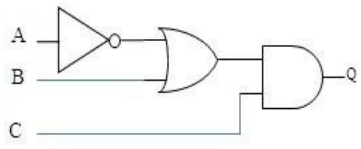
SEM / YEAR: III SEMESTER/ SECOND YEAR

UNIT-I: COMBINATIONAL LOGIC			
Combinational Circuits – Karnaugh Map - Analysis and Design Procedures – Binary Adder – Subtractor – Decimal Adder - Magnitude Comparator – Decoder – Encoder – Multiplexers - Demultiplexers.			
PART-A			
Q.no	**Question**	**BTL**	**Competence**
1	What are some common examples of combinational circuits used in digital systems?	BTL2	Understanding
2	How does a multiplexer function as a combinational circuit?	BTL1	Remembering
3	Explain the main difference between combinational and sequential circuits.	BTL1	Remembering
4	What is the primary purpose of a full adder in digital circuits?	BTL1	Remembering
5	How can multiple full adders be combined to add two multi-bit binary numbers?	BTL1	Remembering
6	How does a half subtractor differ from a full subtractor?	BTL1	Remembering
7	What is the primary challenge in designing a BCD (Binary-Coded Decimal) adder compared to a binary adder?	BTL1	Remembering
8	Explain how a BCD adder handles sums greater than 9.	BTL1	Remembering
9	What is a Karnaugh Map and what is its primary use in digital logic design?	BTL1	Remembering
10	How does grouping work in a Karnaugh Map?	BTL1	Remembering
11	What are the rules for creating groups in a Karnaugh Map?	BTL1	Remembering
12	What is a magnitude comparator and what is its primary function?	BTL2	Understanding
13	How does a 4-bit magnitude comparator function?	BTL1	Remembering
14	What is the main purpose of a decoder in digital circuits?	BTL1	Remembering
15	What is the function of an encoder in digital electronics?	BTL1	Remembering

16	Describe the primary function of a multiplexer.	BTL1	Remembering
17	What is the primary purpose of a demultiplexer?	BTL1	Remembering
18	What is the role of selection lines in a 4-to-1 multiplexer?	BTL1	Remembering

19	How does a 1-to-4 demultiplexer function?	BTL1	Remembering
20	Simplify the boolean function F(A,B,C)F(A, B, C)F(A,B,C) given by the minterms: F(A,B,C)=Σ(0,1,2,5,6,7)	BTL2	Understanding
21	What are the primary components and outputs of a half adder?	BTL1	Remembering
22	How does a full adder differ from a half adder in terms of inputs and functionality?	BTL1	Remembering
23	How can multiple full adders be used to construct a multi-bit binary adder?	BTL1	Remembering
24	Describe the basic function of a 3-to-8 line decoder.	BTL1	Remembering

PART-B

Q.no	Question	Mark	BTL	Competence
1	Design and analyze a 4-bit Binary Adder/Subtractor Circuit	16	BTL4	Analyzing
2	Design and analyze an 8-bit Binary Adder with example	16	BTL4	Analyzing
3	Design and analyze an 8-bit Binary subtractor with example	16	BTL4	Analyzing
4	Given the following Boolean function F(A,B,C,D)F(A, B, C, D)F(A,B,C,D), simplify it using a Karnaugh Map and derive the minimal Sum of Products (SOP) form.The Boolean function is defined as:F(A,B,C,D)=∑m(0,1,2,5,7,8,9,12,14)	16	BTL4	Analyzing
5	Simplify the following switching function using karnaugh map method and realize expression using gates F (A, B, C, D) = ∑ (0,3,5,7,8,9,10,12,15)	16	BTL3	Applying
6	Examine how to minimize the function: F (A, B, C, D) =∑m (0,4,6,8,9,10,12) +∑d (2,13) and implement it using only NOR gates.	16	BTL3	Applying
7(a)	Simplify the Boolean function in Sum of Products (SOP) and Product of Sum (POS) F(w,x,y,z)=∑m(0,1,2,5,8,9,10).	08	BTL4	Analyzing
7(b)	Design the Boolean function in Karnaugh map and simplify it F(w,x,y,z)=∑m(0,1,2,4,5,6,8,9,12,13,14).	08	BTL6	Creating
8	Simplify the following Boolean expression in (a) Sum of Product (b) Product of Sum using Karnaugh map AC' + B'D + A'CD + ABCD.	08+08	BTL4	Analyzing
9(a)	Express the following function in sum of min-terms and product of max-terms: F(x,y,z)=x+yz.	08	BTL2	Understanding
9(b)	Convert the following logic system in to NAND gates only. 	08	BTL3	Applying

10(a)	What is De-Multiplexer explain in detail with example	16	BTL2	Understanding
11	What is Multiplexer explain in detail with example	16	BTL2	Understanding
12	Design a 4-bit binary adder/subtractor circuit. Provide the circuit diagram and explain the logic behind the design. Show how the circuit handles both addition and subtraction operations. Include the truth table for the adder/subtractor in both modes, and describe how the carry and borrow operations are managed.	16	BTL6	Creating
13	Given the Boolean function F (A, B, C, D) =Σ (1,3,5,7,9,11,13,15) simplify the function using a Karnaugh Map. Provide the K-map, identify groups, and derive the simplified Boolean expression. Explain the steps taken to group minterms and simplify the expression.	16	BTL5	Evaluating
14	Design an 8-to-3-line encoder. Provide the circuit diagram and derive the Boolean expressions for the output lines.	16	BTL6	Creating
15	Design a 1-to-4-line demultiplexer. Provide the circuit diagram and derive the Boolean expressions for each output.	16	BTL6	Creating
16	Analyze a 4-bit magnitude comparator. Describe the functionality and provide the circuit diagram. Provide the truth table and discuss the use cases of magnitude comparators in digital systems.	16	BTL4	Analyzing
17	Implement the following function using 8 to 1 multiplexer f(a, b,c,d)= ∑m(0,1,3,5,9,12,14,15)	16	BTL5	Evaluating

UNIT II - SYNCHRONOUS SEQUENTIAL LOGIC

Introduction to Sequential Circuits – Flip-Flops – operation and excitation tables, Triggering of FF, Analysis and design of clocked sequential circuits – Design – Moore/Mealy models, state minimization, state assignment, circuit implementation - Registers – Counters.

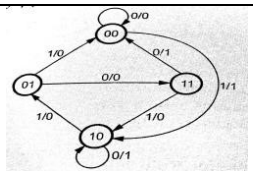
PART-A

Q.no	Question	BTL	Competence
1	Difference between Combinational & Sequential Circuits.	BTL1	Remembering
2	What are the classifications of sequential circuits?	BTL1	Remembering
3	Define Latch.	BTL1	Remembering
4	Define a flip flop.	BTL1	Remembering
5	What are the different types of flip-flops?	BTL1	Remembering
6	Define registers.	BTL1	Remembering
7	State few applications of Flip-Flop.	BTL1	Remembering
8	What is the operation of D flip-flop?	BTL1	Remembering
9	What is the operation of JK flip-flop?	BTL1	Remembering
10	What is the operation of T flip-flop?	BTL1	Remembering
11	Define race around condition	BTL1	Remembering

12	What is triggering? What is the need for trigger in flip-flop?	BTL2	Understanding
13	What is meant by level and edge-triggering?	BTL1	Remembering
14	Draw the logic diagram and write the function table of D Latch.	BTL1	Remembering
15	How do you eliminate race around condition in JK flip flop?	BTL1	Remembering
16	Define rise time	BTL1	Remembering
17	Define fall time.	BTL1	Remembering
18	Define skew and clock skew.	BTL1	Remembering
19	State the difference between latches and flip flops.	BTL2	Understanding
20	What is mealy and Moore circuit? Or what are the models used to represent clocked sequential circuits?	BTL1	Remembering
21	What is counter?	BTL2	Understanding
22	List the types of counters.	BTL1	Remembering
23	State the Steps or Design procedure for Synchronous Counter.	BTL2	Understanding
24	What is modulo-N counter?	BTL1	Remembering

PART-B

Q.no	Question	Mark	BTL	Competence
1	Explain the operation of flipflops.	16	BTL 5	Evaluating
2	Write short notes on Mealy and Moore models in sequential circuits	16	BTL2	Understanding
3	Explain the operation of a 4-bit binary ripple counter.	16	BTL3	Applying
4	Explain about Modulo 16 /4-bit Ripple Down counter.	16	BTL 5	Evaluating
5	Explain about Asynchronous Up/Down counter.	16	BTL 5	Evaluating
6	Explain about 4-bit Synchronous up-counter.	16	BTL 5	Evaluating
7	Explain about 4-Bit Synchronous down counter.	16	BTL 5	Evaluating
8	Explain about Modulo 8 Synchronous Up/Down Counter.	16	BTL 5	Evaluating
9	Design a 3-bit binary counter using T-flip flops.	16	BTL 5	Evaluating
10	Design of a Synchronous Modulus-Six Counter Using SR Flip-Flop	16	BTL 5	Evaluating
11	What are registers? Construct a 4-bit register using D-flip flops and explain the operations on the register.	16	BTL 5	Evaluating
12	Explain about universal shift register	16	BTL3	Applying
13	Explain about Johnson and Ring counter	16	BTL3	Applying
14	Design the sequential circuit specified by the following state diagram using T flip flops	16	BTL 5	Evaluating

				
15	Implement T flip-flop using D flip-flop and JK using D flip flop.	16	BTL3	Applying
16(a)	Explain about synchronous and asynchronous sequential Circuit.	08	BTL3	Applying
16(b)	Explain the working procedure of 3 bit parallel- in serial-out shift register construct the state table.	08	BTL1	Remembering
17	Explain the different types of shift registers with neat diagram.	16	BTL2	Understanding

UNIT - III - COMPUTER FUNDAMENTALS

Functional Units of a Digital Computer: Von Neumann Architecture – Operation and Operands of Computer Hardware Instruction – Instruction Set Architecture (ISA): Memory Location, Address and Operation – Instruction and Instruction Sequencing – Addressing Modes, Encoding of Machine Instruction – Interaction between Assembly and High-Level Language.

PART – A

Q. No.	Questions	BT Level	Competence
1	What are the five components of computer system?	BTL1	Remembering
2	What is cache memory?	BTL1	Remembering
3	What is the function of ALU?	BTL1	Remembering
4	What is the function of control unit?	BTL1	Remembering
5	What are basic operations of a computer memory?	BTL1	Remembering
6	List out the operations of the computer.	BTL1	Remembering
7	What is instruction set architecture	BTL2	Understanding
8	State Amdahl's law.	BTL2	Understanding
9	Define Stored Programmed Concept.	BTL2	Understanding
10	What are the registers generally contained in the processor?	BTL2	Understanding
11	**Describe** about the various logical operators.	BTL1	Understanding
12	What are called Instruction?	BTL1	Understanding
13	**Discuss** the functions of control unit?	BTL2	Understanding
14	Define clock rate. What is meant by clock cycle?	BTL2	Understanding
15	Define Register addressing mode with an example.	BTL2	Understanding
16	What is relative addressing mode with an example?	BTL2	Understanding
17	What is indirect addressing mode?	BTL2	Understanding
18	What is indexed addressing mode?	BTL2	Understanding
19	What is register?	BTL2	Understanding
20	List the phases, which are included in each instruction cycle?	BTL2	Understanding

21	What are the two major steps in processing an instruction? (Or) Write the two steps that are common to implement any type of instruction.	BTL2	Understanding
22	What are the speedup techniques available to increase the performance of a computer?	BTL2	Understanding
23	Distinguish between auto increment and auto decrement addressing mode	BTL2	Understanding
24	What are the limitations of assembly language?	BTL2	Understanding

PART – B

Q.no	Questions	Mark	BTL	Competence
1	Explain in detail about the components of a computer system.	16	BTL5	Evaluating
2	Explain about operations operands of computer hardware instruction.	16	BTL5	Evaluating
3	Discuss about ISA.	16	BTL6	Creating
4	Discuss about instructions and instruction sequencing	16	BTL6	Creating
5	What is the need for addressing in a computer system? Analyze the different addressing modes with suitable examples.(Or) Explain direct, immediate, relative and indexed addressing modes with examples.(Or) Identify the addressing mode involved in the instruction XOR r1 r2+ 100 r1 and determine the resultant stored in register R1 if all of its bit were 1'st initially .	16	BTL3	Applying
6.	Consider the computer with three instruction classes and CPI measurements as given below and instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 4 GHZ. Which code sequence will execute faster according to execution time?	16	BTL6	Creating
7	Explain about encoding of machine instruction.	16	BTL5	Evaluating
8	Explain the concept of interaction between assembly and high-level language	16	BTL3	Applying
9	With a neat diagram, describe about Von Newmann Architecture	16	BTL3	Applying
10	What is an addressing mode? Outline the types of Addressing mode with an example.	16	BTL3	Applying
11	Analyze about the functional unit of Digital Computer? Discuss about instruction cycle.	16	BTL4	Analyze

12	Describe instruction sequencing and branching with example	16	BTL4	Analyze
13	Explain any four addressing modes with example.	16	BTL5	Evaluating
14	Give the comparison between compiler and interpreter.	16	BTL4	Analyze
15	Give the comparison between machine level, and assembly level and high-level languages.	16	BTL4	Analyze
16	How to encode assembly instructions into 32-bit words? Analyze with examples.	16	BTL4	Analyze
17	Explain the following: i) Byte addressability, ii) Big-endian assignment, iii) Little-endian assignment.	16	BTL5	Evaluating

UNIT - IV: PROCESSOR

I/O Instruction Execution – Building a Data Path – Designing a Control Unit – Hardwired Control, Microprogrammed Control – Pipelining – Data Hazard – Control Hazards.

PART – A

Q. No	Questions	BT Level	Competence
1	What is the primary function of a processor in a computer system?	BTL 2	Understanding
2	Define instruction execution in the context of a processor.	BTL 1	Remembering
3	What is the significance of instruction fetch in instruction execution?	BTL 2	Understanding
4	What is a data path in a processor?	BTL 2	Understanding
5	What is the purpose of an ALU in a data path?	BTL 2	Understanding
6	Explain the role of a control unit in a processor.	BTL 2	Understanding
7	Explain the term 'instruction decode' in the execution cycle.	BTL 2	Understanding
8	What is a branch prediction?	BTL 2	Understanding
9	What is hardwired control?	BTL 2	Understanding
10	Define microprogrammed control.	BTL 1	Remembering
11	Differentiate between hardwired control and microprogrammed control.	BTL 1	Analyzing
12	What is pipelining in a processor?	BTL 1	Understanding
13	Define the term 'pipeline stage.'	BTL 1	Understanding
14	What is a pipeline stall?	BTL 2	Understanding

15	What is meant by instruction throughput in pipelining?	BTL 1	Understanding
16	Define the term 'control signal' in a processor.	BTL 1	Remembering
17	What is a register file in a processor?	BTL 2	Understanding
18	Explain the term 'pipeline hazard.'	BTL 2	Understanding
19	Explain the concept of a data hazard.	BTL 2	Understanding
20	What is a control hazard?	BTL 1	Remembering
21	Define pipelining in computer architecture.	BTL 1	Remembering
22	List the types of data hazards in pipelining.	BTL 1	Remembering
23	State the function of a control unit in a CPU.	BTL 1	Remembering
24	Define microprogrammed control.	BTL 1	Remembering

PART – B

Q. No	Questions	Marks	BT Level	Competence
1	Apply the concepts of data path design to a specific CPU architecture of your choice. Explain how the various components such as the ALU, registers, and control unit are interconnected and managed within this architecture.	16	BTL3	Applying
2	Discuss how pipeline stages can lead to data hazards and the techniques used to mitigate these hazards.	16	BTL3	Applying
3	Generalize the principles of hardwired and microprogrammed control units.	16	BTL3	Applying
4	Estimate the performance impact of control hazards in a pipelined architecture. Discuss the various techniques used to minimize these hazards and how they affect overall CPU performance.	16	BTL3	Applying
5	Demonstrate the process of designing a microprogrammed control unit for a simple instruction set.	16	BTL3	Applying
6	Analyse the impact of pipelining on processor performance.	16	BTL 4	Analyzing
7	Compare hardwired control and microprogrammed control in terms of design complexity, flexibility, and performance.	16	BTL 4	Analyzing
8	Examine the causes and solutions for data hazards in pipelined processors.	16	BTL 4	Analyzing
9	Distinguish between control hazards and data hazards, providing examples of each.	16	BTL 4	Analyzing
10	Classify the different types of data paths used in computer architecture and discuss their respective advantages and disadvantages.	16	BTL 4	Analyzing
11	Construct a detailed data path for a simple RISC processor. Include all necessary components such as registers, ALU, memory units, and control signals.	16	BTL5	Evaluating

12	Develop a comprehensive microprogrammed control unit for a basic CPU. Explain the control signals and microinstructions required for executing various instructions.	16	BTL5	Evaluating
13	Design a hardwired control unit for a simple instruction set. Describe the state diagram and the logic equations needed to generate the control signals.	16	BTL5	Evaluating
14	Modify a basic pipelined processor to handle data hazards. Discuss the techniques such as forwarding, stalling, and hazard detection units used to resolve these hazards.	16	BTL5	Evaluating
15	Compare and contrast different techniques such as branch prediction, delayed branching, and branch target buffers.	16	BTL5	Evaluating
16	Choose a Data Path Design for a Given Processor Architecture and Justify Your Choice.	16	BTL6	Creating
17	Decide on the Control Unit Design for a Processor and Explain Your Decision.	16	BTL6	Creating

UNIT – V: MEMORY AND I/O

Memory Concepts and Hierarchy – Memory Management – Cache Memories: Mapping and Replacement Techniques – Virtual Memory – DMA – I/O – Accessing I/O: Parallel and Serial Interface – Interrupt I/O – Interconnection Standards: USB, SATA

PART – A

Q.No.	Questions	BT Level	Competence
1	What is memory hierarchy?	BTL 2	Understanding
2	Define memory management.	BTL 1	Remembering
3	What is cache memory?	BTL 2	Understanding
4	Explain direct mapping in cache memory.	BTL 2	Understanding
5	What is a cache replacement policy?	BTL 2	Understanding
6	Define virtual memory.	BTL 1	Remembering
7	What does DMA stand for?	BTL 2	Understanding
8	What is the purpose of I/O in a computer system?	BTL 2	Understanding
9	Differentiate between parallel and serial interfaces.	BTL 1	Remembering
10	What is an interrupt in the context of I/O?	BTL 2	Understanding
11	What does USB stand for?	BTL 2	Understanding
12	What is the full form of SATA?	BTL 2	Understanding
13	What is meant by memory access time?	BTL 2	Understanding
14	Define page in memory management.	BTL 1	Remembering
15	What is cache hit and miss?	BTL 2	Understanding

16	Explain the concept of a page table.	BTL 2	Understanding
17	Explain the structure and functioning of an arithmetic logic unit (ALU) within a data path.	BTL 2	Understanding
18	Discuss the design and working of a control unit in a processor.	BTL 1	Remembering
19	Discuss the challenges and solutions in designing a control unit for a complex instruction set.	BTL 2	Understanding
20	Explain the concept of plug and play in USB.	BTL 2	Understanding
21	Define cache memory and briefly explain its role in computer systems.	BTL 1	Remembering
22	List two benefits of using virtual memory in operating systems.	BTL 1	Remembering
23	State two differences between parallel and serial interfaces in terms of data transmission.	BTL 1	Remembering
24	Define USB (Universal Serial Bus) and list two advantages it offers over other interconnection standards.	BTL 1	Remembering

PART – B

Q.No	Questions	Marks	BT Level	Competence
1	How does direct mapping in cache memory improve data retrieval speed? Provide a real-world example.	16	BTL3	Applying
2	Explain how virtual memory management supports multitasking in operating systems. Give one practical example.	16	BTL3	Applying
3	Compare DMA and interrupt-driven I/O in terms of their impact on CPU utilization and system performance.	16	BTL3	Applying
4	Estimate the storage capacity difference between USB 2.0 and USB 3.0 for transferring a 2 GB file.	16	BTL3	Applying
5	Describe the role of SATA in connecting storage devices to a computer.	16	BTL3	Applying
6	Analyse the role of cache memories in computer systems, comparing and contrasting different mapping and replacement techniques.	16	BTL 4	Analyzing
7	Compare virtual memory management with direct memory access (DMA), examining their respective roles and functionalities in computer systems.	16	BTL 4	Analyzing
8	Examine the characteristics and functionalities of USB and SATA interconnection standards, highlighting their respective strengths and applications in modern computing.	16	BTL 4	Analyzing
9	Distinguish between parallel and serial interfaces in I/O operations, highlighting their architectures, advantages, and limitations.	16	BTL 4	Analyzing
10	Classify interrupt-driven I/O mechanisms, examining their role in handling external events and enhancing system responsiveness.	16	BTL 4	Analyzing
11	Construct a brief explanation of cache memory and its role in computer systems.	16	BTL5	Evaluating
12	Develop a comparison between direct memory access (DMA) and interrupt-driven I/O.	16	BTL5	Evaluating
13	Design a virtual memory system outline, including key components like paging and swapping.	16	BTL5	Evaluating
14	Modify a cache memory configuration for better performance,	16	BTL5	Evaluating