SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF

ELECTRONICS AND INSTRUMENTATION ENGINEERING

QUESTION BANK

IV SEMESTER

EE3361 -DIGITAL LOGIC CIRCUITS

Regulation – 2023

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Prepared by

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SUBJECT : EE3361 -DIGITAL LOGIC CIRCUITS

SEM / YEAR : II / IV

UNIT-I - NUMBER SYSTEMS AND DIGITAL LOGIC FAMILIES

Number system, error detection, corrections & codes conversions, Boolean algebra: DeMorgan's theorem, switching functions and minimization using K-maps & Quine McCluskey method - Digital Logic Families -comparison of RTL, DTL, TTL, ECL and MOS families -operation, characteristics of digital logic family.

PART-A

Q.No	Questions	BT Level	Competence	CO
1.	What are the types of Number system?	BTL1	Remember	CO1
2.	Convert 378.9310 to octal	BTL2	Understand	CO1
3.	Contrast error detection and error correction codes?	BTL2	Understand	CO1
4.	Defin the concept of parity.	BTL2	Understand	CO1
5.	Summarize about the excess code.	BTL2	Understand	CO1
6.	State the associative property of boolean algebra.	BTL2	Understand	CO1
7.	State the distributive property of Boolean algebra.	BTL1	Remember	CO1
8.	Reduce A (A + B)	BTL2	Understand	CO1
9.	What are the methods adopted to reduce Boolean function?	BTL1	Remember	CO1
10.	Solve: $Y = C + \overline{BC}$	BTL1	Remember	CO1
11.	State De Morgan's theorem.	BTL1	Remember	CO1
12.	What are switching functions?	BTL1	Remember	CO1
13.	What are prime implicants in the Quine-McCluskey method?	BTL2	Remember	CO1
14.	What is minimization of switching functions?	BTL1	Remember	CO1
15.	List the different logic families.	BTL1	Remember	CO1
16.	Define noise margin.	BTL2	Understand	CO1
17.	What is fan-out of a gate ?	BTL2	Understand	CO1
18.	Define power dissipation.	BTL2	Understand	CO1
19.	Define propagation delay.	BTL2	Understand	CO1
20.	What is operating temperature ?	BTL1	Remember	CO1
21.	Mention the characteristics of RTL family.	BTL1	Remember	CO1
22.	Summarize the advantages of ECL as compared to TTL logic family.	BTL1	Remember	CO1

23.	Which is faster TTL or ECL?		BTL2	Understand	CO1
24.	List the advantages of DTL.		BTL2	Understand	CO1
	PART-B				
1.	i. Convert 378.9310 to octal ii. 5C716 to decimal	(8) (8)	BTL3	Apply	CO1
2.	Convert the following. i. $(1100)_2$ = (_____)$_{10}$ ii. $(137)_{10}$ = (_____)$_8$ iii. $(56)_{10}$ = (_____)$_8$ iv. $(223)_{10}$ = (_____)$_{16}$ v. $(DF)_{16}$ = (_____)$_{10}$	 (3) (3) (3) (3) (4)	BTL3	Apply	CO1
3.	Explain the procedure to form hamming code and how to detect error and correct the message as well as determine hamming code for the binary word 1001 for odd parity.	(16)	BTL3	Apply	CO1
4.	Evaluate error detection and correction code with examples.	(16)	BTL4	Analyze	CO1
5.	Compose the details of Boolean algebra with postulates and prove i. Absorption theorem ii. Associative law iii. Demorgan's theorem	(16)	BTL3	Apply	CO1
6.	Reduce the following (i) AB + (AC)' + AB'C (AB + C) (ii)Y = (A + B) (A + C') (B' + C')	(16)	BTL4	Analyze	CO1
7.	Apply the rules and convert the following SOP to standard SOP. i. F(A,B,C)=AC+AB+BC ii. F(A,B,C)=A+ABC	 (8) (8)	BTL3	Apply	CO1
8.	Analyze the rules for converting POS to standard POS. i. F(A,B,C)=(A+B).(B+C).(A+C) ii. F(A,B,C)=(A+B+C).A	 (8) (8)	BTL4	Analyze	CO1
9.	(i) Explain briefly about SOP and POS forms with example. (ii) Plot the logical expression ABCD + AB' C' D' + AB'C + AB on a 4 variable K-map. Obtain the simplified expression from the map.	(8) (8)	BTL4	Analyze	CO1
10.	Indulge the min terms and max terms and express the following in M-notation i. F(A,B,C)=ABC+AB'C+ABC'+A'BC ii. F(A,B,C)=(A+B+C).(A+B+C').(A'+B+C).(A+B'+C)	 (8) (8)	BTL3	Apply	CO1

11.	Given the 2 binary numbers X=1010100 and Y=1000011 perform the subtraction Y-X by using 2's complements	(16)	BTL3	Apply	CO1
12.	Simplify the Boolean function using Quine McCluskey's tabulation method:F(A,B,C,D)= ∑m(0,5,7,8,9,10,11,14,15)	(16)	BTL4	Analyze	CO1
13.	(i) Express the function Y = A+B' C in canonical SOP and canonical POS form. (ii) Design BCD to Excess 3 code converter.	(16)	BTL3	Apply	CO1
14.	Simplify the Boolean function using Quine McCluskey's tabulation method:F(A,B,C,D)= ∑m(0,4,5,7,8,11,12,15)	(16)	BTL4	Analyze	CO1
15.	Recall the postulates of Boolean algebra and prove any two theorems.	(16)	BTL4	Analyze	CO1
16.	Explain the characteristics and implementation of the following digital logic families. i. CMOS ii. ECL iii. TTL	(16)	BTL3	Apply	CO1
17.	Write short notes on following: i. RTL ii. DTL iii. ECL	(16)	BTL3	Apply	CO1

UNIT-II - COMBINATIONAL CIRCUITS

Combinational logic - representation of logic functions-SOP and POS forms, K-map representations - minimization using K maps - simplification and implementation of combinational logic – multiplexers and de multiplexers - code converters, adders, subtractors, Encoders and Decoders.

PART-A

Q.No	Questions	BT Level	Competence	CO
1.	Define combinational logic circuit.	BTL1	Remember	CO2
2.	Mention the dependency of the output in combinational circuits.	BTL2	Understand	CO2
3.	What are the four combinational logic circuits?	BTL1	Remember	CO2
4.	Infer the basic logic gates.	BTL2	Understand	CO2
5.	List the design procedure for combinational circuits	BTL1	Remember	CO2
6.	Interpret about magnitude comparator.	BTL1	Remember	CO2
7.	Bring out the applications of multiplexer.	BTL1	Remember	CO2
8.	Draw the logic diagram of a half adder.	BTL1	Remember	CO2
9.	What are called don't care conditions?	BTL2	Understand	CO2
10.	Draw half subtractor with logic diagram.	BTL1	Remember	CO2
11.	Recall the working of demultiplexer.	BTL1	Remember	CO2
12.	Infer the reason why multiplexer is called data selector.	BTL2	Understand	CO2
13.	Define half adder and full adder.	BTL2	Understand	CO2
14.	Draw OR gate using only NAND gates.	BTL2	Understand	CO2
15.	Implement the function $F=\sum(0,2,3,7)$ to form a logic diagram.	BTL2	Understand	CO2
16.	What is a prime implicant?	BTL1	Remember	CO2
17.	What is an essential implicant?	BTL1	Remember	CO2
18.	What is priority Encoder?	BTL1	Remember	CO2
19.	Draw the NAND gate circuit using NOT, AND & OR gates.	BTL2	Understand	CO2
20.	Draw the truth table of 2:1 MUX	BTL2	Understand	CO2
21.	Define multiplexer.	BTL1	Remember	CO2
22.	List the applications of Multiplexer	BTL2	Understand	CO2
23.	Compare and compile the difference between decoder and demultiplexer.	BTL2	Understand	CO2
24.	Interpret the block diagram of encoder.	BTL2	Understand	CO2

PART-B

1.	Design a half adder, full adder, half subtractor and full subtractor.	(16)	BTL6	Create	CO2
2.	Use two half adder to form a full adder.	(16)	BTL3	Apply	CO2
3.	Design a 4-bit gray to binary code converter and implement it using logic gates.	(16)	BTL6	Create	CO2

4.	Explain the implementation procedure using multiplexer and also implement the switching function using 8:1 multiplexer f(A,B,C,D)=∑m(0,1,3,4,8,9,15)	(16)	BTL4	Analyze	CO2
5.	Design a BCD to Excess 3 code converter and implement it using logic gates.	(16)	BTL6	Create	CO2
6.	Analyze and implement the switching function f(a,b,c)= ∑m(3,4,5,7) using suitable multiplexer.	(16)	BTL4	Analyze	CO2
7.	i. Implement the following Boolean function using 8:1 multiplexer. F(A, B, C, D) = A'BD' + ACD + A'C' D +B'CD ii. Explain the functionality of a Multiplexer?	(8) (8)	BTL3	Apply	CO2
8.	Propose the combinational circuit for a half adder and half subtractor.	(16)	BTL3	Apply	CO2
9.	Form full subtractor employing half subtractor.	(16)	BTL3	Apply	CO2
10.	Articulate the realization procedure using multiplexer and also implement the switching function using 8*1 multiplexer f(A,B,C,D)=∑m(0,2,3,4,8,9,14,15)	(16)	BTL4	Analyze	CO2
11.	Describe magnitude comparator and explain two bit magnitude comparator.	(16)	BTL3	Apply	CO2
12.	Implement the sum output of full adder using i. 4 X 1 multiplexer ii. 2 X 1 multiplexer	(16)	BTL4	Analyze	CO2
13.	Create a combinational circuit for full adder and full subtractor.	(16)	BTL3	Apply	CO2
14.	Design a full adder and half adder using 4*1 multiplexer.	(16)	BTL6	Create	CO2
15.	Summarize the following i. Demultiplxer ii. Encoder iii. Decoder iv. Magnitude comparator	(16)	BTL4	Analyze	CO2
16.	Propose a 4-bit gray to binary code converter and realize it using logic gates.	(16)	BTL3	Apply	CO2
17.	Implement the function using decoder. F(p,q,r,s) = Σ (0, 1, 2, 4, 7, 10, 11, 12)	(16)	BTL4	Analyze	CO2

UNIT-III - SYNCHRONOUS SEQUENTIAL CIRCUITS

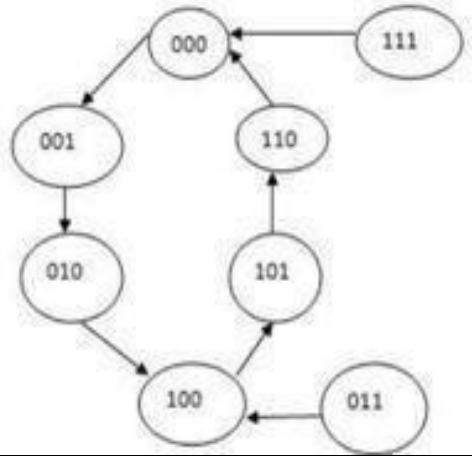
Sequential logic- SR, JK, D and T flip flops - level triggering and edge triggering - counters - asynchronous and synchronous type - Modulo counters - Shift registers - design of synchronous sequential circuits –Up-Down Counters, Ripple counter, state diagram; state reduction; state assignment with examples.

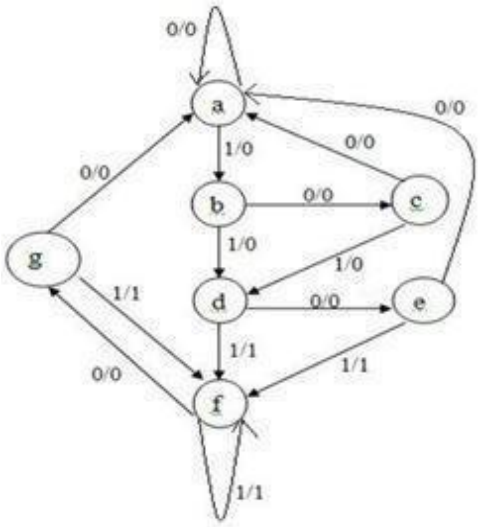
PART-A

Q.No	Questions	BT Level	Competence	CO
1.	Describe synchronous sequential circuit.	BTL1	Remember	CO3
2.	Compare combinational and sequential circuits.	BTL2	Understand	CO3
3.	State truth table for SR flip flop.	BTL1	Remember	CO3
4.	Interpret the benefits of state reduction.	BTL2	Understand	CO3
5.	What is the operation of T flip-flop?	BTL1	Remember	CO3
6.	Give the characteristic equation and state diagram of JK flip-flop.	BTL2	Understand	CO3
7.	What is a self-starting counter?	BTL1	Remember	CO3
8.	Bring out truth table for SR flip flop.	BTL2	Understand	CO3
9.	List out drawback of RS flip-flop.	BTL2	Understand	CO3
10.	Define race around condition.	BTL1	Remember	CO3
11.	What is a preset table counter and ripple counter?	BTL1	Remember	CO3
12.	List the drawback of SR flip-flop.	BTL2	Understand	CO3
13.	Convert T Flip Flop to D Flip Flop.	BTL2	Understand	CO3
14.	What is edge-triggered flip-flop?	BTL1	Remember	CO3
15.	Identify the truth table for T flip-flop.	BTL2	Understand	CO3
16.	Give the characteristic equation and characteristic table of T flip flop.	BTL1	Remember	CO3
17.	Design the excitation table for JK flip-flop.	BTL1	Remember	CO3
18.	Give the characteristic equation and state diagram of T flip-flop	BTL2	Understand	CO3
19.	Draw the excitation table for T flip-flop.	BTL2	Understand	CO3
20.	Draw the excitation table for D flip-flop.	BTL2	Understand	CO3
21.	Realize T flip-flop using JK flip-flop.	BTL1	Remember	CO3
22.	What is a master-slave flip-flop?	BTL1	Remember	CO3
23.	What is the operation of RS flip-flop?	BTL1	Remember	CO3
24.	Define state assignment.	BTL2	Understand	CO3

PART-B

1.	Explain the working of SR and JK flip-flops with logic symbols, truth tables, characteristic equations.	(16)	BTL4	Analyze	CO3
2.	Describe the working of D, and T flip-flops with logic symbols, truth tables, characteristic equations.	(16)	BTL4	Analyze	CO3
3.	Draw the logic diagram of 4-bit synchronous	(16)	BTL3	Apply	CO3

	counter. Explain the operation of the counter using the timing diagram				
4.	Explain the types of shift register in detail.	(16)	BTL4	Analyze	CO3
5.	A sequential circuit has two JK flip-flop A and B, two inputs x and y, and one output z. the equations are JA=Bx+B'y'; KA= B'xy' JB= A'x; KB=A+xy' Z=Ax'y'+Bx'y. Draw the logic diagram and state table.	(16)	BTL3	Apply	CO3
6.	i. Estimate a sequential circuit with two D-flip-flops A and B and one output x. When x=0, the state of the circuit goes through the state transitions from 00 01 11 10 00 and repeats. ii. Estimate mod 7 counter using D flip-flops.	(8) (8)	BTL3	Apply	CO3
7.	A sequential circuit has two JK flip-flops A and B. The flipflop input functions are: JA=B; JB=x KA= B x ; KB=A⊕x i. Draw the logic diagram of the circuit ii. Tabulate the state table iii. Draw the state diagram	 (5) (5) (6)	BTL4	Analyze	CO3
8.	Design a counter for the following state diagram 	(16)	BTL6	Create	CO3
9.	Explain in detail the concepts of level triggering and edge triggering in flip-flops. Compare them with suitable diagrams, timing waveforms, and applications.	(16)	BTL4	Analyze	CO3
10.	Determine the reduced state table for the given state table.	(16)	BTL4	Analyze	CO3

	<table><tr><th rowspan="2">Present state</th><th colspan="2">Next state</th><th colspan="2">Output</th></tr><tr><th>X = 0</th><th>X = 1</th><th>X = 0</th><th>X = 1</th></tr><tr><td>a</td><td>b</td><td>c</td><td>0</td><td>0</td></tr><tr><td>b</td><td>b</td><td>d</td><td>0</td><td>0</td></tr><tr><td>c</td><td>b</td><td>a</td><td>0</td><td>0</td></tr><tr><td>d</td><td>e</td><td>c</td><td>1</td><td>0</td></tr><tr><td>e</td><td>b</td><td>d</td><td>0</td><td>0</td></tr></table>				
11.	Design a 4-bit BCD ripple counters.	(16)	BTL6	Create	CO3
12.	Design a 3 bit binary counter using T flip-flop.	(16)	BTL6	Create	CO3
13.	Implement JK FF using SR FF.	(16)	BTL3	Apply	CO3
14.	Compile the logic diagram and state table for a sequential circuit has two JK flip-flop A and B, two inputs x and y, and one output z. the equations are JA=Bx+B'y'; KA= B'xy' JB= A'x; KB=A+xy' Z=Ax'y'+Bx'y.	(16)	BTL3	Apply	CO3
15.	Differentiate asynchronous and synchronous type counters.	(16)	BTL4	Analyze	CO3
16.	Design a 5-bit ring counter and mention its applications.	(16)	BTL6	Create	CO3
17.	Construct reduced state diagram for the following state diagram. 	(16)	BTL3	Apply	CO3

UNIT-IV - ASYNCHRONOUS SEQUENTIAL CIRCUITS AND PROGRAMMABILITY LOGIC DEVICES

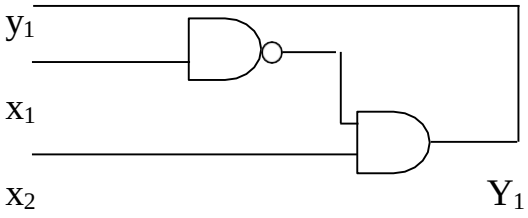
Transition stability, flow stability-race conditions, hazards & errors in digital circuits; analysis of asynchronous sequential logic circuits introduction to Programmability Logic Devices: PROM – PLA –PAL, CPLD-FPGA table.

PART-A

Q.No	Questions	BT Level	Competence	CO
1.	List the disadvantages of asynchronous sequential circuit.	BTL1	Remember	CO4
2.	Define asynchronous sequential machine.	BTL2	Understand	CO4
3.	Draw the block diagram of asynchronous sequential circuits.	BTL1	Remember	CO4
4.	What is meant by transition table?	BTL1	Remember	CO4
5.	Compare and compile the difference between flow table and transition table.	BTL2	Understand	CO4
6.	Identify races in Asynchronous sequential circuit.	BTL2	Understand	CO4
7.	Show fundamental mode of operation in asynchronous sequential circuits.	BTL1	Remember	CO4
8.	Compose the types of sequential circuits.	BTL2	Understand	CO4
9.	Compare critical race and non critical race.	BTL2	Understand	CO4
10.	Define flow table with example.	BTL2	Understand	CO4
11.	Outline deadlock condition.	BTL1	Remember	CO4
12.	Point out the definition for flow table in asynchronous sequential circuit.	BTL1	Remember	CO4
13.	Infer about basic storage element.	BTL2	Understand	CO4
14.	Point out the characteristic table of SR latch.	BTL2	Understand	CO4
15.	Identify the meaning of latch.	BTL2	Understand	CO4
16.	How many types of latches are?	BTL1	Remember	CO4
17.	Compile the application of latches.	BTL1	Remember	CO4
18.	List basic types of programmable logic devices.	BTL2	Understand	CO4
19.	Justify whether the fastest circuit is synchronous or asynchronous circuits?	BTL2	Understand	CO4
20.	Define EPROM.	BTL2	Understand	CO4
21.	What is programmable logic array?	BTL1	Remember	CO4
22.	List the major differences between PLA and PAL	BTL2	Understand	CO4
23.	Define PLD.	BTL1	Remember	CO4
24.	What is CPLD?	BTL1	Remember	CO4

PART-B

1.	Design an asynchronous sequential circuit has two inputs X_2 and X_1 and one output Z. When X_1=0, the output Z is to remain as 0 as long as X_1 is 0. The first change in X_2 that occurs while	(16)	BTL6	Design	CO4

	X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.				
2.	Explain the internal architecture of a CPLD and an FPGA with block diagrams.	(16)	BTL4	Analyze	CO4
3.	How do you identify and eliminate static and dynamic hazards from an asynchronous sequential circuit?	(16)	BTL3	Apply	CO4
4.	Discover an asynchronous sequential circuit with two inputs T and C. The output attains a value of 1 when T=1 & C moves from 1 to 0. Otherwise the output is 0.	(16)	BTL4	Analyze	CO4
5.	Describe the steps involved in design of asynchronous sequential circuit in detail with an example.	(16)	BTL4	Analyze	CO4
6.	i. How do you get output specifications from a flow table in asynchronous sequential circuit operating in fundamental mode? ii. When do you get the critical and non- critical races?How will you obtain race free conditions?	(8) (8)	BTL3 BTL3	Apply Apply	CO4 CO4
7.	An asynchronous sequential circuit is described by the following excitation and the output function Y=x1x2+(x1+x2)y. i. Draw the logic diagram of the circuit. ii. Derive the transition table and output map. iii. Describe the behaviour of the circuit.	 (4) (5) (7)	BTL4	Analyze	CO4
8.	Check whether the given asynchronous sequential circuit is stable or unstable  	(16)	BTL3	Apply	CO4
9.	Design a asynchronous sequential circuit with two input D and G and with one output Z. whenever G is 1 input D is transferred to Z. When G is 0 the output does not change for any charge in D. Use SR FF for implementation of the circuit.	(16)	BTL6	Design	CO4
10.	Propose an asynchronous sequential circuit has two inputs X_2 and X_1 and one output Z. When X_1=0, the output Z is to remain as 0 as long as X_1 is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z	(16)	BTL3	Apply	CO4

	will remain 1 until X_1 returns to 0.				
11.	Discuss about hazards in asynchronous sequential circuit and the ways to eliminate them.	(16)	BTL4	Analyze	CO4
12.	Derive the asynchronous sequential circuit specified by the flow table y \ x_1 x_2 a: a,0 | a,0 | a,0 | b,0 b: a,0 | a,0 | b,1 | b,0	(16)	BTL3	Apply	CO4
13.	Evaluate and sketch the logic diagram, transition table and output mapfor an asynchronous sequential circuit described by $Y=x_1x'_2+(x_1 + x'_2)$ y; z=y.	(16)	BTL4	Analyze	CO4
14.	Compile an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T=1 & C moves from 1 to 0. Otherwise the output is 0.	(16)	BTL3	Apply	CO4
15.	Explain the architectures of PLA ,PAL and PROM with neat block diagrams.	(16)	BTL3	Apply	CO4
16.	Design the following function using PLA and PAL: $F(X, Y, Z) = \Sigma m (0, 1, 3, 5, 7)$.	(16)	BTL6	Design	CO4
17.	Design a PLA structure using AND & OR logic for the following function. $F1=\sum m(0,1,2,3,4,7,8,11,12,15)$ $F2=\sum m(2,3,6,7,8,9,12,13)$ $F3=\sum(1,3,7,8,11,12,15)$ $F4=\sum(0,1,4,8,11,12,15)$	(16)	BTL6	Design	CO4

UNIT-V - VHDL

RTL Design – combinational logic – Sequential circuit – Operators – Introduction to Packages– Subprograms – Test bench. (Simulation /Tutorial Examples: adders, counters, flip flops, Multiplexers & De multiplexers).

PART-A

Q.No	Questions	BT Level	Competence	CO
1.	Summarize on RTL Design	BTL1	Remember	CO5
2.	What are the types of subprograms?	BTL2	Understand	CO5
3.	When can RTL be used to represent digital systems?	BTL1	Remember	CO5
4.	What are the various operators in VHDL?	BTL2	Understand	CO5
5.	What is Verilog?	BTL1	Remember	CO5
6.	What are the various modeling used in Verilog?	BTL1	Remember	CO5
7.	What is the structural gate-level modeling?	BTL1	Remember	CO5
8.	Define the term package in VHDL.	BTL2	Understand	CO5
9.	Develop a VHDL behavioral model for D-flip-flop.	BTL2	Understand	CO5
10.	Write the VHDL code for a logical gate which gives high output only when both the inputs are high.	BTL1	Remember	CO5
11.	Name any four hardware description language test benches.	BTL1	Remember	CO5
12.	List the syntax for package declaration and package body in VHDL	BTL2	Understand	CO5
13.	Write VHDL code for 2*1 MUX using behavioral modeling	BTL2	Understand	CO5
14.	Give the two blocks in behavioral modeling.	BTL1	Remember	CO5
15.	Display the function of wait statement in VHDL package?	BTL2	Understand	CO5
16.	Compile VHDL code for half adder in data flow model.	BTL1	Remember	CO5
17.	List the merits of hardware languages.	BTL1	Remember	CO5
18.	What is the function of wait statement in VHDL package? Compose the operators used in VHDL.	BTL1	Remember	CO5
19.	Predict the need for VHDL.	BTL1	Remember	CO5
20.	Categorize different test bench.	BTL2	Understand	CO5
21.	What is a Procedure?	BTL1	Remember	CO5
22.	List the importance of any hardware description language test benches.	BTL2	Understand	CO5
23.	What is package declaration?	BTL2	Understand	CO5
24.	Write the syntax for package declaration?	BTL2	Understand	CO5

PART-B

1.	Explain in detail about the RTL design Procedure	(16)	BTL4	Analyze	CO5
2.	Describe the role of RTL simulation tools in the design process	(16)	BTL4	Analyze	CO5

3.	Write a note on simulation and synthesis	(16)	BTL3	Apply	CO5
4.	Explain the different timing control available in VHDL with suitable examples	(16)	BTL4	Analyze	CO5
5.	i. Write the VHDL code for a logical gate which gives high output only when both the inputs are high ii. Write the VHDL entity for a full adder	(8) (8)	BTL4	Analyze	CO5
6.	Write the VHDL code for a D-flip flop		BTL3	Apply	CO5
7.	Write short notes on package and subprograms	(16)	BTL4	Analyze	CO5
8.	Write the VHDL code to realize a 2:1 mulitplexer using data flow modeling	(16)	BTL4	Analyze	CO5
9.	Write the VHDL code to realize a full adder using behavioral modeling and structural modeling.	(16)	BTL4	Analyze	CO5
10.	Write the VHDL code to realize a 3-bit gray code counter using case statement.	(16)	BTL4	Analyze	CO5
11.	Write VHDL code for Binary UP/ DOWN counter using JK flip- flops.	(16)	BTL4	Analyze	CO5
12.	Design a 3 bit magnitude comparator and write the VHDL coding to realize it using structural modeling.	(16)	BTL3	Apply	CO5
13.	Explain in detail the concept of Structural modeling in VHDL with an example of full adder.	(16)	BTL4	Analyze	CO5
14.	Design a VHDL code for full adder and 8*1 MUX	(16)	BTL6	Create	CO5
15.	Write the VHDL code to realize a half adder using behavioral modeling and structural modeling.	(16)	BTL3	Apply	CO5
16.	Represent with neat diagram about the MOS logic circuit for NOT gate and explicate its operation.	(16)	BTL3	Apply	CO5
17.	Establish the circuit diagram of CMOS NOR gate.	(16)	BTL3	Apply	CO5