

# **SRM VALLIAMMAI ENGINEERING COLLEGE**

**(An Autonomous Institution)**

SRM Nagar, Kattankulathur – 603 203

## **DEPARTMENT OF ELECTRONICS AND INSTRUMENTATION ENGINEERING**

**Lab Manual  
IV SEMESTER**

**EI3467– Linear and Digital Integrated Circuits Laboratory**

**Regulation – 2023**

**Academic Year 2025-2026 (Even Semester)**



*Prepared by*

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## **SYLLABUS**

### **EI3467 LINEAR AND DIGITAL INTEGRATED CIRCUITS LABORATORY**

#### **OBJECTIVES:**

- To learn design, testing and characterizing of various combinational logic circuits.
- To learn design, testing and characterizing of applications like Mux, Demux, Encoder and Decoder circuits.
- To learn design, testing and characterizing of Synchronous and Asynchronous digital circuits.
- To learn design, testing and characterizing of circuit behavior with analog ICs.
- To study about working of 566 IC and LM 317 IC

#### **LIST OF EXPERIMENTS:**

1. Design and implementation of adder, subtractor. (2 bit, 3 bit)
2. Design and implementation of Code converters: Excess-3 to BCD and Binary to Gray code converter and vice-versa
3. Design and implementation of Parity generator and parity checking
4. Design and implementation of Encoders and Decoders
5. Design and implementation of Mux and Demux (4:1)
6. Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO
7. Design and implementation of 3-bit modulo counters. (Synchronous /Asynchronous)
8. Application of Op-Amp: inverting and non-inverting amplifier, Adder, Subtractor.
9. Design and implementation of comparator, Integrator and Differentiator using opamp.
10. Astable, Monostable operation of Timer IC NE/SE 555 timer.
11. Voltage to frequency characteristics of NE/ SE 566 IC.
- 12 .Variable Voltage Regulator using IC LM317.

#### **OUTCOMES:**

- Ability to understand and implement combinational circuits Functions.
- Ability to understand the importance of encoders, decoders, multiplexers and demultiplexers
- Ability to Design and implement sequential circuits.
- Ability to acquire knowledge on Application of Op-Amp.
- Ability to Design and implement voltage regulators.
- Ability to acquire knowledge on Application of timer and PLL

## **LIST OF EXPERIMENTS**

### **I CYCLE:**

1. Design and implementation of adder, subtractor. (2 bit, 3 bit)
2. Design and implementation of Code converters: Excess-3 to BCD and Binary to Gray code converter and vice-versa
3. Design and implementation of Parity generator and parity checking
4. Design and implementation of Encoders and Decoders
5. Design and implementation of Mux and Demux (4:1)
6. Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO

### **II CYCLE:**

7. Design and implementation of 3-bit modulo counters. (Synchronous /Asynchronous)
8. Application of Op-Amp: inverting and non-inverting amplifier, Adder, Subtractor.
9. Design and implementation of comparator, Integrator and Differentiator using opamp.
10. Astable, Monostable operation of Timer IC NE/SE 555 timer.
11. Voltage to frequency characteristics of NE/ SE 566 IC.
12. Variable Voltage Regulator using IC LM317.

Ex.No:

## DESIGN AND IMPLEMENTATION OF ADDER/SUBTRACTOR

Date:

### AIM:

To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truth table using logic gates.

### APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7432, 7408, 7486, 7483	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

### THEORY:

The most basic arithmetic operation is the addition of two binary digits. There are four possible elementary operations, namely,

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

The first three operations produce a sum of whose length is one digit, but when the last operation is performed the sum is two digits. The higher significant bit of this result is called a carry and lower significant bit is called the sum.

### HALF ADDER:

A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables produce the sum and carry bits.

### FULL ADDER:

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

## HALF ADDER

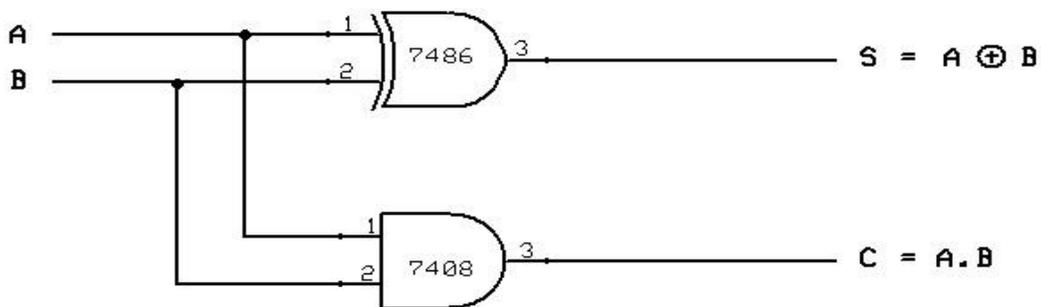
TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	S	C
1.	0	0	0	0
2.	0	1	1	0
3.	1	0	1	0
4.	1	1	0	1

DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as, Sum,  $S = A \oplus B$  ; Carry,  $C = A \cdot B$

CIRCUIT DIAGRAM:



## FULL ADDER

TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	SUM	CARRY
1.	0	0	0	0	0
2.	0	0	1	1	0
3.	0	1	0	1	0
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	1
7.	1	1	0	0	1
8.	1	1	1	1	1

## DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as,  $SUM = A'B'C + A'BC' + AB'C' + ABC$ ;  $CARRY = A'BC + AB'C + ABC' + ABC$  Using Karnaugh maps the reduced expression for the output bits can be obtained as,

### SUM

		BC			
		B'C'	B'C	BC	BC'
A	A'	0	1	0	1
	A	1	0	1	0

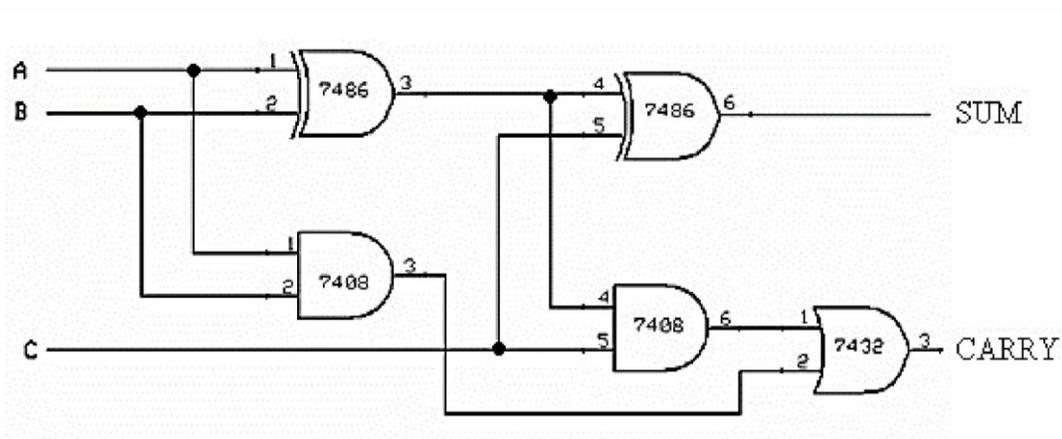
$$SUM = A'B'C + A'BC' + AB'C' + ABC = A \oplus B \oplus C$$

### CARRY

		BC			
		B'C'	B'C	BC	BC'
A	A'	0	0	1	0
	A	0	1	1	1

$$CARRY = AB + AC + BC$$

## CIRCUIT DIAGRAM:



## HALF SUBTRACTOR:

A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits.

## FULL SUBTRACTOR:

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate.

## HALF SUBTRACTOR

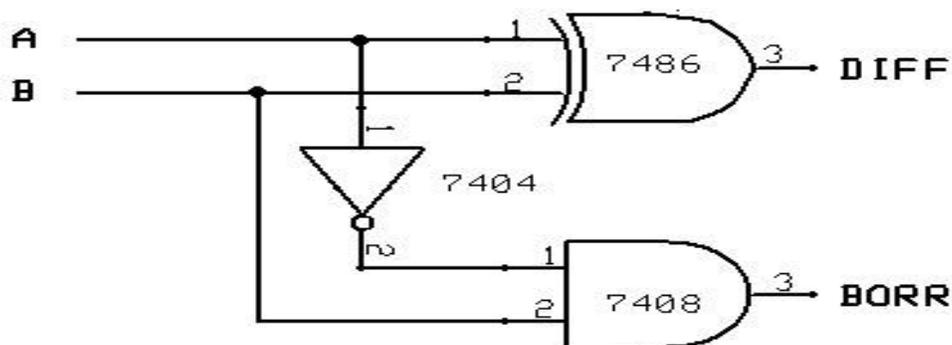
TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	DIFF	BORR
1.	0	0	0	0
2.	0	1	1	1
3.	1	0	1	0
4.	1	1	0	0

DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as, Difference,  $DIFF = A \oplus B$ ; Borrow,  $BORR = A' \cdot B$

CIRCUIT DIAGRAM:



## FULLS UBTRACTOR

TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	DIFF	BORR
1.	0	0	0	0	0
2.	0	0	1	1	1
3.	0	1	0	1	1
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	0
7.	1	1	0	0	0
8.	1	1	1	1	1

## DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as,

Difference,  $DIFF = A'B'C + A'BC' + AB'C' + ABC$

Borrow,  $BORR = A'BC + AB'C + ABC' + ABC$ . Using Karnaugh maps the reduced expression for the output bits can be obtained as,

### DIFFERENCE

A \ BC	BC			
	B'C'	B'C	BC	BC'
A'	0	1	0	1
A	1	0	1	0

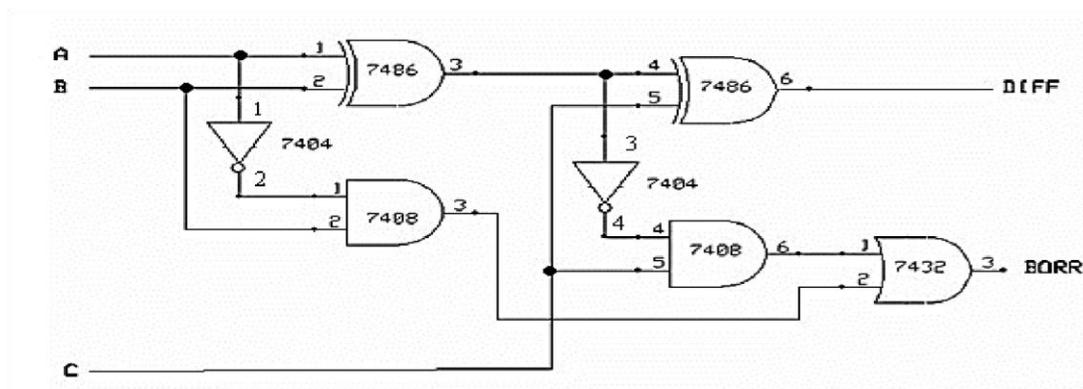
$$A'B'C + A'BC' + AB'C' + ABC = A \oplus B \oplus C$$

### BORROW

A \ BC	BC			
	B'C'	B'C	BC	BC'
A'	0	1	1	1
A	0	0	1	0

$$BORROW = A'B + A'C + BC$$

### CIRCUIT DIAGRAM:



## **PROCEDURE:**

1. The connections are given as per the circuit diagram.
2. Two 4 – bit numbers added or subtracted depend upon the control input and the output is obtained.
3. Apply the inputs and verify the truth table for the half adder or s subtractor and full adder or subtractor circuits.

## **DISCUSSION QUESTIONS:**

1. What is a combinational circuit?
2. What is different between combinational and sequential circuit?
3. What are the gates involved for binary adder?
4. List the properties of Ex-Nor gate?
5. What is the expression for sum and carry in half and full adder?

## **RESULT:**

Thus the half adder, full adder, half subtractor and full subtractor circuits were designed and their truth table were verified.

Ex. No:

Date:

## **DESIGN AND IMPLEMENTATION OF CODE CONVERTER**

### **AIM:**

To construct and verify the performance of binary to gray and gray to binary.

### **APPARATUS REQUIRED:**

<b>S. No</b>	<b>Name</b>	<b>Specification</b>	<b>Quantity</b>
1.	IC	7404, 7486	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

### **THEORY:**

#### **BINARY TO GRAY:**

The MSB of the binary code alone remains unchanged in the Gray code. The remaining bits in the gray are obtained by EX-OR ing the corresponding gray code bit and previous bit in the binary code. The gray code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers.

#### **GRAY TO BINARY:**

The MSB of the Gray code remains unchanged in the binary code the remaining bits are obtained by EX – OR ing the corresponding gray code bit and the previous output binary bit.

### **PROCEDURE:**

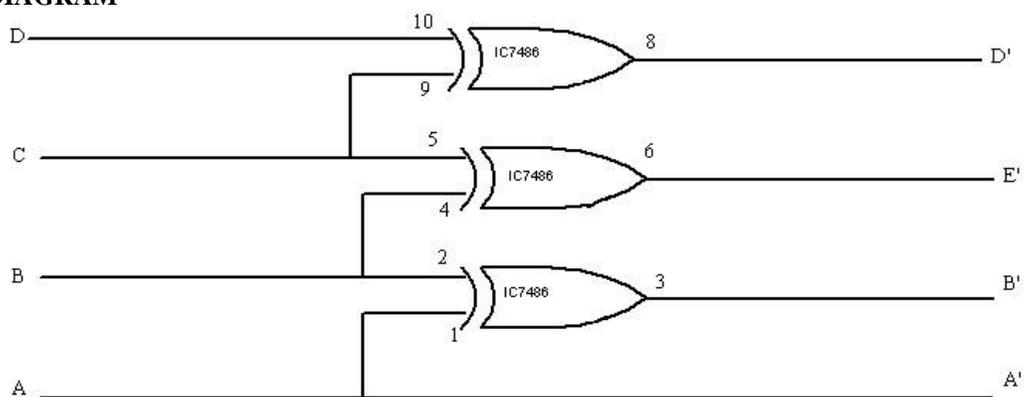
- Connections are given as per the logic diagram.
- The given truth tables are verified.

## BINARY TO GRAY:

### TRUTH TABLE

Decimal	Binary code				Gray code			
	D	C	B	A	D'	C'	B'	A'
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

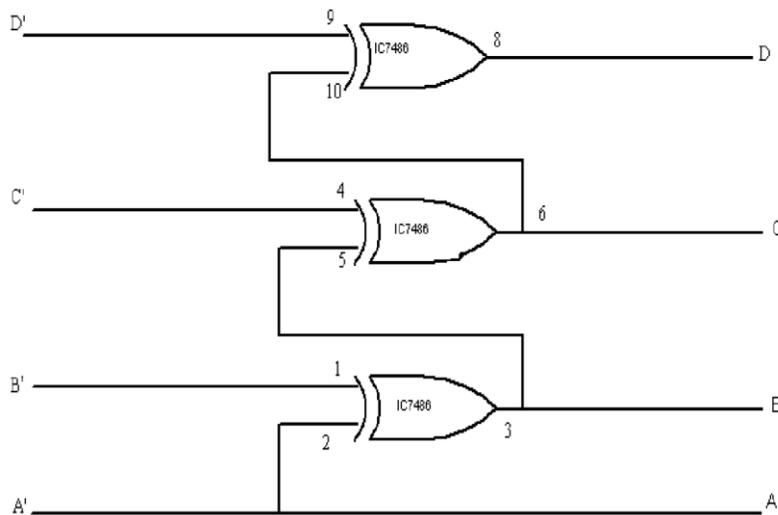
### LOGIC DIAGRAM



**GRAY TO BINARY**  
**TRUTH TABLE**

Decimal	Gray code				Binary code			
	D'	C'	B'	A'	D	C	B	A
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	1	0	0	1	0
3	0	0	1	0	0	0	1	1
4	0	1	1	0	0	1	0	0
5	0	1	1	1	0	1	0	1
6	0	1	0	1	0	1	1	0
7	0	1	0	0	0	1	1	1
8	1	1	0	0	1	0	0	0
9	1	1	0	1	1	0	0	1
10	1	1	1	1	1	0	1	0
11	1	1	1	0	1	0	1	1
12	1	0	1	0	1	1	0	0
13	1	0	1	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	0	1	1	1	1

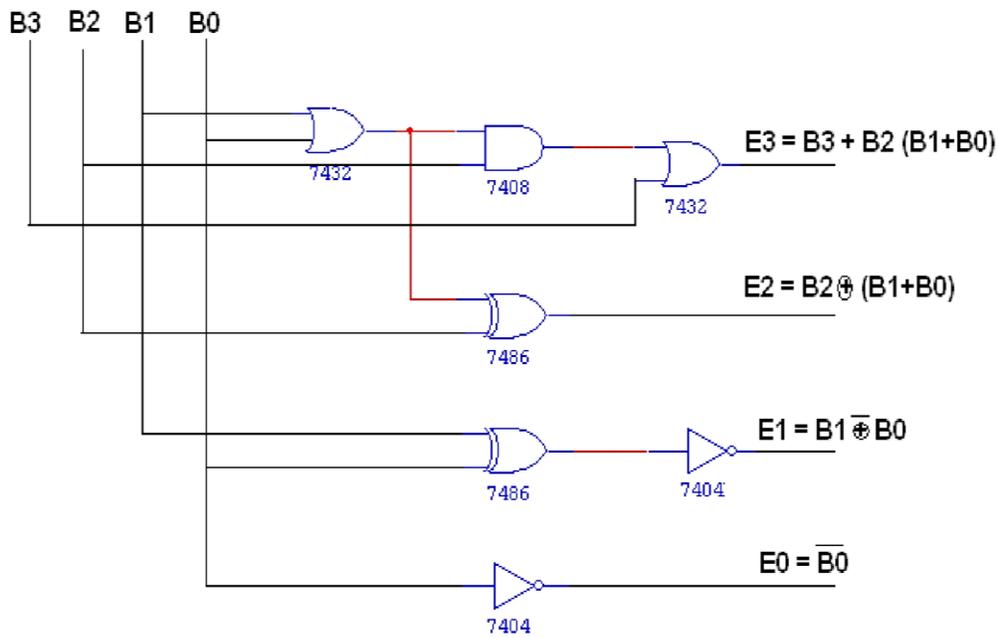
**LOGIC DIAGRAM**



**BCD TO EXCESS-3**  
**TRUTH TABLE**

BCD Input				Excess-3 Output			
B3	B2	B1	B0	E3	E2	E1	E0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

**Logic diagram**

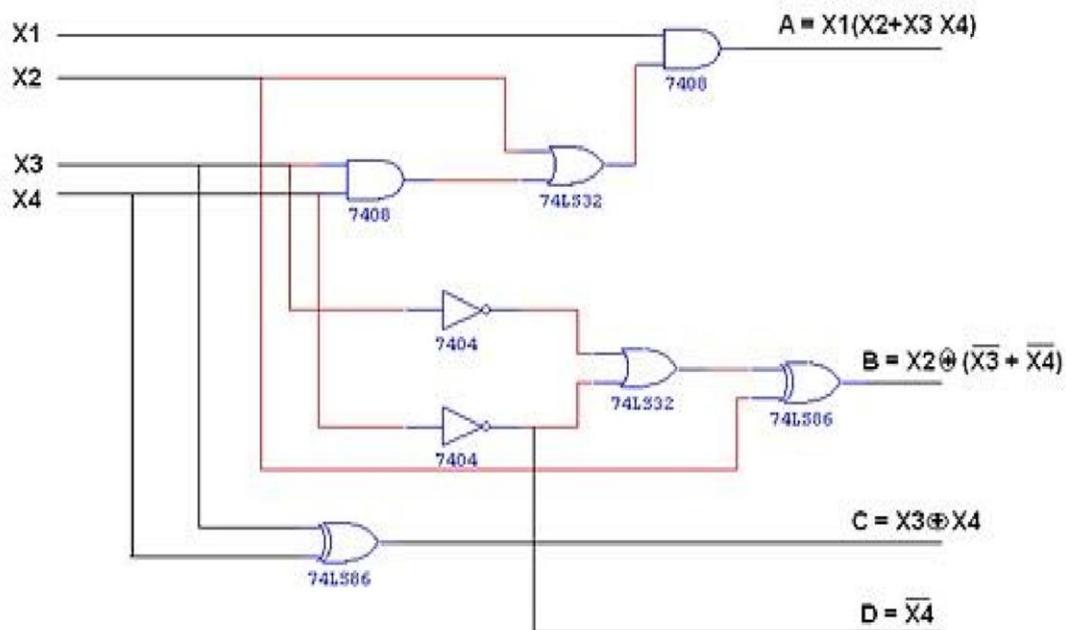


## EXCESS-3 TO BCD

### TRUTH TABLE

Excess-3 Input				BCD Output			
E3	E2	E1	E0	B3	B2	B1	B0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

### Logic diagram



### **DISCUSSION QUESTIONS:**

1. List the procedures to convert gray code into binary?
2. Why weighted code is called as reflective codes?
3. What is a sequential code?
4. What is error deducting code?
5. What is ASCII code?

### **RESULT:**

The design of the three bit Binary to Gray code converter & Gray to Binary code converter circuits was done and its truth table was verified

Ex. No:

Date: **DESIGN AND IMPLEMENTATION OF PARITY GENERATOR AND CHECKER**

**AIM:**

To design and verify the truth table of a three bit Odd Parity generator and checker & Even Parity Generator And Checker.

**APPARATUS REQUIRED:**

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	EX-OR gate	IC 7486	
3.	NOT gate	IC 7404	
4.	Connecting wires		As required

**THEORY:**

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.

In even parity the added parity bit will make the total number of 1's an even amount and in odd parity the added parity bit will make the total number of 1's an odd amount.

In a three bit odd parity generator the three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit. The parity checker circuit checks for possible errors in the transmission.

Since the information was transmitted with odd parity the four bits received must have an odd number of 1's. An error occurs during the transmission if the four bits received have an even number of 1's, indicating that one bit has changed during transmission. The output of the parity checker is denoted by PEC (parity error check) and it will be equal to 1 if an error occurs, i.e., if the four bits received has an even number of 1's.

## PARITY GENERATOR

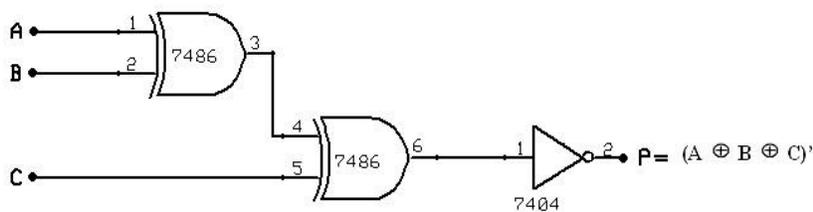
TRUTH TABLE:

S.No	INPUT ( Three bit message)			OUTPUT ( Odd Parity bit)	OUTPUT ( Even Parity bit)
	A	B	C	P	P
1.	0	0	0	1	0
2.	0	0	1	0	1
3.	0	1	0	0	1
4.	0	1	1	1	0
5.	1	0	0	0	1
6.	1	0	1	1	0
7.	1	1	0	1	0
8.	1	1	1	0	1

From the truth table the expression for the output parity bit is,  $P(A, B, C) = \Sigma (0, 3, 5, 6)$  Also written as,  $P = A'B'C' + A'BC + AB'C + ABC' = (A \oplus B \oplus C)'$

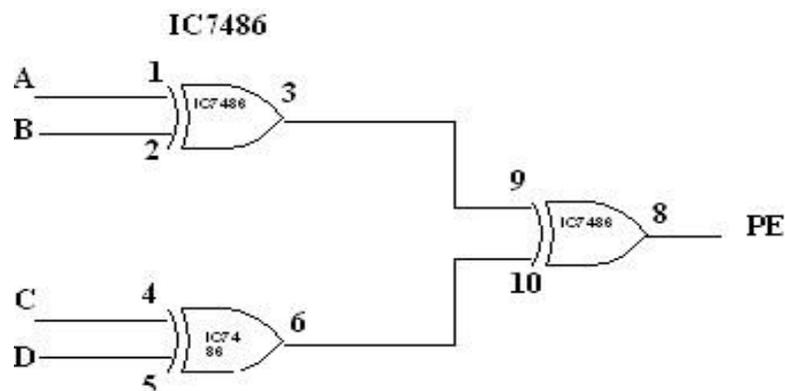
**CIRCUIT DIAGRAM:**

### ODD PARITY GENERATOR

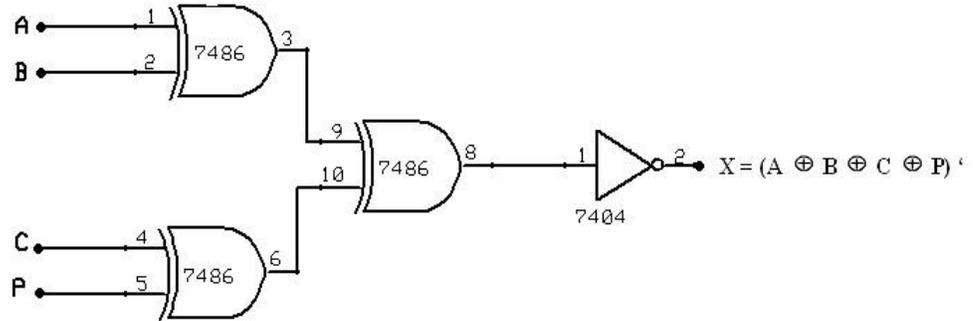


**CIRCUIT DIAGRAM:**

### EVEN PARITY GENERATOR



## PARITY CHECKER



### **PROCEDURE:**

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7<sup>th</sup> pin is grounded and 14<sup>th</sup> pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the Parity generator and checker.

### **DISCUSSION QUESTIONS:**

1. What is parity bit?
2. Why parity bit is added to message?
3. What is parity checker?
4. What is odd parity and even parity?
5. What are the gates involved for parity generator?

### **RESULT:**

The design of the three bit odd Parity generator and checker & Even Parity Generator and Checker circuits was done and their truth tables were verified.

Ex. No:

## DESIGN AND IMPLEMENTATION OF ENCODER

Date:

### AIM:

To design and implement encoder using IC 74148 (8-3 encoder)

### APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	74148	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

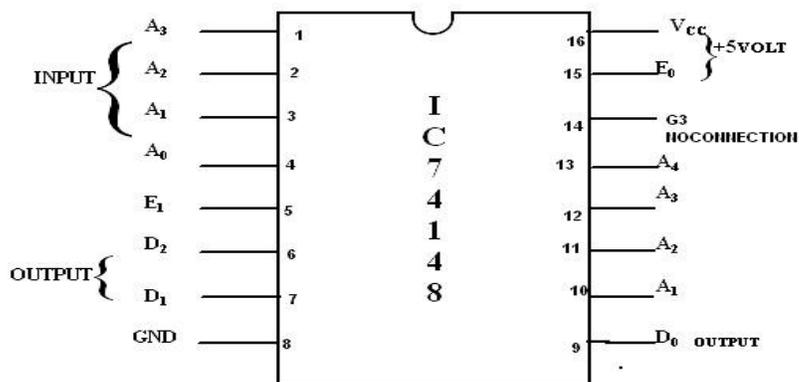
### THEORY:

An encoder is digital circuit that has  $2^n$  input lines and n output lines. The output lines generate a binary code corresponding to the input values 8 – 3 encoder circuit has 8 inputs, one for each of the octal digits and three outputs that generate the corresponding binary number. Enable inputs  $E_1$  should be connected to ground and  $E_0$  should be connected to  $V_{CC}$

### PROCEDURE:

- Connections are given as per the logic diagram.
- The truth table is verified by varying the inputs.

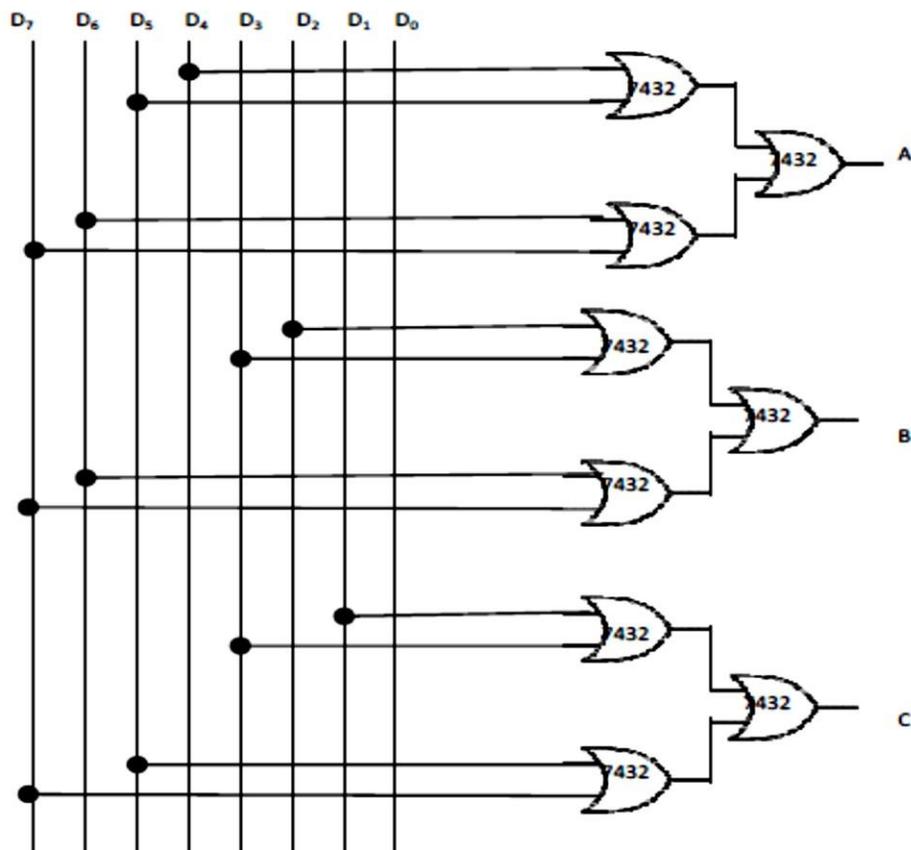
### PIN DIAGRAM



## TRUTH TABLE

Input								Output		
D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	A	B	C
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

## LOGIC DIAGRAM:



## DESIGN AND IMPLEMENTATION OF DECODER

### AIM:

To design and implement decoder using IC 74155 (3-8 decoder).

### APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	74155	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

### THEORY:

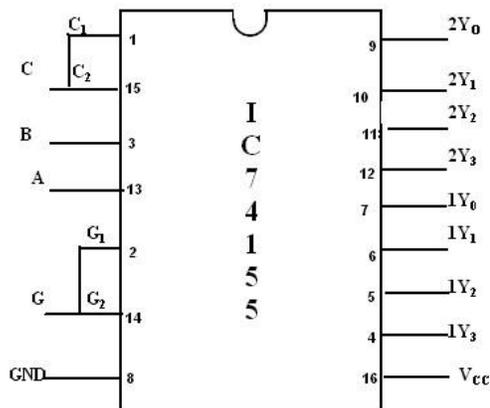
A decoder is a combinational circuit that converts binary information from  $n$  input lines to  $2^n$  unique output lines.

In 3-8 line decoder the three inputs are decoded into eight outputs in which each output representing one of the minterm of 3 input variables. IC 74155 can be connected as a dual 2\*4 decoder or a single 3\*8 decoder desired input in  $C_1$  and  $C_2$  must be connected together and used as the C input.  $G_1$  and  $G_2$  should be connected and used as the G (enable) input. G is the enable input and must be equal to 0 for proper operation.

### PROCEDURE:

- Connections are given as per the logic diagram.
- The truth table is verified by varying the inputs.

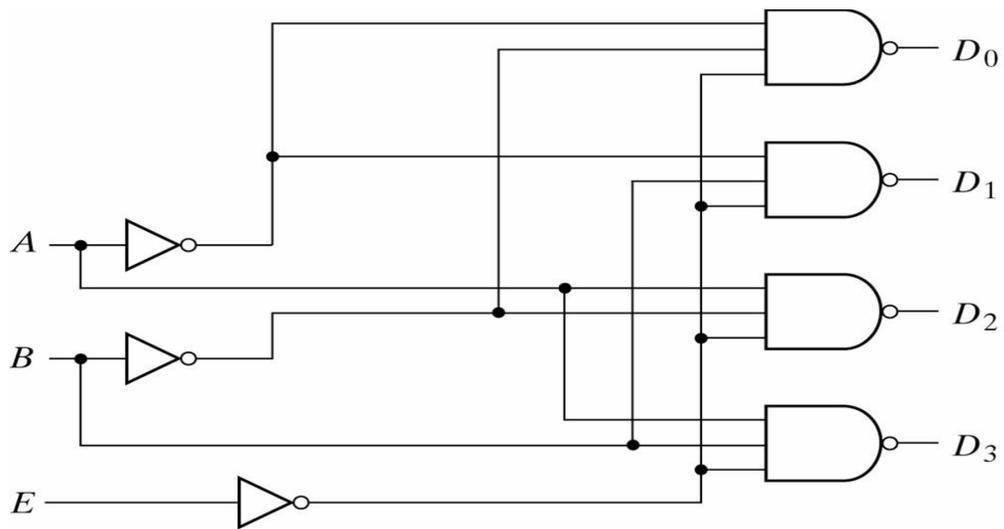
### PIN DIAGRAM



### TRUTH TABLE

$E$	$A$	$B$	$D_0$	$D_1$	$D_2$	$D_3$
1	$X$	$X$	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

### LOGIC DIAGRAM:



### **DISCUSSION QUESTIONS:**

1. How the output line will be activated in decoder circuit?
2. What are the necessary steps for implementing higher order decoders?
3. What is the use of code converters?
4. How to convert BCD to Decimal decoder?
5. What is seven segment displays?
6. What is the other name of encoder?
7. What is encoding?
8. What are the applications of encoder?
9. What is BCD encoder?

### **RESULT:**

Thus the encoder and decoder circuits were designed and implemented.

Ex. No: **DESIGN AND IMPLEMENTATION OF MULTIPLEXER & DEMULTIPLEXER**

Date:

**AIM:**

To design and verify the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.

**APPARATUS REQUIRED:**

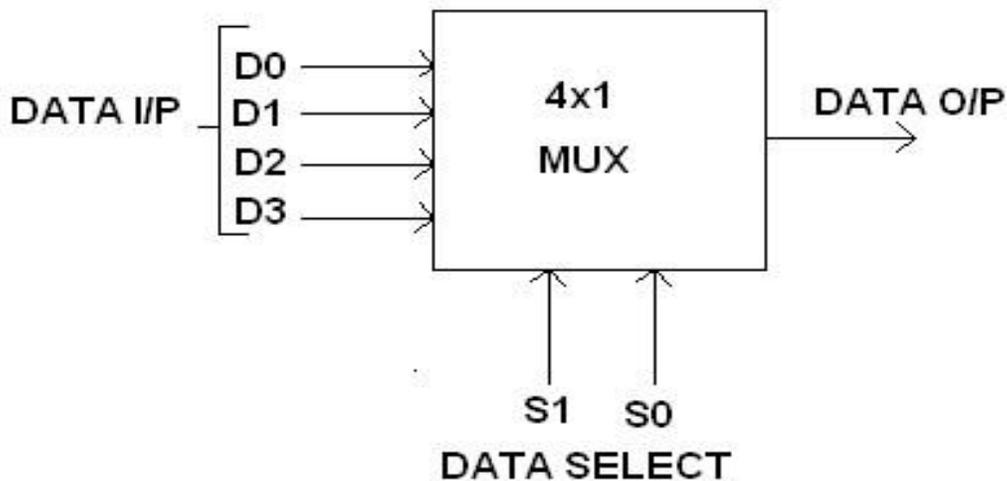
S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	OR gate	IC 7432	
3.	NOT gate	IC 7404	
4.	AND gate ( three input )	IC 7411	
5.	Connecting wires		As required

**THEORY:**

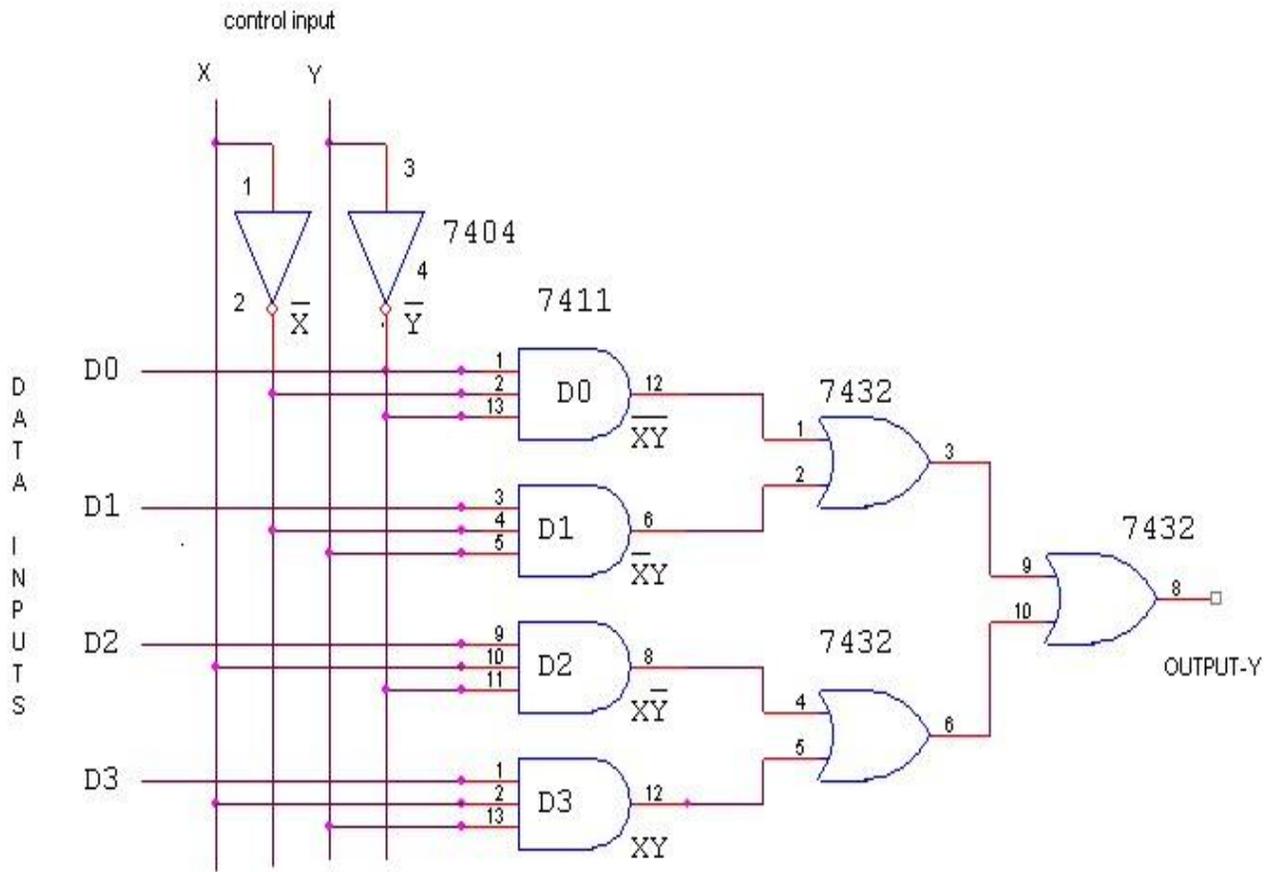
Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are  $2^n$  input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of  $2^n$  possible output lines. The selection of specific output line is controlled by the values of n selection lines.

**BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:**



**CIRCUIT DIAGRAM : (4 x 1)**

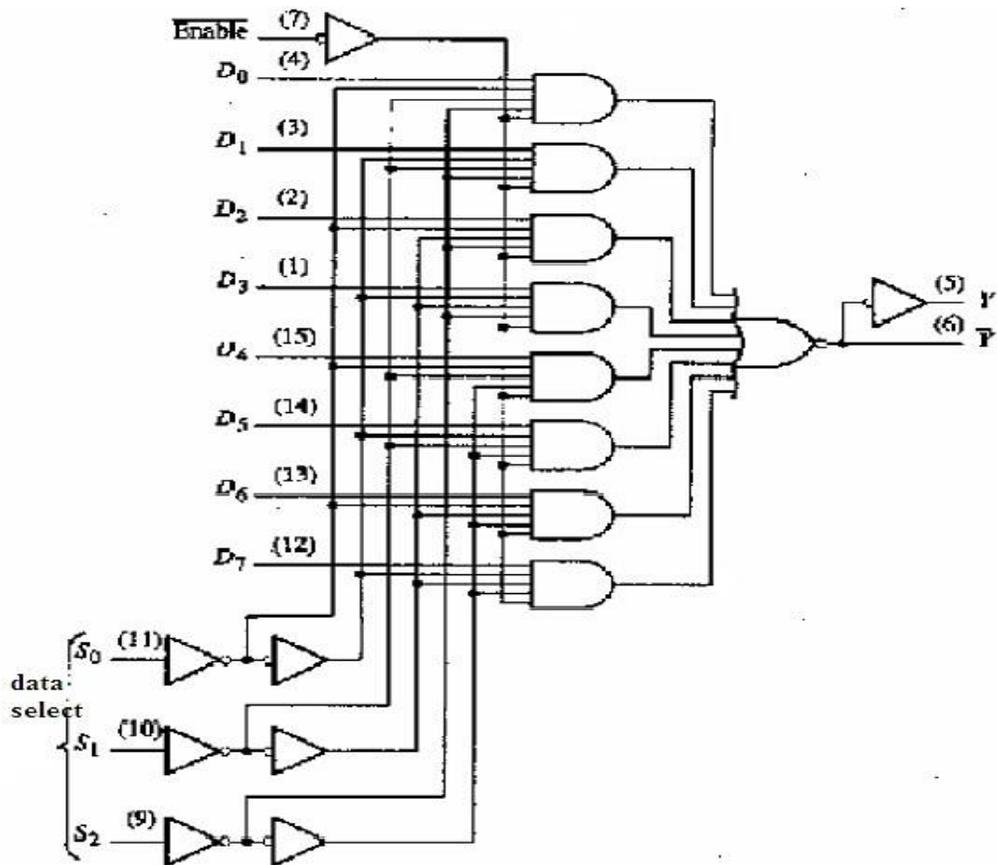


**FUNCTION TABLE (4 x 1)**

X	Y	OUTPUTS (Y)
0	0	$D0 \rightarrow D0 X' Y'$
0	1	$D1 \rightarrow D1 X' Y$
1	0	$D2 \rightarrow D2 X Y'$
1	1	$D3 \rightarrow D3 X Y$

$$Y = D0 X' Y' + D1 X' Y + D2 X Y' + D3 X Y$$

**CIRCUIT DIAGRAM (8 X 1)**

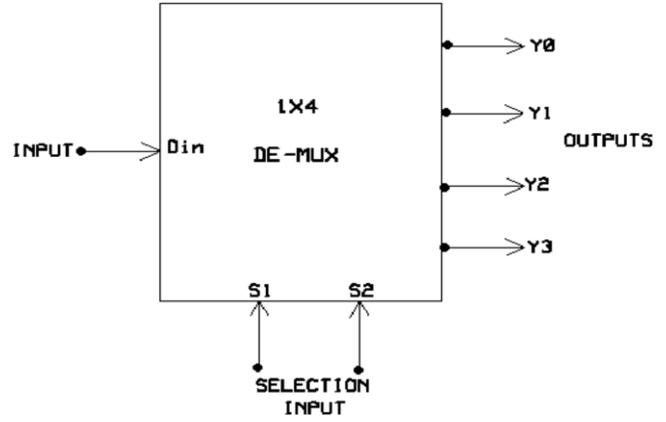


**FUNCTION TABLE (8 x 1)**

S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	OUTPUTS(Y)
0	0	0	D <sub>0</sub>
0	0	1	D <sub>1</sub>
0	1	0	D <sub>2</sub>
0	1	1	D <sub>3</sub>
1	0	0	D <sub>4</sub>
1	0	1	D <sub>5</sub>
1	1	0	D <sub>6</sub>
1	1	1	D <sub>7</sub>

## 1X4 DEMULTIPLEXER

**LOGIC SYMBOL:**

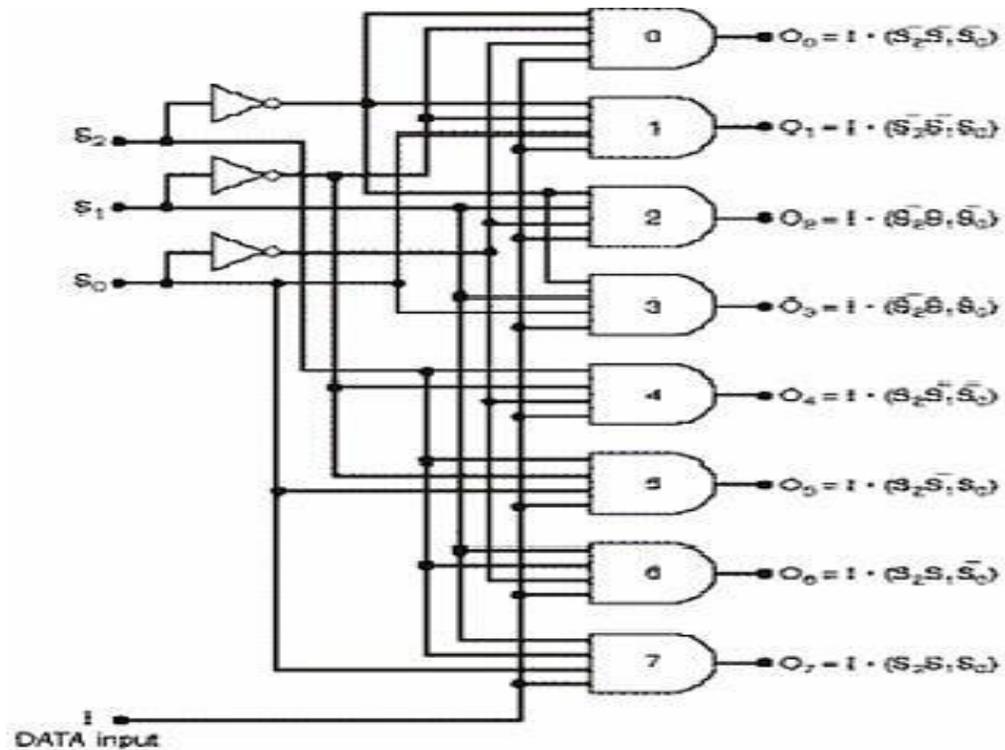


**TRUTH TABLE:**

S.No	INPUT			OUTPUT			
	S1	S2	Din	Y0	Y1	Y2	Y3
1.	0	0	0	0	0	0	0
2.	0	0	1	1	0	0	0
3.	0	1	0	0	0	0	0
4.	0	1	1	0	1	0	0
5.	1	0	0	0	0	0	0
6.	1	0	1	0	0	1	0
7.	1	1	0	0	0	0	0
8.	1	1	1	0	0	0	1



### CIRCUIT DIAGRAM:



### PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7<sup>th</sup> pin is grounded and 14<sup>th</sup> pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the multiplexer & demultiplexer.

### DISCUSSION QUESTIONS:

1. What is the other name of de-multiplexer?
2. Compare MUX and DE-MUX?
3. How many select lines needed for four outputs of DE-MUX?
4. What is other name of multiplexer?
5. What is serial to parallel converter?
6. What is the use of select lines?
7. How to enable the multiplexer?
8. What are the applications of multiplexer?

### RESULT:

The design of the 4x1 Multiplexer and 1x4 Demultiplexer circuits was done and their truth tables were verified.

Ex. No: **DESIGN AND IMPLEMENTATION OF SHIFT REGISTERS**

Date:

**AIM:**

To implement the following shift register using flip flop

- (i) SIPO
- (ii) SISO
- (iii) PISO
- (iv) PIPO

**APPARATUS REQUIRED:**

S. No	Name	Specification	Quantity
1.	IC	7474	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

**THEORY:**

A register is used to move digital data. A shift register is a memory in which information is shifted from one position in to another position at a line when one clock pulse is applied. The data can be shifted either left or right direction towards right or towards left.

A shift register can be used in four ways depending upon the input in which the data are entered in to and takes out of it. The four configuration are given as

Serial input – Serial output

Parallel input – Serial output

Serial input – Parallel output

Parallel input – Parallel output

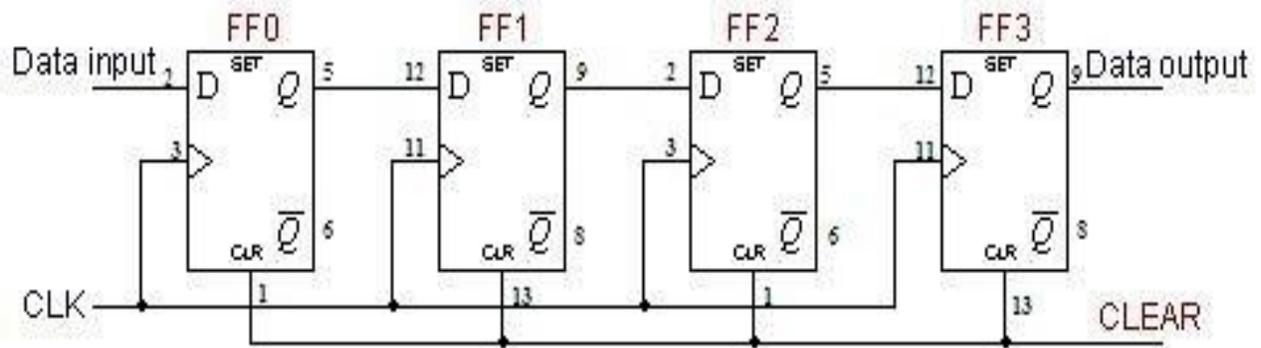
RS or JK flip flop are used to construct shift register have D flip flop is used for constructing shift register.

**PROCEDURE:**

1. Give the connections as per the circuit
2. Set or Reset at the pin 2 which it's the MSB of serial data.

3. Apply a single clock Set or Reset second digital input at pin 2.
4. Repeat step 2 until all 4-bit data are taken away.

**SHIFT REGISTER: SISO:**

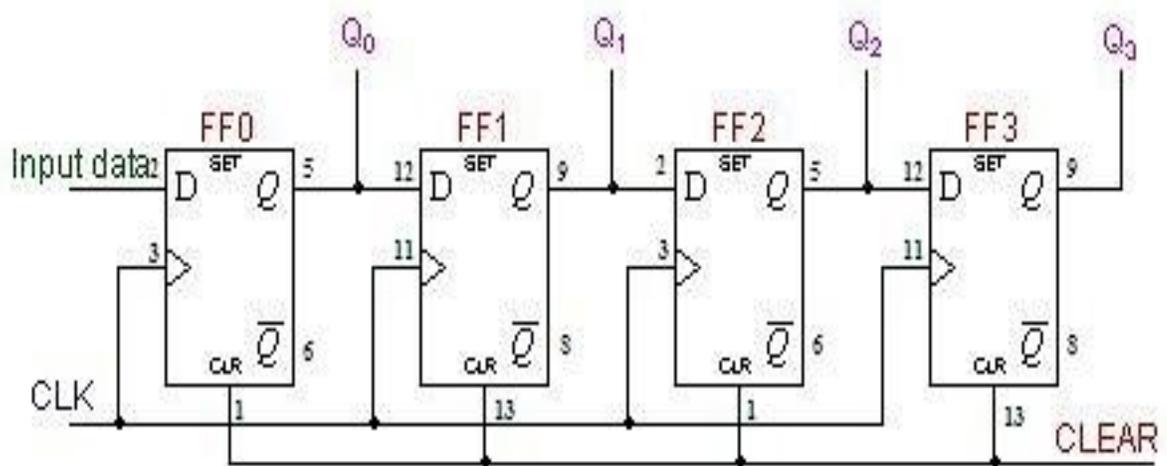


**Truth table:**

Data input = 1001

Clock	Serial input	Serial output
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

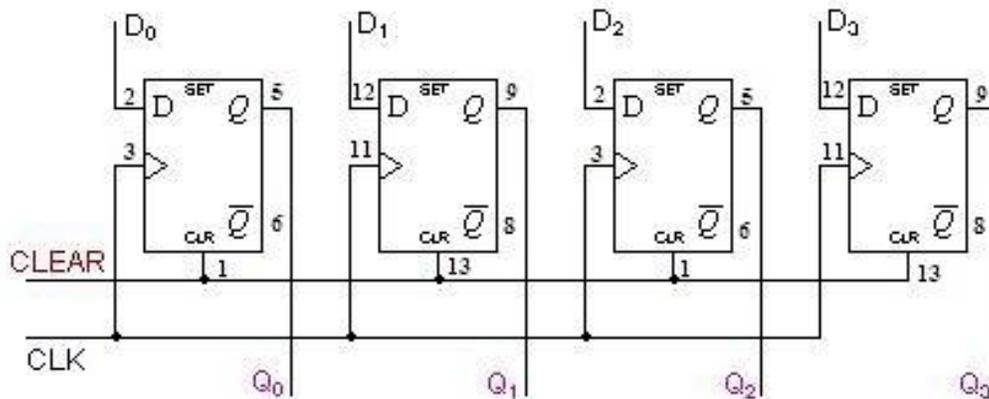
**SIPO:**



### Truth table

No of clk pulse	Serial input $D_{in}$	Parallel output			
		$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1
3	0	0	1	1	0
4	1	1	1	0	1
5	0	1	0	1	0
6	0	0	1	0	0
7	0	1	0	0	0
8	0	0	0	0	0

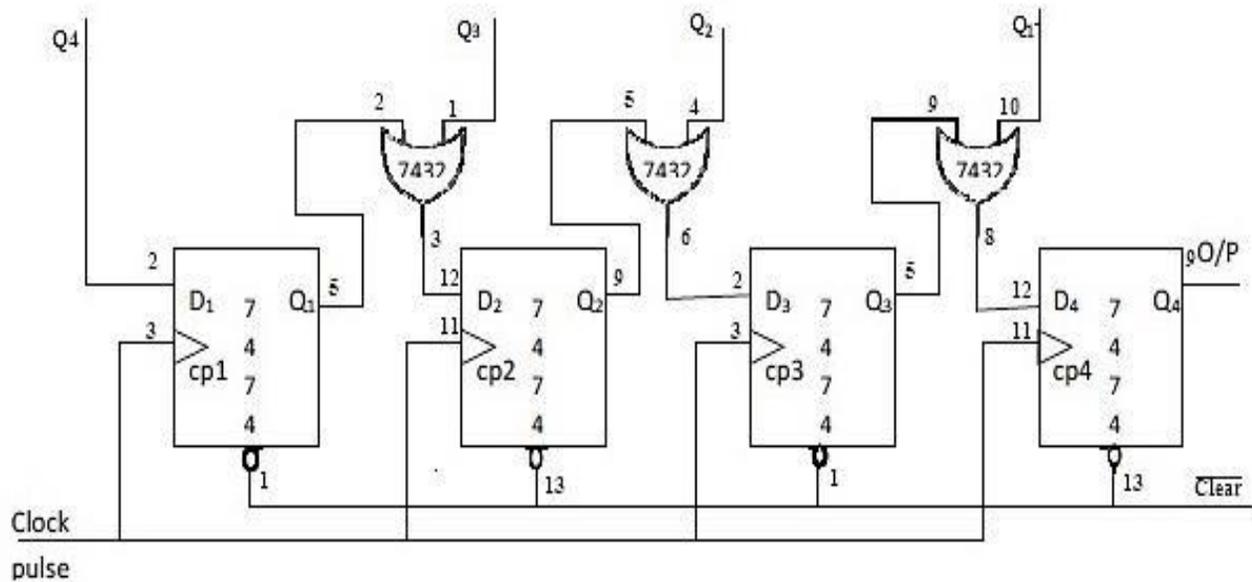
### PIPO



### Truth table

Clock	Parallel input				Parallel output			
	$D_0$	$D_1$	$D_2$	$D_3$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1

## PISO



## Truth table

Clock	PARALLEL INPUT				OUTPUT
	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	
1	1	0	0	1	1
2	X	X	X	X	0
3	X	X	X	X	0
4	X	X	X	X	1

## DISCUSSION QUESTIONS:

1. What is register?
2. What are the modes of shift register?
3. How ring counter is implemented using shift registers?
4. Compare parallel and serial sub registers?
5. Define sequence generator?
6. What are the types of shift register?
7. Define shift registers.

## RESULT:

Thus the SISO, SIPO, PISO, PIPO shift registers were designed and implemented.

Ex. No:

Date:

COUNTER

## DESIGN AND IMPLEMENTATION OF ASYNCHRONOUS

AIM:

To implement and verify the truth table of an asynchronous decade counter.

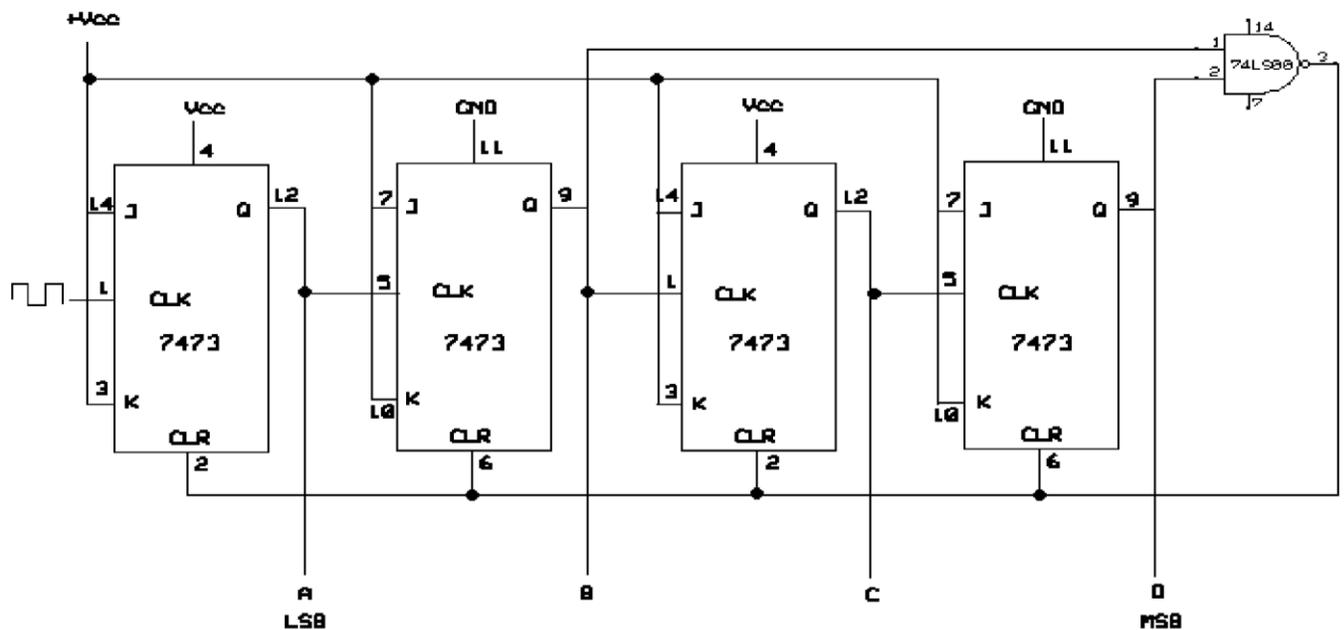
APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC 7473	2
4.	NAND gate	IC 7400	1
5.	Connecting wires		As required

THEORY:

Asynchronous decade counter is also called as ripple counter. In a ripple counter the flip flop output transition serves as a source for triggering other flip flops. In other words the clock pulse inputs of all the flip flops are triggered not by the incoming pulses but rather by the transition that occurs in other flip flops. The term asynchronous refers to the events that do not occur at the same time. With respect to the counter operation, asynchronous means that the flip flop within the counter are not made to change states at exactly the same time, they do not because the clock pulses are not connected directly to the clock input of each flip flop in the counter.

CIRCUIT DIAGRAM:



**TRUTH TABLE:**

S.No	CLOCK PULSE	OUTPUT			
		D(MSB)	C	B	A(LSB)
1	0	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	0	1
11	10	0	0	0	0

**PROCEDURE:**

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter.

**RESULT:**

Thus an asynchronous decade counter was implemented and verified



Ex. No: **DESIGN AND IMPLEMENTATION OF SYNCHRONOUS COUNTER**

Date:

**AIM:**

To design and implement 4-bit synchronous BCD counter.

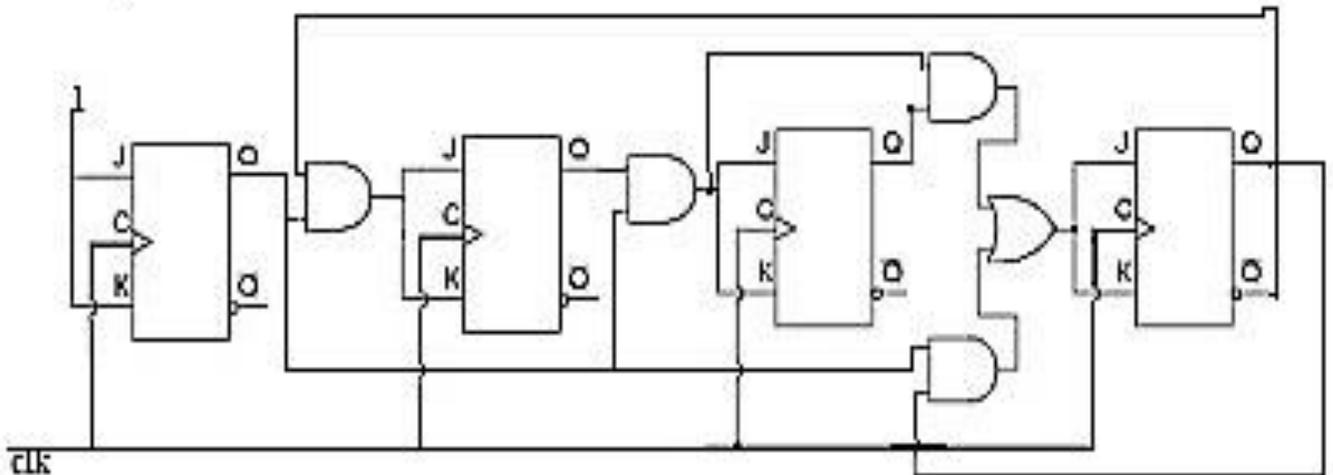
**APPARATUS REQUIRED:**

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC 7473	2
3.	AND gate	IC 7408	2
4.	OR gate	IC 7432	1
5.	Connecting wires		As required

**THEORY:**

A counter is a register capable of counting number of clock pulse arriving at the clock input. In synchronous counter all the flip-flops are clocked simultaneously. It is faster in speed because of the propagation delay of the single flip-flop is involved. It is also called as a parallel counter. A BCD synchronous counter can be called as a decade counter or mod-10 counter. It requires 4 flip flops ( $10 \leq 2^4$ ). So there are 16 possible states out of which 10 are valid and other 6 are invalid.

**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**

Present State				Next State				Excitation Required							
Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	J <sub>4</sub>	K <sub>4</sub>	J <sub>3</sub>	K <sub>3</sub>	J <sub>2</sub>	K <sub>2</sub>	J <sub>1</sub>	K <sub>1</sub>
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

**PROCEDURE:**

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter.

**DISCUSSION QUESTIONS:**

1. Compare synchronous and asynchronous sequential circuits?
2. What is a ripple counter?
3. What is propagation delay in ripple counter?
4. Define MOD counter?
5. What are the applications of counters?
6. State the types of counter?
7. Define bit, byte and word.
8. Define address of a memory.
9. What is a parallel counter?
10. What is the speed of a synchronous counter?

**Result:**

Thus the synchronous and asynchronous counter circuits were designed and the outputs were verified.

## APPLICATIONS OF OP-AMP (INVERTING AND NON – INVERTING AMPLIFIER)

### a. INVERTING AMPLIFIER

#### AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

#### APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	
7.	Connecting wires and probes	As required	

#### THEORY:

The input signal  $V_i$  is applied to the inverting input terminal through  $R_1$  and the non- inverting input terminal of the op-amp is grounded. The output voltage  $V_o$  is fed back to the inverting input terminal through the  $R_f - R_1$  network, where  $R_f$  is the feedback resistor. The output voltage is given as,

$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is  $180^\circ$  out of phase with the input signal.

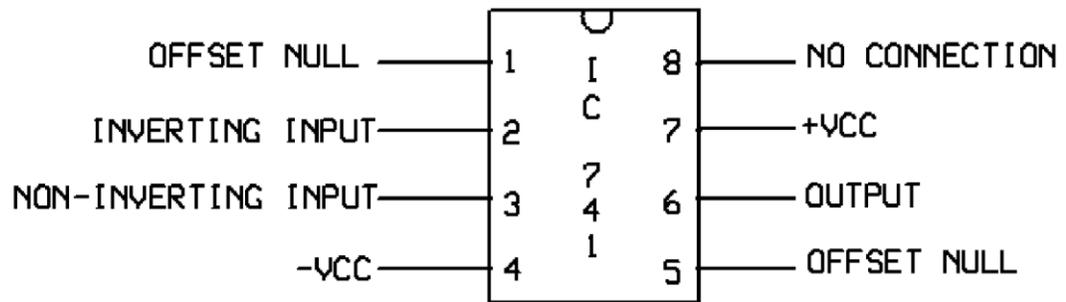
#### PRECAUTIONS:

1. Output voltage will be saturated if it exceeds  $\pm 15V$ .

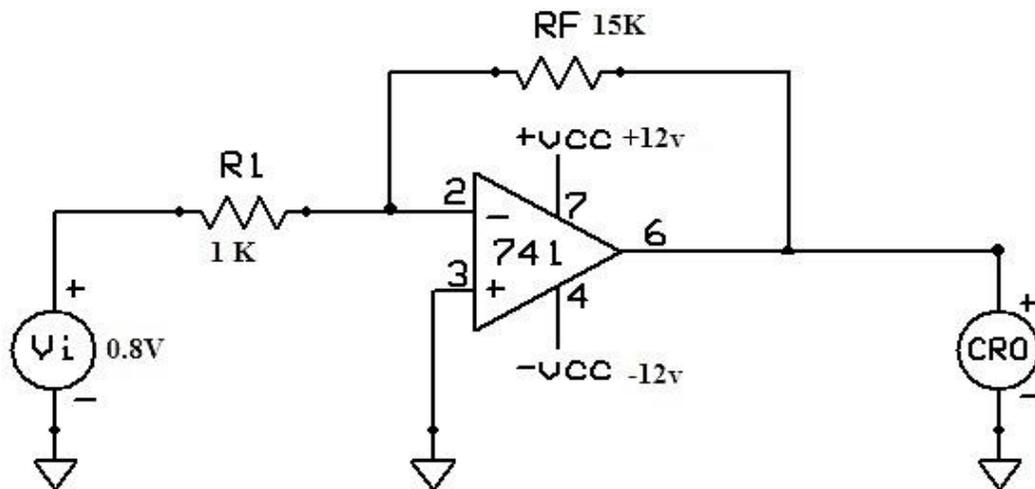
#### PROCEDURE:

1. Connections are given as per the circuit diagram.
2.  $+V_{cc}$  and  $-V_{cc}$  supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

#### PIN DIAGRAM:



**CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:**



**DESIGN:**

We know for an inverting Amplifier  $A_{CL} = R_f / R_1$

Assume  $R_1$  (approx.  $10\text{ K}\Omega$ ) and find  $R_f$

Hence  $V_o$  (theoretical) =  $- A_{CL} V_i$

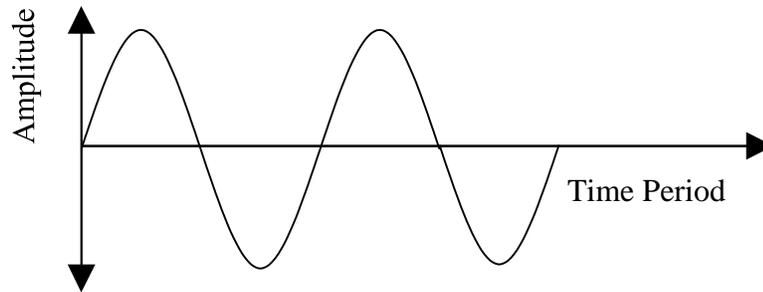
**OBSERVATIONS:**

S.No.	Amplitude ( No. of div x Volts per div )	Time period ( No. of div x Time per div )
Input		
Output	Theoretical -	
	Practical -	

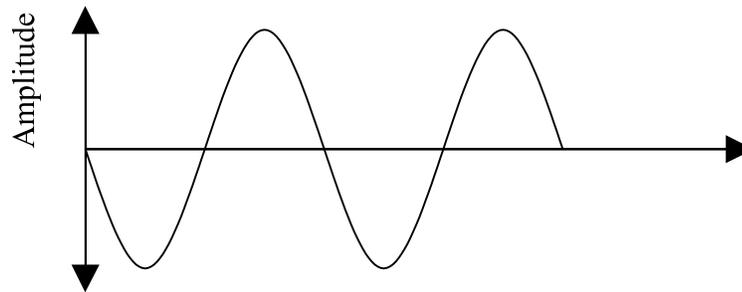
**MODEL GRAPH:**

## INVERTING AMPLIFIER:

### INPUT SIGNAL:



### OUTPUT SIGNAL:



### RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn.

## **b. NON - INVERTING AMPLIFIER**

### AIM:

To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

### APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors	As required	

7.	Connecting wires and probes	As required	
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**THEORY:**

The input signal  $V_i$  is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage  $V_d$  at the inverting input terminal of the opamp is zero ideally and the output voltage is given as,

$$V_o = A_{CL} V_i$$

Here the output voltage is in phase with the input signal.

**PRECAUTIONS:**

1. Output voltage will be saturated if it exceeds  $\pm 15V$ .

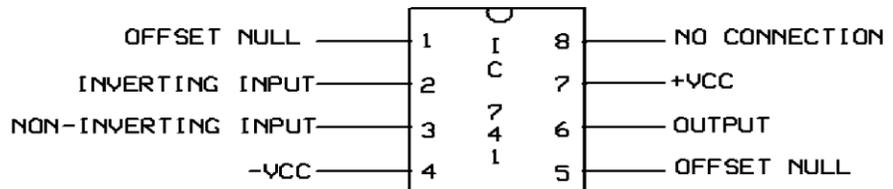
**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2.  $+V_{cc}$  and  $-V_{cc}$  supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

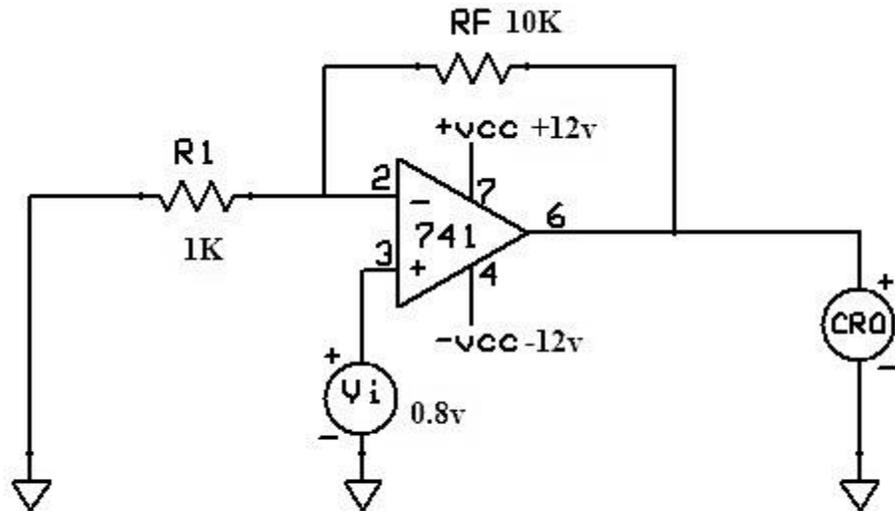
**DESIGN:**

We know for a Non-inverting Amplifier  $A_{CL} = 1 + (R_f / R_1)$  Assume  $R_1$  ( approx.  $10 K\Omega$  ) and find  $R_f$   
Hence  $V_o = A_{CL} V_i$

**PIN DIAGRAM:**



**CIRCUIT DIAGRAM OF NON INVERTING AMPLIFIER:**



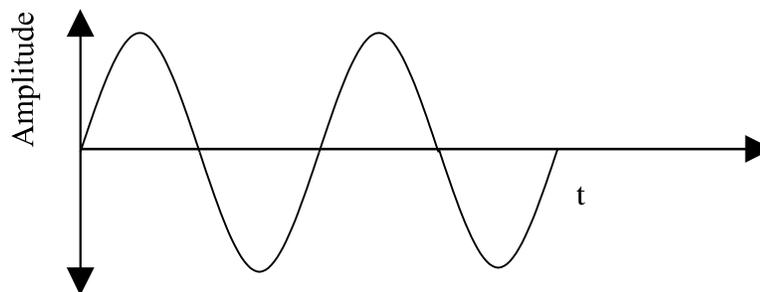
**OBSERVATIONS:**

S.No.	Amplitude (No. of div x Volts per div )	Time period (No. of div x Time per div )
Input		
Output	Theoretical -	
	Practical -	

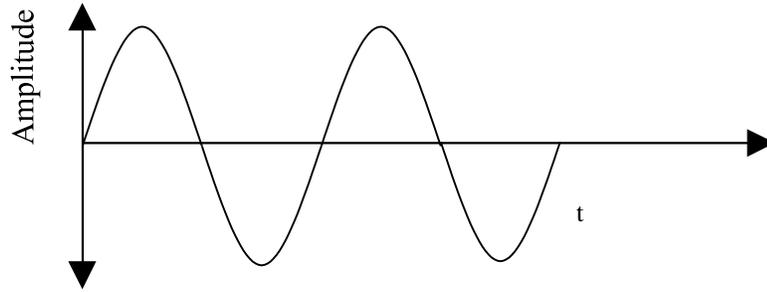
**MODEL GRAPH:**

NON- INVERTING AMPLIFIER:

**INPUT SIGNAL:**



## OUTPUT SIGNAL:



## DISCUSSION QUESTIONS:

1. What do you mean by linear circuits?
2. Define an IC?
3. What is an inverting amplifier?
4. What is the type of feedback employed in the inverting op-amp
5. What is a voltage follower?
6. Define a non-inverting amplifier?
7. Give the closed loop gain of an inverting amplifier?
8. What is the gain of a non-inverting amplifier?

## RESULT:

The design and testing of the Non-inverting amplifier is done and the input and output waveforms were drawn

Ex.No: **APPLICATION OF OP-AMP**

Date: **DESIGN OF ADDER, COMPARATOR, INTEGRATOR AND DIFFERENTIATOR**

**AIM:**

a) To study the applications of IC 741 as adder and comparator.

**APPARATUS:**

1. IC 741
2. Resistors (1K $\Omega$ )—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

**THEORY:**

**ADDER:**

Op-Amp may be used to design a circuit whose output is the sum of several input signals such as circuit is called a summing amplifier or summer. We can obtain either inverting or non inverting summer.

The circuit diagrams shows a two input inverting summing amplifier. It has two input voltages  $V_1$  and  $V_2$ , two input resistors  $R_1$ ,  $R_2$  and a feedback resistor  $R_f$ .

Assuming that op-amp is in ideal conditions and input bias current is assumed to be zero, there is no voltage drop across the resistor  $R_{comp}$  and hence the non inverting input terminal is at ground potential. By taking nodal equations.

$$V_1/R_1 + V_2/R_2 + V_0/R_f = 0$$

$$V_0 = - [(R_f/R_1) V_1 + (R_f/R_2) V_2] \text{ And here}$$

$$R_1 = R_2 = R_f = 1K$$

$$V_0 = -(V_1 + V_2)$$

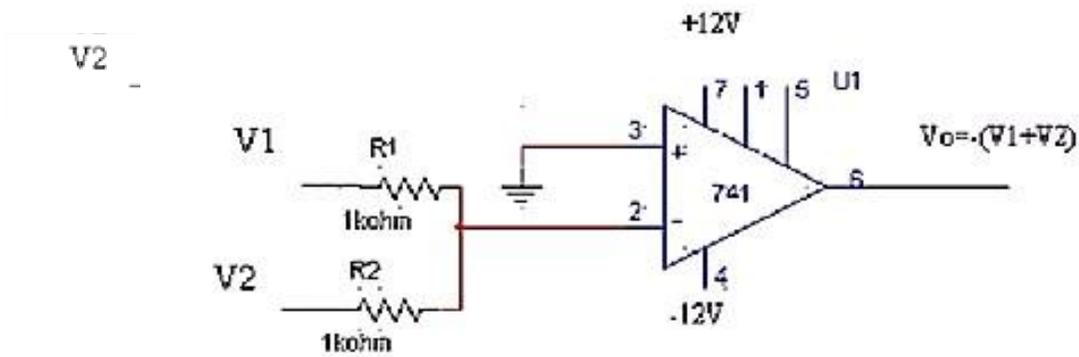
Thus output is inverted and sum of input.

**COMPARATOR:**

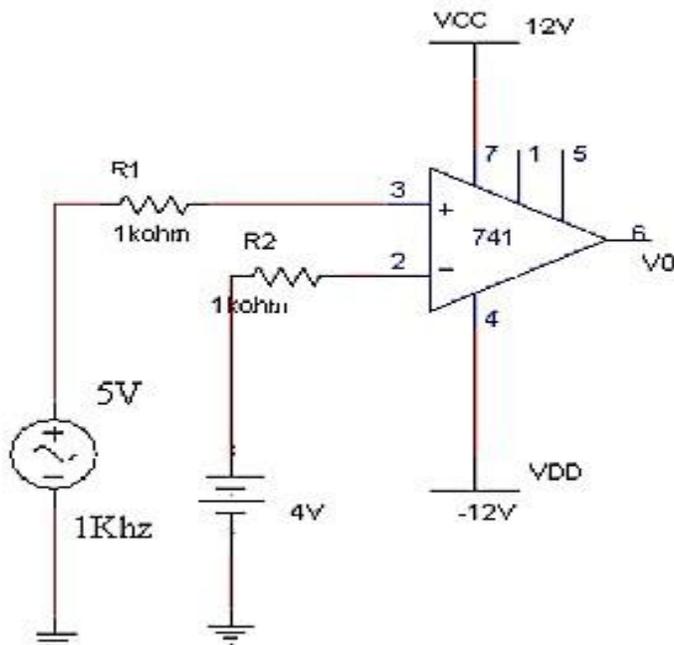
A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with output  $\pm V_{sat}$  as in the ideal transfer characteristics.

### CIRCUIT DIAGRAM:

Adder:



Comparator:



It is clear that the change in the output state takes place with an increment in input  $V_i$  of only 2mv. This is the uncertainty region where output cannot be directly defined There are basically 2 types of comparators.

1. Non inverting comparator and.
2. Inverting comparator.

The applications of comparator are zero crossing detector , window detector, time marker generator and phase meter.

### **PROCEDURE:**

#### **ADDER:**

1. connections are made as per the circuit diagram.
2. Apply input voltage 1)  $V_1= 5v, V_2=2v$   
2)  $V_1= 5v, V_2=5v$   
3)  $V_1= 5v, V_2=7v$ .
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of  $V_1$  and  $V_2$  measure the output voltage.

#### **COMPARATOR:**

1. Connections are made as per the circuit diagram.
2. Select the sine wave of 10V peak to peak , 1K Hz frequency.
3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to  $V_{ref}$ .
5. Repeat steps 3 and 4 with reference voltages as 2V, 4V, -2V, -4V and observe the waveforms.
6. Replace sine wave input with 5V dc voltage and  $V_{ref}= 0V$ .
7. Observe dc voltage at output using CRO.
- 8 . Slowly increase  $V_{ref}$  voltage and observe the change in saturation voltage.

#### **PRECAUTIONS:**

1. Make null adjustment before applying the input signal.
2. Maintain proper  $V_{cc}$  levels.

#### **RESULT:**

The design and testing of the adder and comparator is done.

Ex. No:

Date:

**APPLICATIONS OF OP-AMP – II**  
**(DIFFERENTIATOR AND INTEGRATOR)**

**2. a. DIFFERENTIATOR**

**AIM:**

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

**APPARATUS REQUIRED:**

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

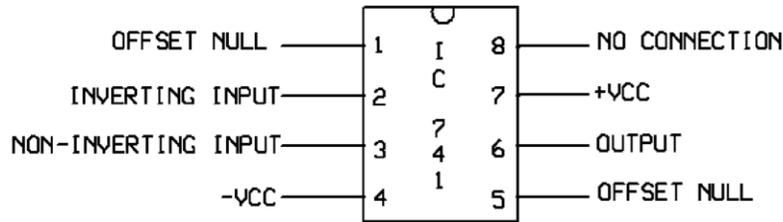
**THEORY:**

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor  $R_1$  is replaced by a capacitor  $C_1$ . The expression for the output voltage is given as,  $V_o = -R_f C_1 (dV_i/dt)$

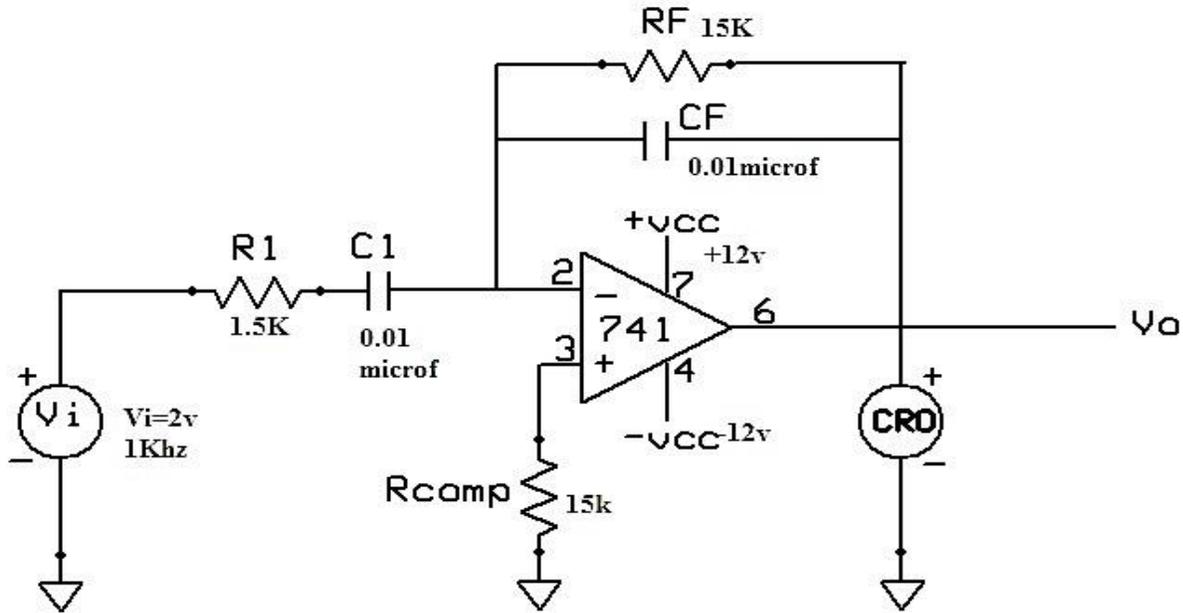
Here the negative sign indicates that the output voltage is  $180^\circ$  out of phase with the input signal. A resistor  $R_{comp} = R_f$  is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

1. Select  $f_a$  equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of  $C_1 < 1 \mu F$ , calculate the value of  $R_f$ .
2. Choose  $f_b = 20 f_a$  and calculate the values of  $R_1$  and  $C_f$  so that  $R_1 C_1 = R_f C_f$ .
3. The differentiator is most commonly used in waveshaping circuits to detect high frequency components in an input signal and also as a rate-of-change detector in FM modulators.

**PIN DIAGRAM:**



**CIRCUIT DIAGRAM OF DIFFERENTIATOR:**



**DESIGN:**

Given  $f_a = \dots\dots\dots$

We know the frequency at which the gain is 0 dB,  $f_a = 1 / (2\pi R_f C_1)$

Let us assume  $C_1 = 0.1 \mu\text{F}$ ; then

$R_f = \dots\dots\dots$

Since  $f_b = 20 f_a$ ,  $f_b = \dots\dots\dots$

We know that the gain limiting frequency  $f_b = 1 / (2\pi R_1 C_1)$

Hence  $R_1 = \dots\dots\dots$

Also since  $R_1 C_1 = R_f C_f$  ;  $C_f = \dots\dots\dots$

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. + V<sub>cc</sub> and - V<sub>cc</sub> supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

**OBSERVATIONS:**

Input - Sine wave

S.No.	Amplitude ( No. of div x Volts per div )	Time period ( No. of div x Time per div )
Input		
Output		

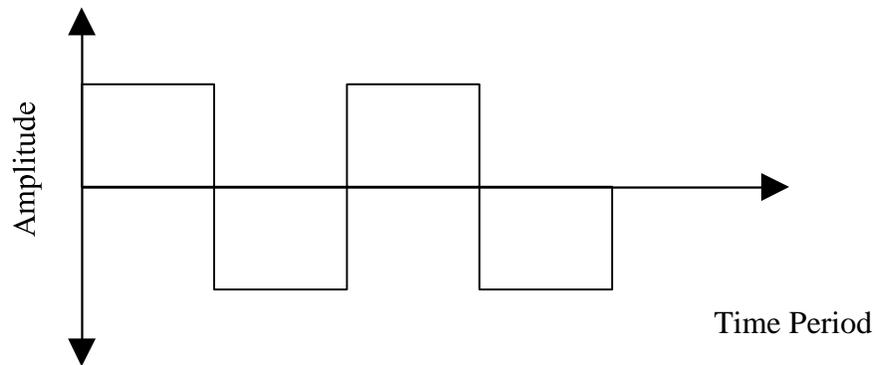
Input – Square wave

S.No.	Amplitude ( No. of div x Volts per div )	Time period ( No. of div x Time per div )
Input		
Output		

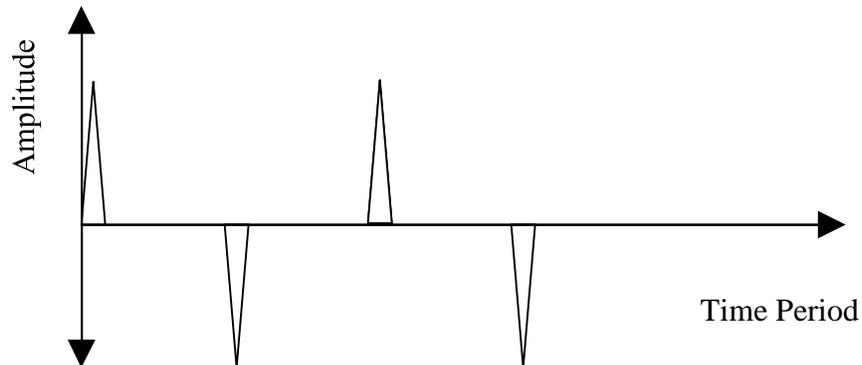
**MODEL GRAPH:**

DIFFERENTIATOR:

**INPUT SIGNAL:**



**OUTPUT SIGNAL:**



**RESULT:**

The design of the Differentiator circuit was done and the input and output waveforms were obtained.

## 2. b. INTEGRATOR

### AIM:

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

### APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

### THEORY:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor  $R_f$  is replaced by a capacitor  $C_f$ . The expression for the output voltage is given as,

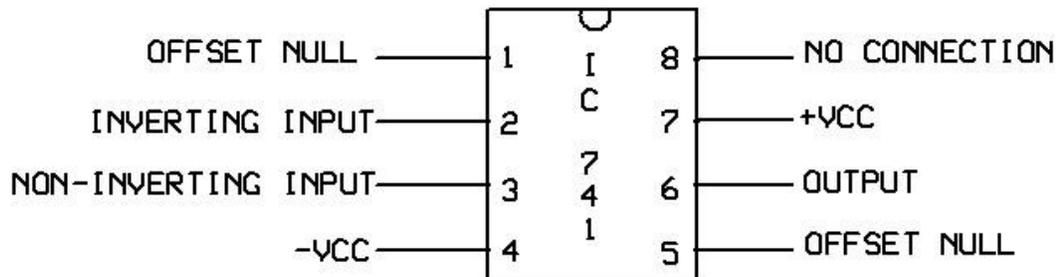
$$V_o = - (1/R_f C_f) \int V_i dt$$

Here the negative sign indicates that the output voltage is  $180^\circ$  out of phase with the input signal. Normally between  $f_a$  and  $f_b$  the circuit acts as an integrator. Generally, the value of  $f_a < f_b$ . The input signal will be integrated properly if the Time period  $T$  of the signal is larger than or equal to  $R_f C_f$ . That is,

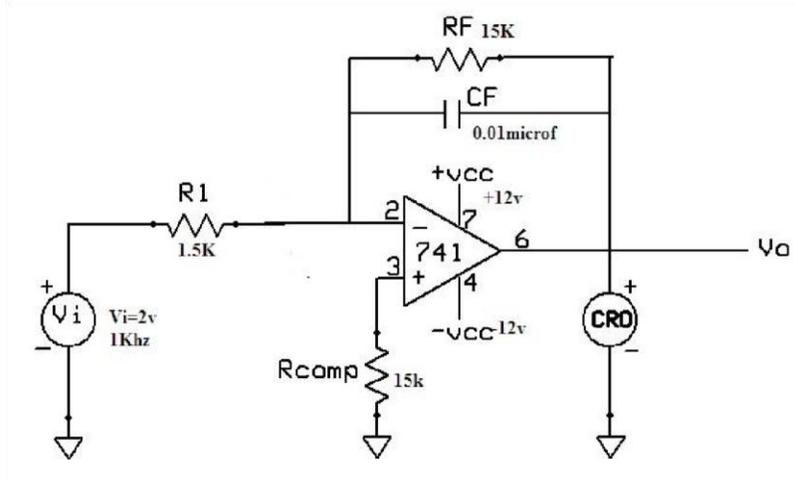
$$T \geq R_f C_f$$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

### PIN DIAGRAM:



**CIRCUIT DIAGRAM OF INTEGRATOR:**



**DESIGN:**

We know the frequency at which the gain is 0 dB,  $f_b = 1 / (2\pi R_1 C_f)$

Therefore  $f_b = \underline{\hspace{2cm}}$

Since  $f_b = 10 f_a$ , and also the gain limiting frequency  $f_a = 1 / (2\pi R_f C_f)$

We get,  $R_f = \underline{\hspace{2cm}}$  and hence  $R_1 = \underline{\hspace{2cm}}$

**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. + V<sub>cc</sub> and - V<sub>cc</sub> supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

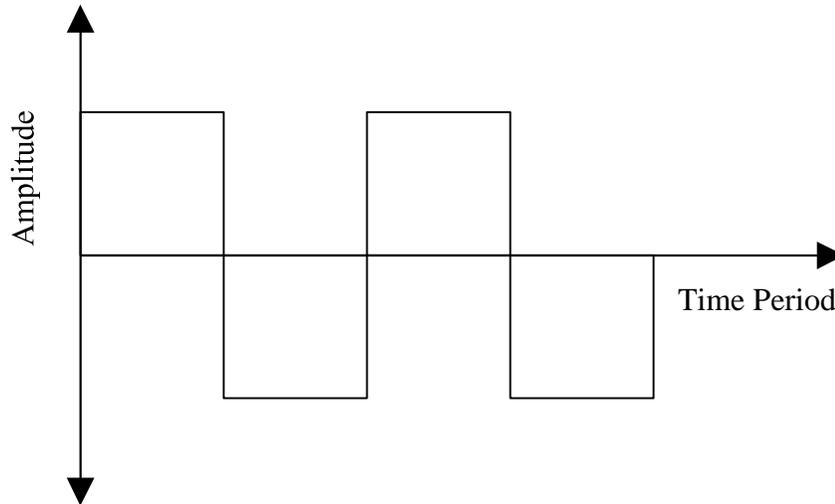
**OBSERVATIONS:**

S.No.	Amplitude ( No. of div x Volts per div )	Time period ( No. of div x Time per div )
Input		
Output		

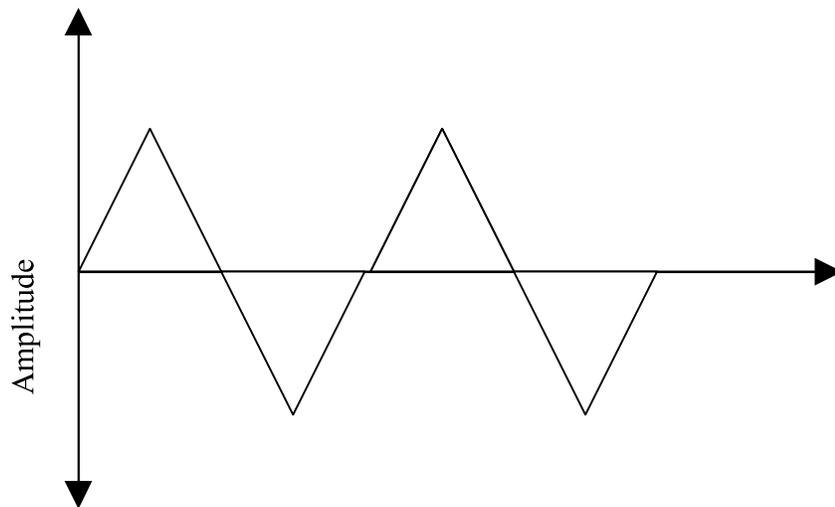
MODEL GRAPH:

INTEGRATOR:

**INPUT SIGNAL:**



**OUTPUT SIGNAL:**



**DISCUSSION QUESTIONS:**

1. What is integrator?
2. Write the disadvantages of ideal integrator?
3. Write the application of integrator?
4. Why compensation resistance is needed in integrator and how will you find its values?
5. What is differentiator?
6. Write the disadvantages of ideal differentiator.

7. Write the application of differentiator?
8. Why compensation resistance is needed in differentiator and how will you find its values?
9. Why integrators are preferred over differentiators in analog comparators?

**RESULT:**

The design of the Integrator circuit was done and the input and output waveforms were obtained.

Ex. No:

## TIMER IC APPLICATIONS - I

Date:

### (ASTABLE MULTIVIBRATOR)

#### AIM:

To design an astable multivibrator circuit for the given specifications using 555 Timer IC.

#### APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Timer IC	IC 555	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

#### THEORY:

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave- generating circuit. This circuit do not require an external trigger to change the state of the output. The time during which the output is either high or low is determined by two resistors and a capacitor, which are connected externally to the 555 timer. The time during which the capacitor charges from  $1/3 V_{cc}$  to  $2/3 V_{cc}$  is equal to the time the output is high and is given by,

$$t_c = 0.69 (R_1 + R_2) C$$

Similarly the time during which the capacitor discharges from  $2/3 V_{cc}$  to  $1/3 V_{cc}$  is equal to the time the output is low and is given by,

$$t_d = 0.69 (R_2) C$$

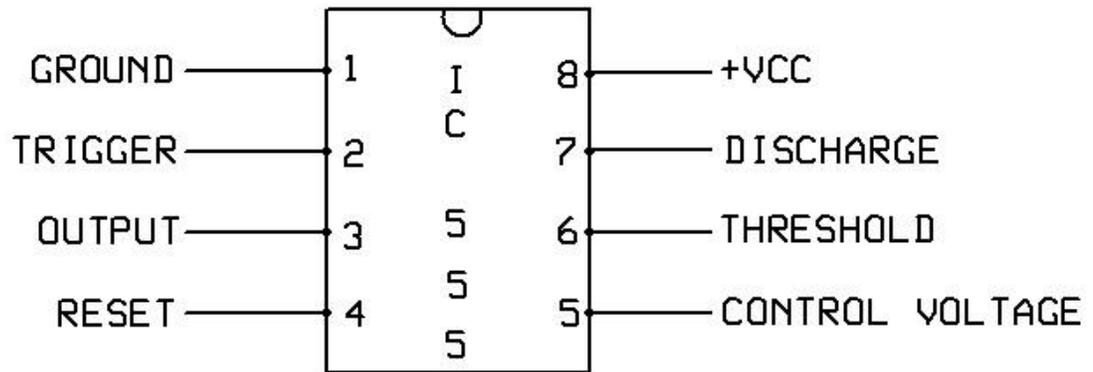
Thus the total time period of the output waveform is,

$$T = t_c + t_d = 0.69 (R_1 + 2 R_2) C$$

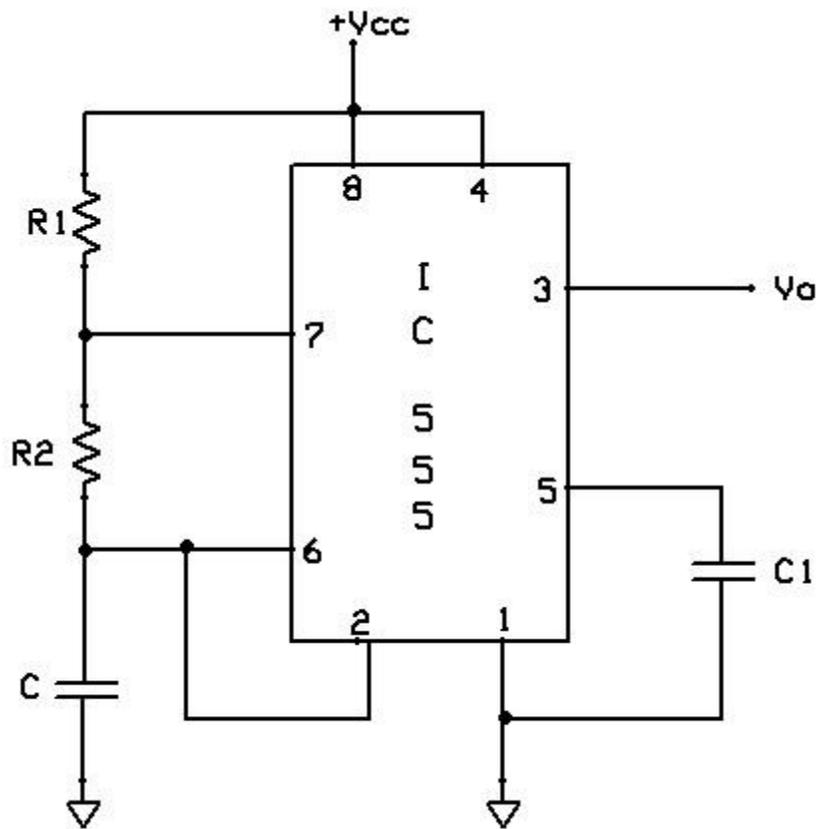
The term duty cycle is often used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time  $t_c$  during which the output is high to the total time period  $T$ . It is generally expressed in percentage. In equation form,

$$\% \text{ duty cycle} = [(R_1 + R_2) / (R_1 + 2 R_2)] \times 100$$

**PIN DIAGRAM:**



**CIRCUIT DIAGRAM OF ASTABLE MULTIVIBRATOR:**



**DESIGN:**

Given  $f = 4 \text{ KHz}$ ,

Therefore, Total time period,  $T = 1/f = \underline{\hspace{2cm}}$

We know, duty cycle =  $t_c / T$

Therefore,  $t_c = \underline{\hspace{2cm}}$

and  $t_d = \underline{\hspace{2cm}}$

We also know for an astable multivibrator  $t_d = 0.69 (R_2) C$

Therefore,  $R_2 = \underline{\hspace{2cm}}$

$t_c = 0.69 (R_1 + R_2) C$

Therefore,  $R_1 = \underline{\hspace{2cm}}$

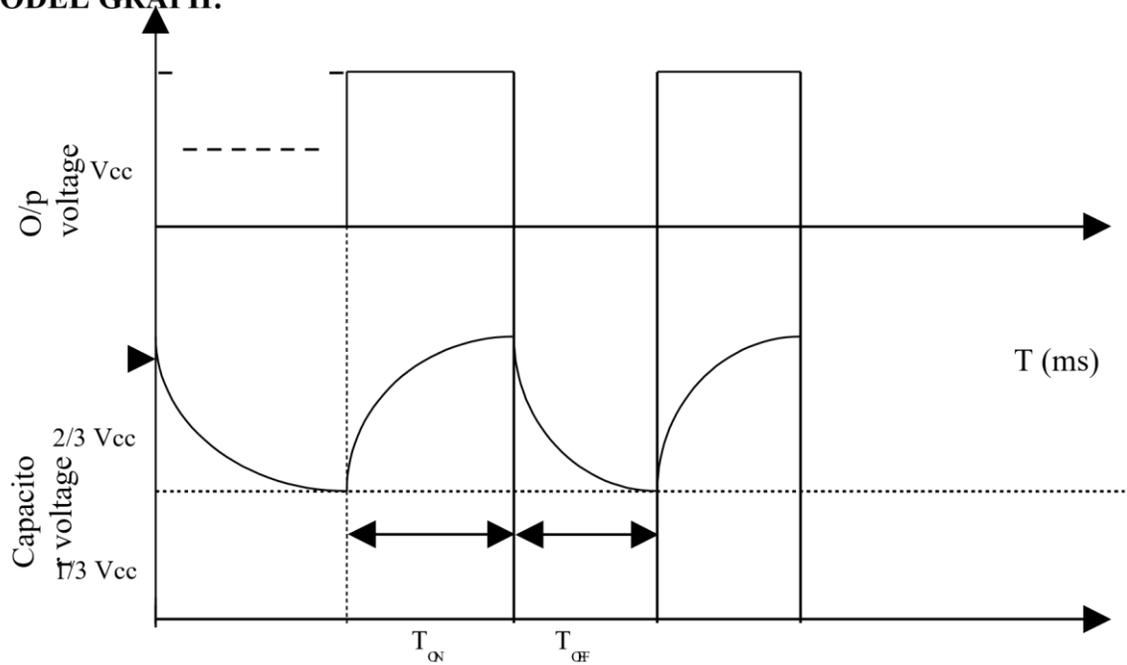
**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the +  $V_{cc}$  terminal of the timer IC.
3. At pin 3 the output waveform is observed with the help of a CRO
4. At pin 6 the capacitor voltage is obtained in the CRO and the  $V_o$  and  $V_c$  voltage waveforms are plotted in a graph sheet.

**OBSERVATIONS:**

S.No	Waveforms	Amplitude ( No. of div x Volts per div )	Time period ( No. of div x Time per div )	
			$t_c$	$t_d$
1.	Output Voltage , $V_o$			
2.	Capacitor voltage , $V_c$			

### MODEL GRAPH:



### DISCUSSION QUESTIONS:

1. Define Offset voltage.
2. Define duty cycle.
3. Mention the applications of IC555.
4. Give the methods for obtaining symmetrical square wave.
5. What is the other name for monostable multivibrator?
6. Explain the operation of IC555 in astable mode..
7. Why negative pulse is used as trigger?

### RESULT:

The design of the Astable multivibrator circuit was done and the output voltage and capacitor voltage waveforms were obtained.

Ex. No:  
Date:

## TIMER IC APPLICATIONS –II

### (MONOSTABLE MULTIVIBRATOR)

#### AIM:

To design a monostable multivibrator for the given specifications using 555 Timer IC.

#### APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz, Analog	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Timer IC	IC 555	1
5.	Bread Board		1
6.	Resistors		
7.	Capacitors		
8.	Connecting wires and probes	As required	

#### THEORY:

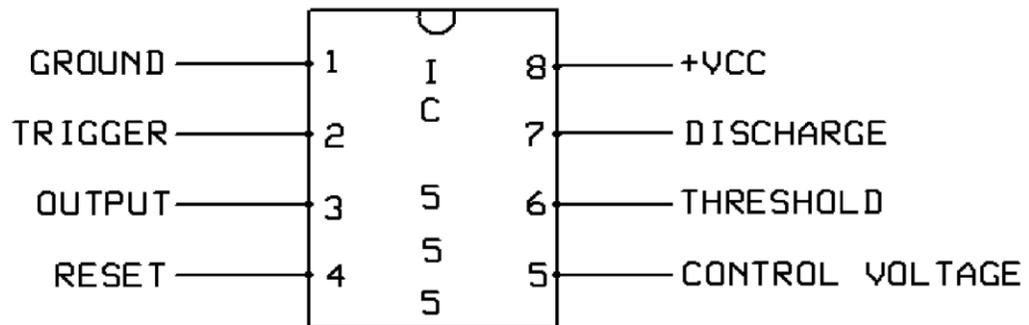
A monostable multivibrator often called a one-shot multivibrator is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand-by state the output of the circuit is approximately zero or at logic low level. When an external trigger pulse is applied, the output is forced to go high (approx.  $V_{cc}$ ). The time during which the output remains high is given by,

$$t_p = 1.1 R_1 C$$

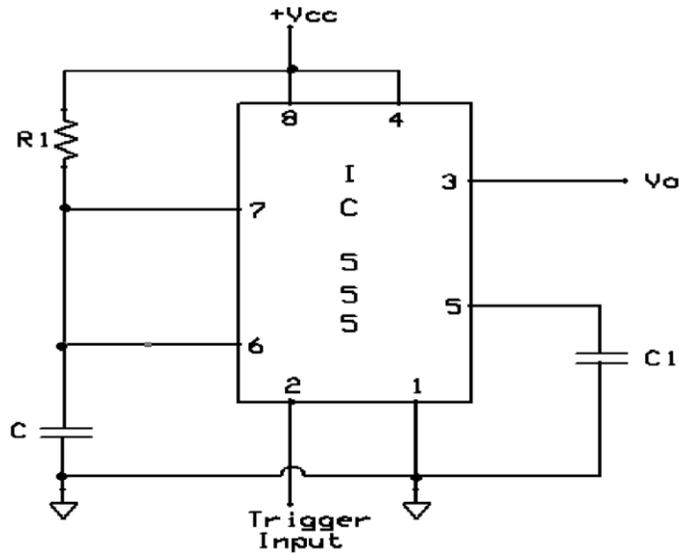
At the end of the timing interval, the output automatically reverts back to its logic low state. The output stays low until a trigger pulse is applied again. Then the cycle repeats.

Thus the monostable state has only one stable state hence the name monostable.

#### PIN DIAGRAM:



**CIRCUIT DIAGRAM OF MONOSTABLE MULTIVIBRATOR:**



**DESIGN:**

Given  $t_p = 0.616 \text{ ms} = 1.1 R_1 C$

Therefore,  $R_1 = \underline{\hspace{2cm}}$

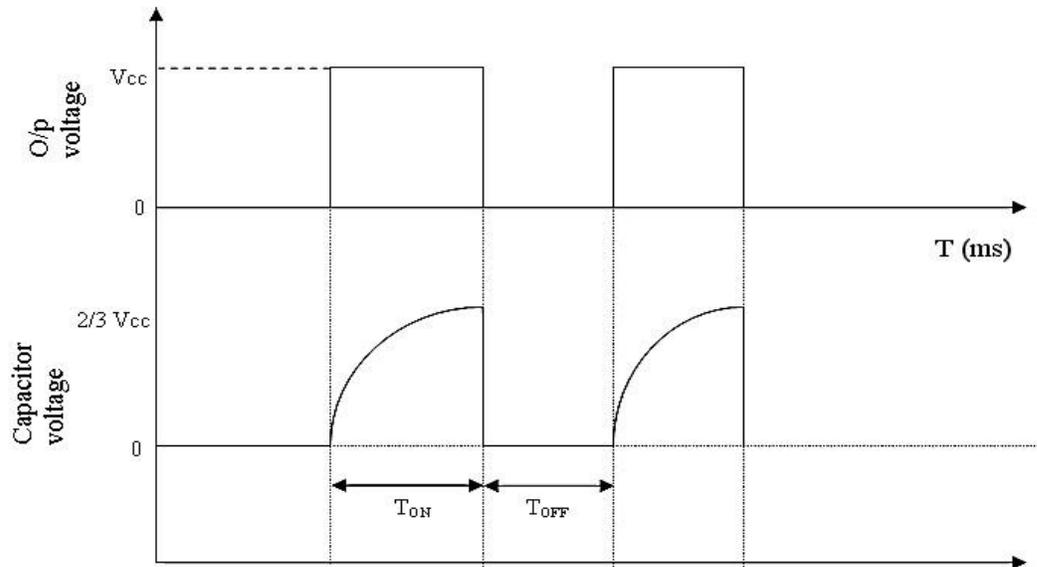
**PROCEDURE:**

1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the +  $V_{cc}$  terminal of the timer IC.
3. A negative trigger pulse of 5V, 2 KHZ is applied to pin 2 of the 555 IC
4. At pin 3 the output waveform is observed with the help of a CRO
5. At pin 6 the capacitor voltage is obtained in the CRO and the  $V_o$  and  $V_c$  voltage waveforms are plotted in a graph sheet.

**OBSERVATIONS:**

S.No		Amplitude ( No. of div x Volts per div )	Time period ( No. of div x Time per div )	
			$t_{on}$	$t_{off}$
1.	Trigger input			
2.	Output Voltage , $V_o$			
3.	Capacitor voltage , $V_c$			

## MODEL GRAPH



## DISCUSSION QUESTIONS:

1. Explain the operation of IC555 in monostable mode.
2. What is the charging time for capacitor in monostable mode?
3. What are the modes of operation of 555 timers?
4. Give the comparison between combinational circuits and sequential circuits.
5. What do you mean by present state?
6. Give the applications of 555 timers IC.

## RESULT:

The design of the Monostable multivibrator circuit was done and the input and output waveforms were obtained.

.Ex. No: Date:

Ex. No:

Date:

## DC POWER SUPPLY USING LM 317 AND LM 723

### AIM:

To design and test the DC power supply using LM723 and LM317.

### APPARATUS REQUIRED:

S. NO	NAME OF THE APPARATUS	SPECIFICATION	QUANTITY
1	LM317	-	1
2	LM723	-	1
3	Resistor	1.4K, 1K,,1.6K	1
4	Resistor	10K	2
5	Capacitor	0.1 $\mu$ F,100pF,330 $\mu$ F,22 $\mu$ F	1
6	DRB	-	1
7	CRO	-	1
8	Bread board	-	-

### PROCEDURE

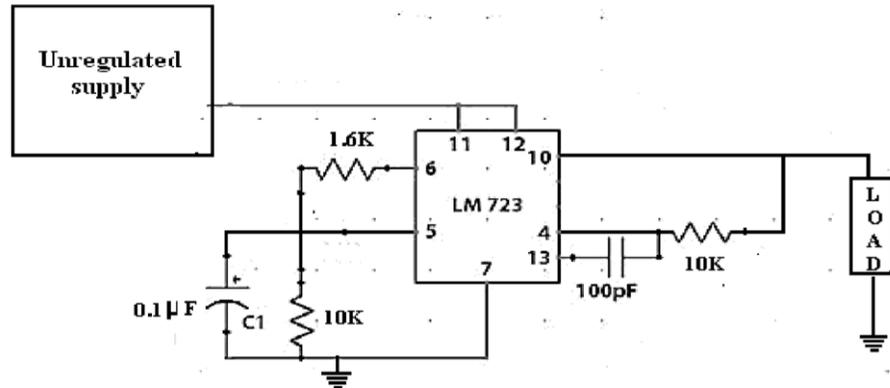
#### ELM723:

- i) Connections are made as per the circuit diagram ii) Set up the input voltage as 5V,6V and 10V
- iii) Vary the resistance  $R_2$  (designing value) the corresponding output voltage are noted down.
- iv) Plot the graph between resistance  $R_2$  and the observed output voltage

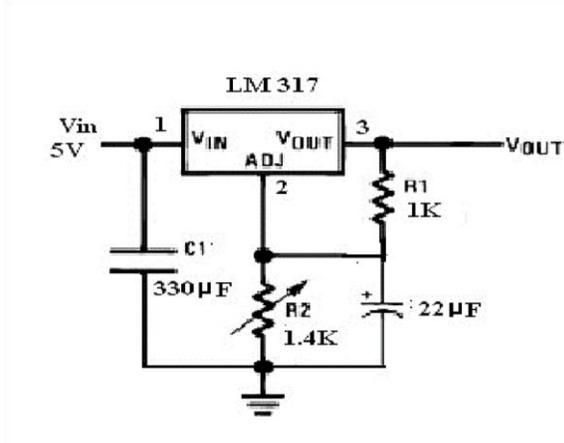
#### LM 317:

- i) Connections are made as per the circuit diagram
- ii) To vary the unregulated power supply from (0-3V) and note down the corresponding output voltage at across the load resistance  $R_L$ (pin no:10)
- iii) Plot the graph between resistance  $V_{in}$  and  $V_o$

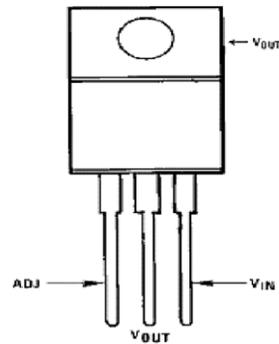
**CIRCUITDIAGRAM LM723:**



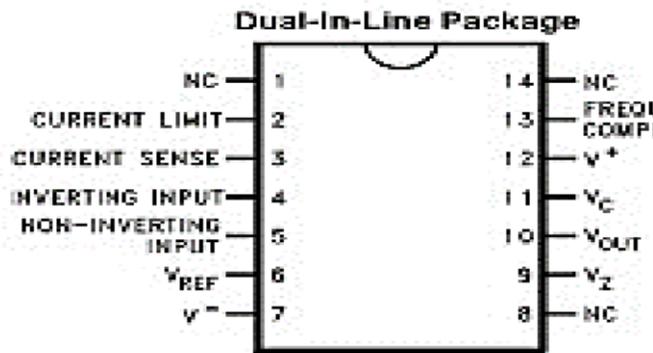
**LM317:**



**LM317:**



**LM723:**



**TABULATION:**

**LM723:**

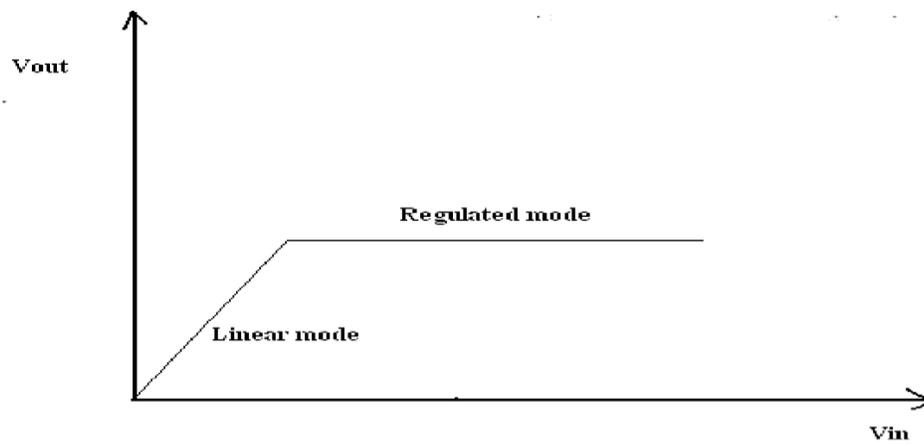
$V_{in}$ :

Resistance in ohms	Output voltage $V_o$

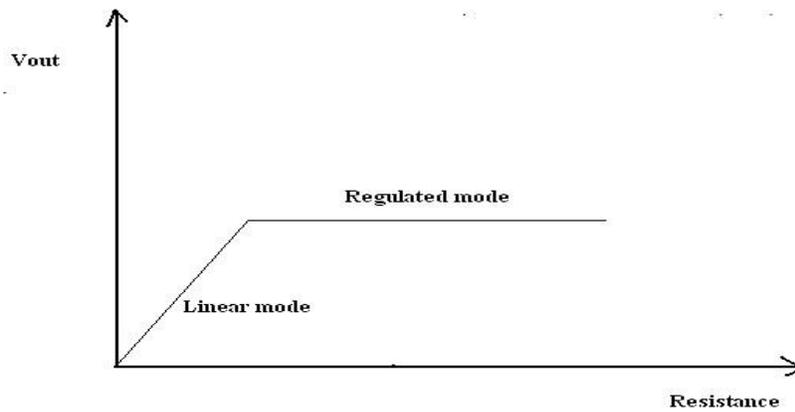
**LM317:**

$V_{in}$	$V_{out}$

**MODEL GRAPH:  
LM723:**



**LM317:**



**DISCUSSION QUESTIONS:**

1. What are the main advantages of voltage regulator?
2. Define line regulator or source regulator/
3. How is the IC 723 protected from short circuit?
4. Define ripple rejection with respect to the voltage regulator?
5. What is meant by drop out voltage?

**RESULT:**

To design and test the DC power supply using LM723 and LM317 was done and wave forms were obtained.