SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VI SEMESTER

PEC103 ANALOG IC DESIGN

Regulation – 2023

Academic Year 2025–2026 (EVEN SEM)

Prepared by

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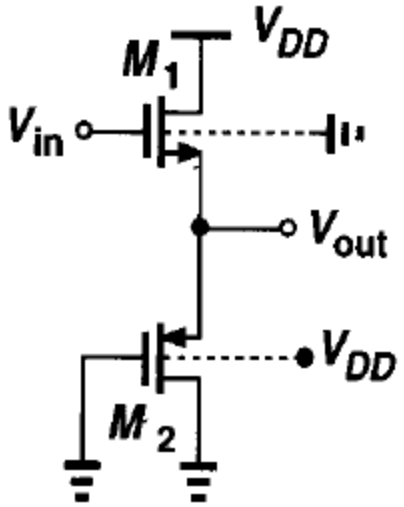
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

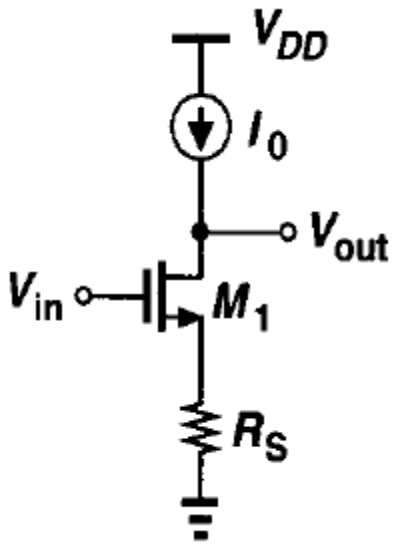
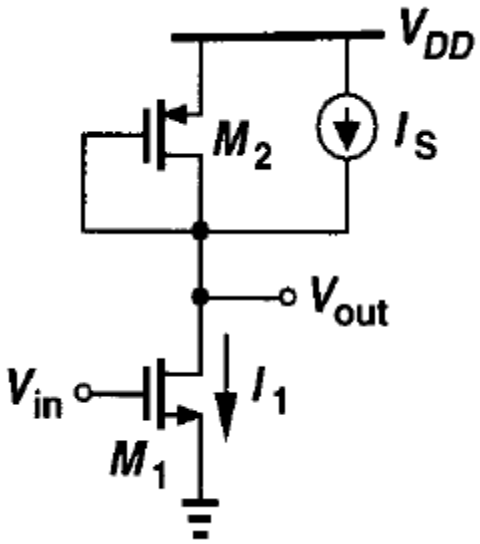
QUESTION BANK – PEC103 Analog IC Design

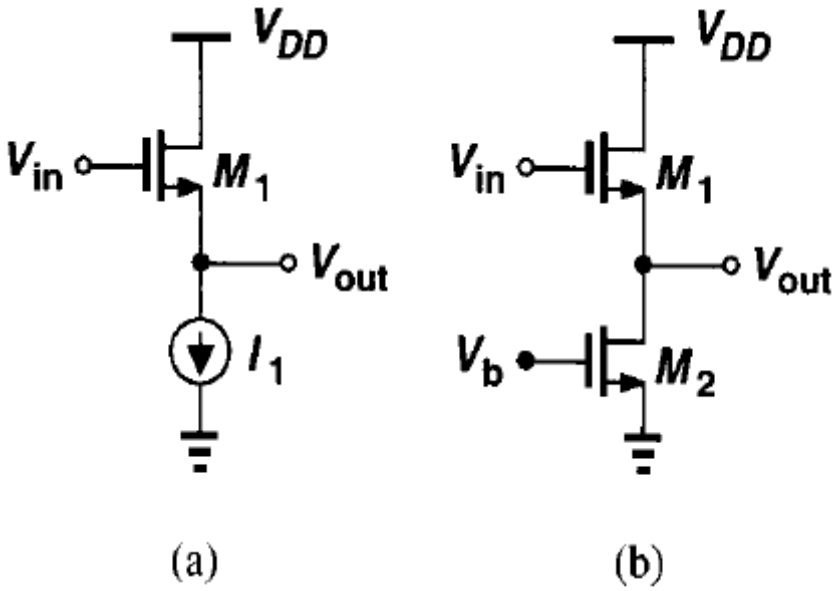
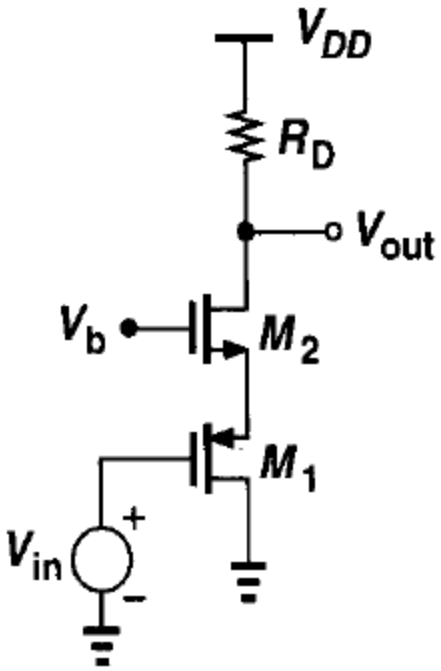
UNIT I – AMPLIFIERS

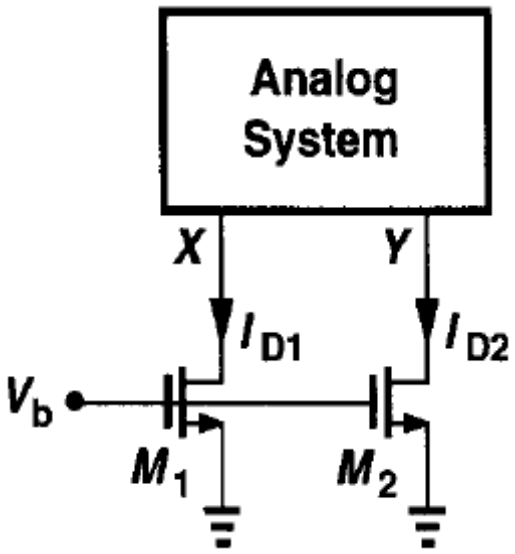
Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

PART – A

Q.No	Questions	CO	BT Level	Competence
1.	Sketch the analog design Octagon.	CO1	BTL1	**Remember**
2.	Define Single Stage Amplifier.	CO1	BTL1	**Remember**
3.	Draw the VI Characteristics of nMOSFET.	CO1	BTL1	**Remember**
4.	What is Pinch-off in MOSFET?	CO1	BTL1	**Remember**
5.	Compare long channel and short channel devices	CO1	BTL1	**Remember**
6.	Draw the small signal model of a MOSFET	CO1	BTL1	**Remember**
7.	Mention the steps involved in Small Signal Analysis of MOSFET	CO1	BTL2	**Understand**
8.	List the properties of Common Source Amplifier.	CO1	BTL2	**Understand**
9.	What is Current Mirror Load?	CO1	BTL2	**Understand**
10.	Define the Lee Load.	CO1	BTL2	**Understand**
11.	List any 4 types of loads used in amplifiers.	CO1	BTL2	**Understand**
12.	What do you mean by Cascode configuration?	CO1	BTL1	**Remember**
13.	Draw the equivalent circuit of Cascode amplifier.	CO1	BTL1	**Remember**
14.	Sketch the equivalent circuit diagram of folded cascode amplifier.	CO1	BTL1	**Remember**
15.	What is ICMR?	CO1	BTL1	**Remember**
16.	Define output offset Voltage	CO1	BTL1	**Remember**
17.	What is Shielding Property in Cascode amplifier?	CO1	BTL1	**Remember**
18.	Define Slew rate.	CO1	BTL2	**Understand**
19.	Define Noise in amplifiers	CO1	BTL2	**Understand**
20.	What is meant by Bandwidth with respect to amplifier response?	CO1	BTL1	**Remember**
21.	What do you mean by voltage swing?	CO1	BTL2	**Understand**
22.	Calculate the voltage gain of the circuit shown in figure below. 	CO1	BTL2	**Understand**
23.	Find the voltage gain of the circuit shown in Figure below. Assume I_0 as ideal.	CO1	BTL1	**Remember**

				
24.	Explain why the Gilbert Cell can operate as an analog voltage multiplier?	CO1	BTL2	**Understand**
	PART – B			
1.	Explain the construction and working of MOS Transistor?	CO1	BTL3	**Apply**
2.	Discuss the second order effects of MOS transistor.	CO1	BTL3	**Apply**
3.	Analyze the small signal model of a Common source amplifier with resistive load	CO1	BTL4	**Analyze**
4.	Analyze the small signal model of a Common source amplifier with diode connected load.	CO1	BTL4	**Analyze**
5.	Analyze the small signal model of a Common source amplifier with Source degeneration.	CO1	BTL4	**Analyze**
6.	Perform the small signal analysis of Source follower.	CO1	BTL3	**Apply**
7.	Derive the Voltage gain of a Common Gate Stage with a current source load.	CO1	BTL3	**Apply**
8.	Explain Cascode and folded cascode configurations with necessary diagrams.	CO1	BTL4	**Analyze**
9.	In the circuit given below, M_1 is biased in saturation with a drain current equal to I_1. The current source $I_s = 0.75I_1$ is added to the circuit. How is Av modified in this case? 	CO1	BTL4	**Analyze**
10.	Suppose for the source follower, in Figure (a), $(W/L)_1 = 20/0.5$, $I_1 = 200\mu A$, $V_{TH0} = 0.6V$, $2\phi_F = 0.7V$, $\mu_n C_{ox} = 50\ \mu A/V^2$ and $\gamma = 0.4V^2$	CO1	BTL3	**Apply**

	(a) Calculate Vout for Vin = 1.2V (b) IF I_1 is implemented as M2 in Figure (b), find the minimum value of $(W/L)_2$ for which M2 remains saturated.  (a) (b)			
11.	Calculate the voltage gain of the circuit shown in Figure below if $\lambda \neq 0$ and $\gamma \neq 0$?  	CO1	BTL3	**Apply**
12.	Two identical NMOS transistors are used as constant current sources in a system as shown in Figure below. However due to internal circuitry of the system, Vx is higher than Vy by ΔV. (a) Calculate the resulting difference between I_{D1} and I_{D2} if $\lambda \neq 0$ (b) Add cascade devices to M1 and M2 and repeat part (a).	CO1	BTL3	**Apply**

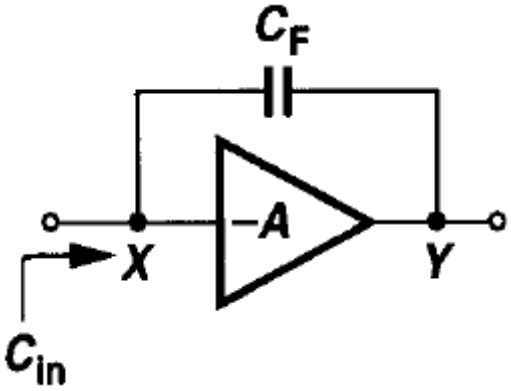
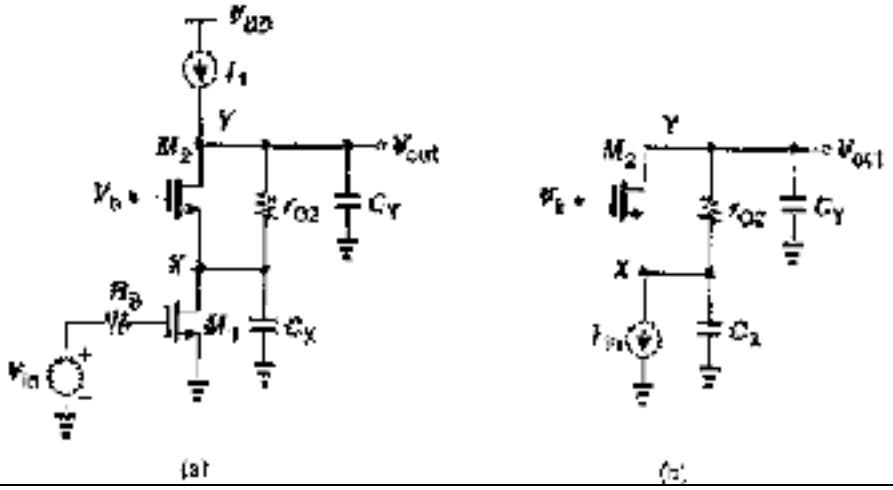
				
13.	Show that the output impedance of the folded cascode amplifier is lower than that of non folded circuit.	CO1	BTL3	**Apply**
14.	Perform Qualitative analysis of Differential pair with neat diagram	CO1	BTL4	**Analyze**
15.	With the supporting diagrams, Perform Quantitative analysis of Differential pair.	CO1	BTL4	**Analyze**
16.	Design a MOS differential amplifier with a current mirror load.	CO1	BTL4	**Analyze**
17.	Describe the Intuitive analysis of a differential amplifier.	CO1	BTL4	**Analyze**

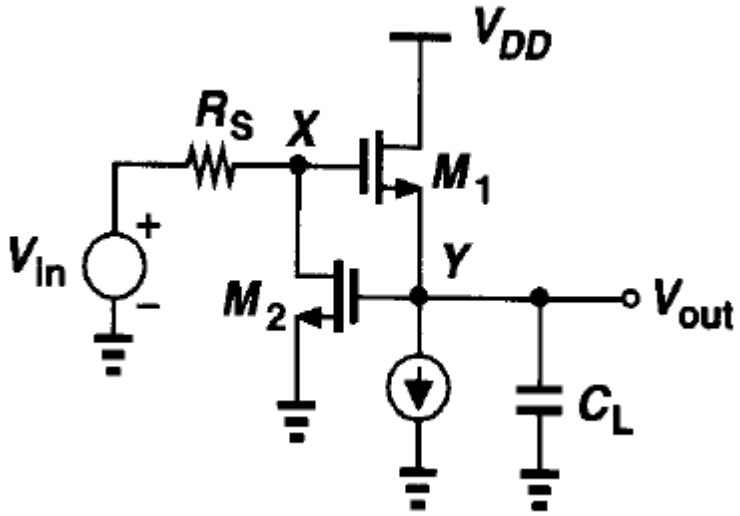
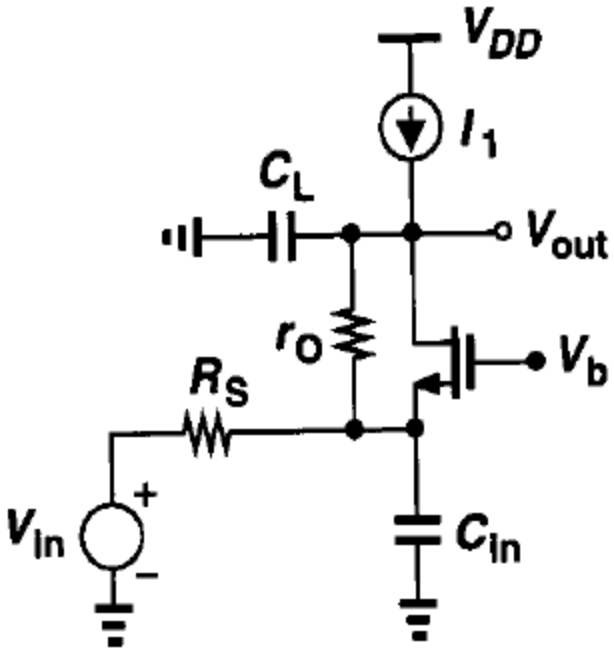
UNIT II – HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

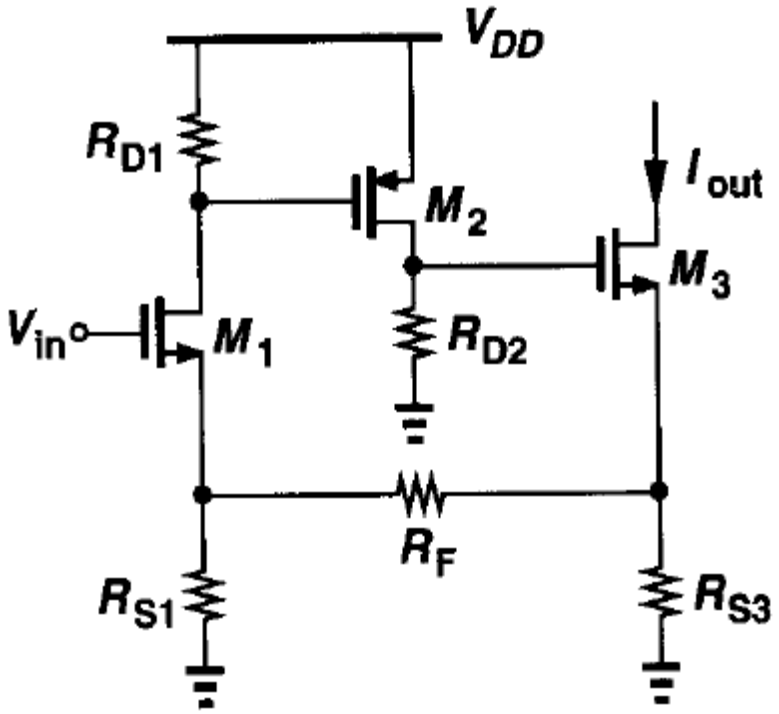
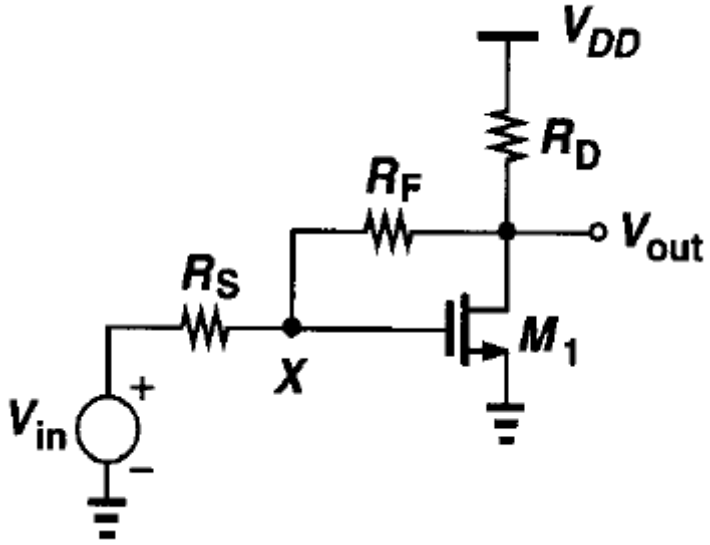
PART – A

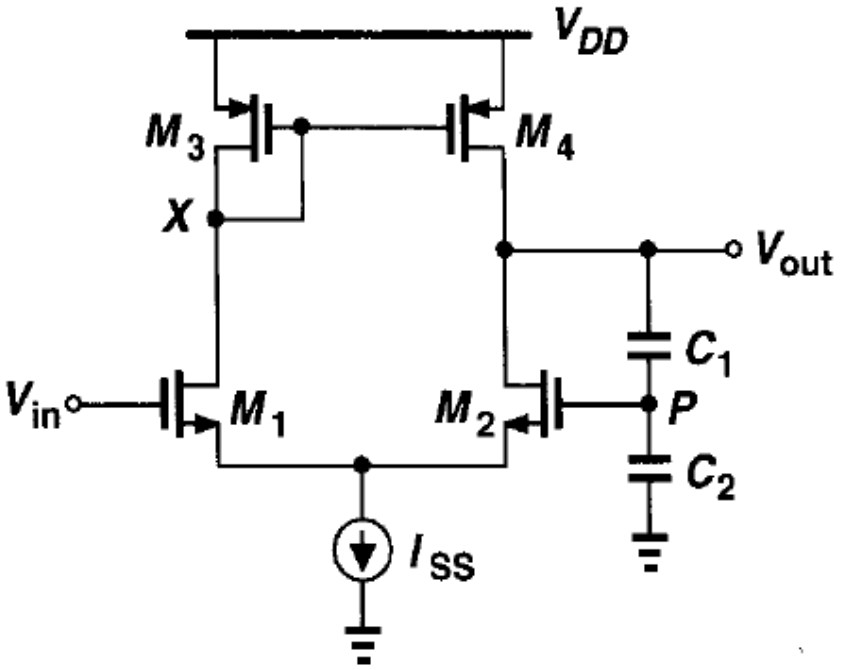
Q.No	Questions	CO	BT Level	Competence
1.	State Millers Theorem	CO2	BTL1	**Remember**
2.	Prove the statement of Millers Theorem	CO2	BTL1	**Remember**
3.	Write the transfer function of a cascade amplifiers by the association of poles with nodes.	CO2	BTL1	**Remember**
4.	Write the transfer function of common source stage amplifier.	CO2	BTL1	**Remember**
5.	Write the transfer function of source follower	CO2	BTL1	**Remember**
6.	Mention the input and the output impedance of source follower.	CO2	BTL1	**Remember**
7.	Write the transfer function of Common gate stage amplifier	CO2	BTL2	**Understand**
8.	Mention the pole frequency of common gate stage.	CO2	BTL2	**Understand**
9.	Write the input impedance of a cascade stage.	CO2	BTL2	**Understand**
10.	Draw the high frequency model of a cascade stage	CO2	BTL2	**Understand**
11.	Explain the lemma model.	CO2	BTL2	**Understand**
12.	Define the expression for noise bandwidth	CO2	BTL1	**Remember**
13.	Define power spectral density	CO2	BTL1	**Remember**
14.	What is meant by white noise spectrum?	CO2	BTL1	**Remember**
15.	Define the probability density function of x(t)	CO2	BTL1	**Remember**
16.	Define Gaussian PDF.	CO2	BTL1	**Remember**
17.	State the statistical characteristics of Noise.	CO2	BTL1	**Remember**
18.	How to quantify the effect of noise?	CO2	BTL2	**Understand**
19.	Name any 4 different noise in single stage amplifier	CO2	BTL2	**Understand**
20.	List any 2 different noise in differential amplifier	CO2	BTL1	**Remember**

21.	Draw the correlated and uncorrelated noise?	CO2	BTL2	**Understand**
22.	What is noise in single stage amplifier?	CO2	BTL2	**Understand**
23.	Explain noise bandwidth?	CO2	BTL1	**Remember**
24.	What is flicker noise?	CO2	BTL2	**Understand**
	PART – B			
1.	Prove the association of poles with nodes in cascode amplifiers.	CO2	BTL4	**Analyze**
2.	Consider the circuit shown in Figure below, where the voltage amplifier has a negative gain equal to – A and is otherwise ideal. Calculate the input capacitance of the circuit. 	CO2	BTL3	**Apply**
3.	Derive the transfer function of Common Source amplifier with necessary diagram	CO2	BTL3	**Apply**
4.	Explain the high frequency response of Common Source amplifier with Miller Capacitance	CO2	BTL4	**Analyze**
5.	Derive the transfer function of Source follower with necessary diagram	CO2	BTL4	**Analyze**
6.	Discuss the high frequency response of Source follower with Miller Capacitance	CO2	BTL3	**Apply**
7.	Apply the large signal analysis to a Common Gate amplifier to derive the governing transfer function?	CO2	BTL3	**Apply**
8.	With the help of high frequency model, discuss the frequency response of a Common gate amplifier.	CO2	BTL3	**Apply**
9.	Describe the high frequency model of a cascode amplifier.	CO2	BTL3	**Apply**
10.	For the cascode stage shown in Figure (a), neglect the capacitance associated with M1, representing Vin and M1 by Nortons equivalent as shown in Figure (b). Assume $\gamma = 0$. Calculate the transfer function. 	CO2	BTL3	**Apply**
11.	Explain the high frequency model of a differential pair with the help	CO2	BTL3	**Apply**

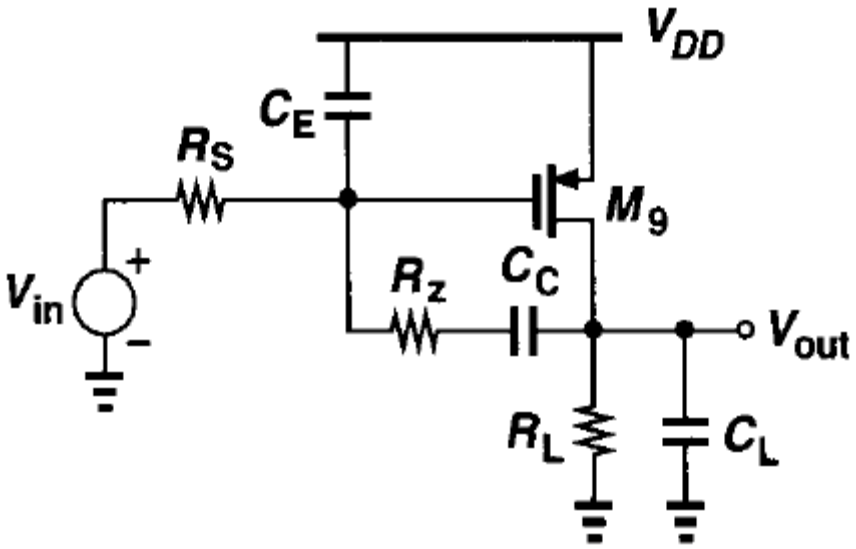
	of neat circuits.			
12.	Discuss the statistical characteristics of Noise.	CO2	BTL4	**Analyze**
13.	Write about Thermal noise and Flicker noise in detail.	CO2	BTL3	**Apply**
14.	Describe the noise in single stage amplifiers	CO2	BTL4	**Analyze**
15.	Write short notes on noise in differential pair.	CO2	BTL4	**Analyze**
16.	Calculate the transfer function of the following circuit. 	CO2	BTL4	**Analyze**
17.	For the common gate stage shown in Figure below, calculate the transfer function and the input impedance Zin. Explain why Zin becomes independent of C_L as this capacitance increases? 	CO2	BTL4	**Analyze**

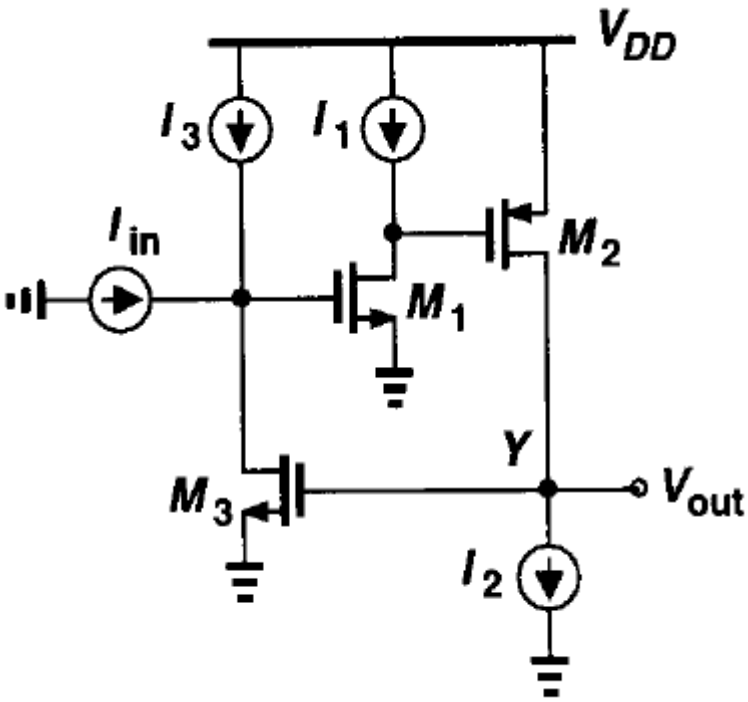
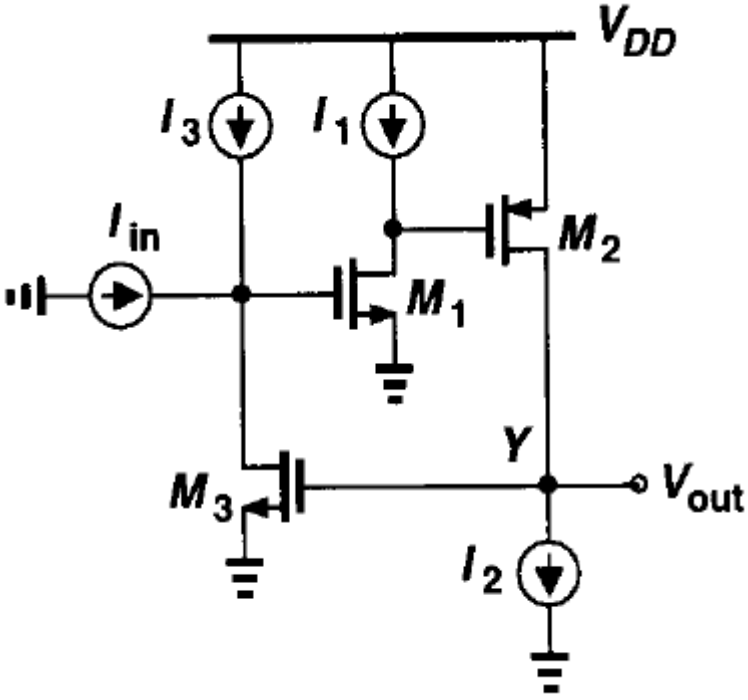
UNIT III – FEEDBACK AND OPERATIONAL AMPLIFIERS				
Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.				
PART – A				
Q.No	**Questions**	**CO**	**BT Level**	**Competence**
1.	What is Feedback amplifier?	CO3	BTL1	**Remember**
2.	Mention the types of feedback amplifiers?	CO3	BTL1	**Remember**
3.	List the advantages of feedback amplifiers?	CO3	BTL1	**Remember**
4.	Point out the disadvantages of feedback amplifiers?	CO3	BTL1	**Remember**
5.	What are the applications of feedback amplifiers?	CO3	BTL1	**Remember**
6.	What are the properties of negative feedback amplifier?	CO3	BTL1	**Remember**
7.	Name the four different feedback topology	CO3	BTL2	**Understand**
8.	Draw the current series feedback amplifier	CO3	BTL2	**Understand**
9.	Sketch the block diagram of Voltage series feedback amplifier	CO3	BTL2	**Understand**
10.	Draw the current shunt voltage feedback amplifier	CO3	BTL2	**Understand**
11.	Sketch the block diagram of current shunt voltage feedback amplifier.	CO3	BTL2	**Understand**
12.	What is the effect of loading in feedback networks?	CO3	BTL1	**Remember**
13.	How to classify the operational amplifiers?	CO3	BTL1	**Remember**
14.	List the key characteristics and parameters of operational amplifier	CO3	BTL1	**Remember**
15.	What is meant by open loop gain in opamp?	CO3	BTL1	**Remember**
16.	Define output impedance?	CO3	BTL1	**Remember**
17.	Compare Telescopic, Folded cascode, two stage and gain boosted amplifiers.	CO3	BTL1	**Remember**
18.	What is power supply rejection ratio?	CO3	BTL2	**Understand**
19.	State the objective of one stage opamp.	CO3	BTL2	**Understand**
20.	When do we go for two stage opamp instead of one stage?	CO3	BTL1	**Remember**
21.	What is the idea behind gain boosting?	CO3	BTL2	**Understand**
22.	Define Slew rate.	CO3	BTL2	**Understand**
23.	What is a buffer amplifier?	CO3	BTL1	**Remember**
24.	Draw the gain roll off with frequency.	CO3	BTL2	**Understand**
PART – B				
1.	Illustrate the general properties of feedback circuits.	CO3	BTL4	**Analyze**
2.	Describe the four types of amplifiers and discuss about the modifications for the improved performance of the same?	CO3	BTL3	**Apply**
3.	Brief about the four different feedback topologies with illustrative diagrams.	CO3	BTL3	**Apply**
4.	How do loading conditions influence the gain and impedance characteristics of a voltage–voltage feedback network?	CO3	BTL4	**Analyze**
5.	Examine the impact of loading on the performance parameters of a current–voltage feedback network.	CO3	BTL4	**Analyze**
6.	Analyze the effect of loading in Voltage – Current feedback network	CO3	BTL4	**Analyze**
7.	Explain how loading alters current gain stability and impedance behavior in a current–current feedback network.	CO3	BTL4	**Analyze**
8.	Determine the open loop and closed loop gain of the given circuit	CO3	BTL3	**Apply**

				
9.	Calculate the voltage gain of the circuit shown in Figure 	CO3	BTL3	**Apply**
10.	Discuss about the performance parameters of an op-amp?	CO3	BTL3	**Apply**
11.	Describe the one stage op-amp with necessary diagrams?	CO3	BTL3	**Apply**
12.	Explain the operation of two stage op-amp in detail.	CO3	BTL3	**Apply**
13.	Briefly explain about the power supply rejection?	CO3	BTL3	**Apply**
14.	Discuss about the slew rate of Op-amp in detail?	CO3	BTL3	**Apply**
15.	Calculate the low frequency PSRR of the feedback circuit shown in figure below.	CO3	BTL4	**Analyze**

				
16.	Explain how gain can be increased in op-amp?	CO3	BTL4	**Analyze**
17.	Analyze the effect of various noise that exist in op-amp?	CO3	BTL4	**Analyze**

UNIT IV – COMPENSATION TECHNIQUES				
Multipole Systems, Phase Margin, Frequency Compensation, Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.				
PART – A				
Q.No	**Questions**	**CO**	**BT Level**	**Competence**
1.	State Barkhausen Criteria.	CO4	BTL1	**Remember**
2.	What is frequency compensation?	CO4	BTL1	**Remember**
3.	What is a dominant pole?	CO4	BTL1	**Remember**
4.	List the methods of frequency compensation?	CO4	BTL1	**Remember**
5.	What is pole splitting?	CO4	BTL1	**Remember**
6.	What is Miller Compensation?	CO4	BTL1	**Remember**
7.	What are poles and Zeros?	CO4	BTL2	**Understand**
8.	What is a non-dominant pole?	CO4	BTL2	**Understand**
9.	Mention the need for compensation?	CO4	BTL2	**Understand**
10.	Write the poles of a Common gate Configuration	CO4	BTL2	**Understand**
11.	Construct the root locus of a one pole system.	CO4	BTL2	**Understand**
12.	Explain the multi pole systems in the context of operational amplifiers?	CO4	BTL1	**Remember**
13.	Define Phase Margin.	CO4	BTL1	**Remember**
14.	How frequency compensation is typically implemented in the two-stage op-amps?	CO4	BTL1	**Remember**
15.	What is the reason behind slewing in two-stage op-amps?	CO4	BTL1	**Remember**
16.	How much is the adequate value of Phase margin for a stable system?	CO4	BTL1	**Remember**
17.	Draw the effect of pole splitting in Miller compensation.	CO4	BTL1	**Remember**
18.	State the significance of the unity gain bandwidth product in op-amp design.	CO4	BTL2	**Understand**
19.	How do slew rate limitations affect the performance of op-amp?	CO4	BTL2	**Understand**
20.	Why a compensation capacitor is added in op-amp?	CO4	BTL1	**Remember**
21.	How can a phase margin be adjusted in a system?	CO4	BTL2	**Understand**
22.	Describe the significance of pole splitting in compensation?	CO4	BTL2	**Understand**

23.	Draw the simplified diagram of Two stage op-amp in positive slewing	CO4	BTL1	**Remember**
24.	Sketch the bode plot of a unstable system and a stable system?	CO4	BTL2	**Understand**
	PART – B			
1.	Construct the root locus for a two pole system.	CO4	BTL4	**Analyze**
2.	Describe the concept of frequency compensation with supporting diagrams?	CO4	BTL3	**Apply**
3.	Explain in detail about two stage op-amps with necessary diagrams?	CO4	BTL3	**Apply**
4.	Elaborate the frequency compensation in two stage op-amps?	CO4	BTL4	**Analyze**
5.	Discuss about the slewing in two stage op-amps?	CO4	BTL4	**Analyze**
6.	Describe the compensation technique using Common gate stage	CO4	BTL3	**Apply**
7.	How the source follower could be used in the frequency compensation technique. Discuss with circuit diagram.	CO4	BTL3	**Apply**
8.	Explain the compensation methods of a two stage op-amp?	CO4	BTL3	**Apply**
9.	Summarize in detail about slewing in two stage op-amp and alternating methods of compensating two stage with neat diagram.	CO4	BTL3	**Apply**
10.	Describe the design process of Miller Compensation in two stage op-amp?	CO4	BTL3	**Apply**
11.	Elaborate the design process of indirect frequency compensation techniques in op-amp?	CO4	BTL3	**Apply**
12.	An amplifier with a forward gain of A0 and two poles at 10Mhz and 500Mhz is placed in a unity-gain feedback loop. Calculate A0 for a phase margin of 60°.	CO4	BTL3	**Apply**
13.	An amplifier with a forward gain of A0 has two coincident poles at ω_p. Calculate the maximum value of A0 for a 60° phase margin with a closed loop gain of unity.	CO4	BTL4	**Analyze**
14.	An amplifier has a forward gain of A0 = 1000 and two poles at ω_{p1} and ω_{p2}. For ω_{p1}= 1 MHz, calculate the phase margin of a unity gain feedback loop if (a) ω_{p2}=2 ω_{p1} (b) ω_{p2}=4 ω_{p1}.	CO4	BTL4	**Analyze**
15.	Determine the Zero of the circuit shown below. 	CO4	BTL4	**Analyze**
16.	Determine the input referred noise current of the figure shown below.	CO4	BTL4	**Analyze**

				
17.	Explain why in the circuit shown below, the compensation capacitor should not be placed between the gate and drain of M2 or M3 	CO4	BTL4	**Analyze**

UNIT V – LOGIC CIRCUIT TESTING				
Faults in Logic Circuits- Basic Concepts of Fault Detection- Design for Testability-Ad Hoc Techniques, Level-Sensitive Scan Design, Partial Scan, Built-in Self-Test.				
PART – A				
Q.No	**Questions**	**CO**	**BT Level**	**Competence**
1.	What is failure in logic circuit?	CO5	BTL1	**Remember**
2.	Define Stuck at fault.	CO5	BTL1	**Remember**
3.	List any 4 types of faults.	CO5	BTL1	**Remember**
4.	What is fault detection?	CO5	BTL1	**Remember**
5.	State Observability.	CO5	BTL1	**Remember**
6.	State Controllability.	CO5	BTL1	**Remember**
7.	Expand ATPG.	CO5	BTL2	**Understand**
8.	What is Design for Testability?	CO5	BTL2	**Understand**
9.	What is Level Sensitive Scan Design?	CO5	BTL2	**Understand**
10.	Describe Partial Scan in fault detection?	CO5	BTL2	**Understand**
11.	Write the advantages of partial scan?	CO5	BTL2	**Understand**
12.	Mention the advantages of using BIST?	CO6	BTL1	**Remember**
13.	What is Built in Self Test (BIST)?	CO6	BTL1	**Remember**
14.	Write about Scan design?	CO6	BTL1	**Remember**
15.	Explain in short about Memory BIST?	CO6	BTL1	**Remember**
16.	How does scan design aid in fault detection?	CO6	BTL1	**Remember**
17.	What is the purpose of scan chain in fault detection?	CO6	BTL1	**Remember**
18.	How does LSSD improve fault detection in sequential circuit?	CO6	BTL2	**Understand**
19.	How does partial scan reduce test time?	CO6	BTL2	**Understand**
20.	Explain adhoc testing in fault detection?	CO6	BTL1	**Remember**
21.	Summarize the advantages of partial scan over full scan	CO6	BTL2	**Understand**
22.	List the primary objectives of BIST?	CO6	BTL2	**Understand**
23.	Illustrate a Stuck at 1 and stuck at 0 fault in two input AND gate.	CO6	BTL1	**Remember**
24.	List the advantages of scan path approach for sequential circuits.	CO6	BTL2	**Understand**
PART – B				
1.	Explain the different types of faults commonly encountered in logic circuits. Provide examples for each type.	CO5	BTL4	**Analyze**
2.	Explain the undetectable faults, Equivalent faults and temporary faults with examples.	CO5	BTL3	**Apply**
3.	Explain how multiplexers and tristate drivers are used to enhance testability	CO5	BTL3	**Apply**
4.	Discuss the principles and advantages of BIST in fault detection. Explain the architecture and operation of BIST?	CO5	BTL3	**Apply**
5.	Describe LSSD and its significance in fault detection and testing of sequential logic circuit.	CO5	BTL3	**Apply**
6.	Discuss the architecture and operation of LSSD.	CO5	BTL4	**Analyze**
7.	Explore the concept of Design for Testability (DFT) in digital circuit design. Discuss the key objectives and principles of DFT.	CO5	BTL3	**Apply**
8.	Discuss on random access scan techniques with neat sketch	CO5	BTL3	**Apply**
9.	Explain the block diagram of boundary scan architecture and its cell with the help of a neat sketch.	CO5	BTL4	**Analyze**
10.	Explain in detail for a faulty and fault free full adder circuit using suitable method.	CO6	BTL3	**Apply**
11.	Examine the concept of partial scan in fault detection and testing of	CO6	BTL3	**Apply**

	digital circuits.			
12.	Describe the basic concepts of Fault detection in logic circuits?	CO6	BTL3	**Apply**
13.	Discuss the adhoc techniques for DFT?	CO6	BTL4	**Analyze**
14.	Write the procedure to test a sequential circuit design using scan path technique?	CO6	BTL4	**Analyze**
15.	Discuss on Partial Scan technique in testing a logic circuit.	CO6	BTL4	**Analyze**
16.	Enumerate the test procedure of a sequential circuit with random access scan-in/scan-out feature along with tis merits.	CO6	BTL4	**Analyze**
17.	Describe the stuck at faults for a two input CMOS NOR gate	CO6	BTL4	**Analyze**