SRM VALLIAMMAI ENGINEERING COLLEGE

(An Autonomous Institution)

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

VI SEMESTER

PEC104 – Low Power Design

Regulation – 2023

Academic Year 2025 – 26(Even Semester)

Prepared by

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SUBJECT : PEC104 – Low Power Design

SEM / YEAR: VI / III

UNIT I - FUNDAMENTALS OF LOW POWER CIRCUITS

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

PART - A

Q. No	Questions	CO	BTL	Competence
1.	Define low power circuit design.	CO1	BTL1	Remembering
2.	Illustrate how glitches contribute to additional power dissipation.	CO1	BTL2	Understanding
3.	Identify the major sources of power dissipation in CMOS circuits.	CO1	BTL1	Remembering
4.	Summarize the influence of short channel effects on low power design.	CO1	BTL2	Understanding
5.	Name the different components of leakage power dissipation.	CO1	BTL1	Remembering
6.	Explain how switching activity influences power consumption.	CO1	BTL2	Understanding
7.	Compare dynamic power dissipation and short circuit power dissipation.	CO1	BTL2	Understanding
8.	State the need for low power circuit design in VLSI systems.	CO1	BTL1	Remembering
9.	Clarify the role of surface scattering on carrier mobility.	CO1	BTL2	Understanding
10.	Write the expression for switching power dissipation.	CO1	BTL1	Remembering
11.	Point out the punch through effect in short channel devices.	CO1	BTL1	Remembering
12.	Justify the importance of controlling leakage power in nanometer technologies.	CO1	BTL2	Understanding
13.	Interpret the impact of DIBL on threshold voltage variation.	CO1	BTL2	Understanding
14.	Examine the phenomenon of velocity saturation in MOS transistors.	CO1	BTL2	Understanding
15.	Mention the conditions under which short circuit power dissipation occurs.	CO1	BTL1	Remembering
16.	Classify power dissipation mechanisms in CMOS circuits.	CO1	BTL2	Understanding
17.	Describe why low power design is essential for portable electronics.	CO1	BTL2	Understanding
18.	Demonstrate how technology scaling increases leakage power.	CO1	BTL2	Understanding
19.	Calculate the switching power dissipation of a CMOS inverter given load capacitance, supply voltage, and operating frequency.	CO1	BTL2	Understanding
20.	Evaluate the change in switching power when clock frequency is doubled for a CMOS circuit.	CO1	BTL2	Understanding
21.	Determine the effect on dynamic power if the supply voltage is reduced by 20%.	CO1	BTL2	Understanding

22.	A CMOS inverter drives a load capacitance of 20 pF and operates at a clock frequency of 50 MHz with a supply voltage of 1.8 V. Assume activity factor α = 1. Calculate the switching power dissipation.		CO1	BTL2	Understanding
23.	A CMOS circuit operates at 1.2 V. If the supply voltage is reduced to 1.0 V, how does switching power change (all other parameters constant)?		CO1	BTL2	Understanding
24.	A CMOS circuit consumes 5 mW at 100 MHz. Estimate the power dissipation when the frequency is increased to 200 MHz.		CO1	BTL2	Understanding
PART – B					
1.	Analyze the relative contribution of switching, short circuit, and leakage power in deep submicron CMOS technologies.	(16)	CO1	BTL4	Analyzing
2.	Compute the switching power dissipation of a CMOS inverter for given load capacitance, supply voltage, and operating frequency.	(16)	CO1	BTL3	Applying
3.	Assess the impact of surface scattering and velocity saturation on MOSFET performance and power consumption.	(16)	CO1	BTL4	Analyzing
4.	Determine the variation in dynamic power dissipation when the supply voltage is scaled down.	(16)	CO1	BTL3	Applying
5.	Compare the sources of power dissipation in CMOS circuits under technology scaling.	(16)	CO1	BTL4	Analyzing
6.	Solve a numerical problem to estimate short circuit power dissipation during input transitions in a CMOS gate.	(16)	CO1	BTL3	Applying
7.	Investigate the effect of Drain Induced Barrier Lowering and punch through on off-state current.	(16)	CO1	BTL4	Analyzing
8.	Estimate the increase in leakage power due to threshold voltage reduction caused by DIBL.	(16)	CO1	BTL3	Applying
9.	Examine the influence of short channel effects on low power circuit design.	(16)	CO1	BTL4	Analyzing
10.	Calculate the total power dissipation of a CMOS circuit considering switching, short circuit, and leakage components.	(16)	CO1	BTL3	Applying
11.	Interpret the role of impact ionization in short channel devices and its effect on reliability.	(16)	CO1	BTL4	Analyzing
12.	Demonstrate the reduction in dynamic power achieved by minimizing glitches in a combinational circuit.	(16)	CO1	BTL3	Applying
13.	Differentiate the trade-offs between performance and power dissipation due to short channel effects.	(16)	CO1	BTL4	Analyzing
14.	Evaluate the impact of clock frequency changes on switching power dissipation with numerical illustration.	(16)	CO1	BTL3	Applying
15.	Discuss the hot electron effect and its influence on long-term device reliability and power efficiency.	(16)	CO1	BTL4	Analyzing
16.	Correlate increased leakage currents with overall power consumption in nanometer CMOS technologies.	(16)	CO1	BTL4	Analyzing
17.	Justify the challenges involved in achieving low power operation in deep submicron CMOS circuits.	(16)	CO1	BTL4	Analyzing

UNIT II – LOW-POWER DESIGN APPROACHES					
Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach – Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.					
PART – A					
Q. No	**Questions**		**CO**	**BTL**	**Competence**
1.	Define voltage scaling in low power VLSI design.		CO2	BTL1	Remembering
2.	Explain how VTCMOS circuits reduce power consumption.		CO2	BTL2	Understanding
3.	List the key features of MTCMOS circuits.		CO2	BTL1	Remembering
4.	Describe the role of threshold voltage control in low power design.		CO2	BTL2	Understanding
5.	Identify the architectural techniques used for low power operation.		CO2	BTL1	Remembering
6.	Discuss how pipelining helps in reducing power dissipation.		CO2	BTL2	Understanding
7.	State the principle of parallel processing for low power systems.		CO2	BTL1	Remembering
8.	Differentiate between pipelining and parallel processing approaches.		CO2	BTL2	Understanding
9.	Outline switched capacitance minimization techniques.		CO2	BTL1	Remembering
10.	Illustrate the importance of system level measures in reducing switched capacitance.		CO2	BTL2	Understanding
11.	Mention circuit level measures used for low power design.		CO2	BTL1	Remembering
12.	Interpret how mask level measures contribute to power reduction.		CO2	BTL2	Understanding
13.	Recall the purpose of sleep transistors in MTCMOS circuits.		CO2	BTL1	Remembering
14.	Clarify the impact of voltage scaling on circuit delay and power.		CO2	BTL2	Understanding
15.	Specify the components contributing to switched capacitance.		CO2	BTL1	Remembering
16.	Analyze how architectural level decisions affect overall power dissipation.		CO2	BTL2	Understanding
17.	Write the expression for dynamic power dissipation.		CO2	BTL1	Remembering
18.	Relate switched capacitance to switching activity factor.		CO2	BTL2	Understanding
19.	Compute the dynamic power consumed by a circuit operating at 1.2 V, 50 MHz, and load capacitance of 10 pF.		CO2	BTL2	Understanding
20.	Estimate the reduction in power when supply voltage is scaled from 1.8 V to 1.2 V (other parameters constant).		CO2	BTL2	Understanding
21.	Calculate the dynamic power if the switching activity factor is reduced by half.		CO2	BTL2	Understanding
22.	Predict the effect on power dissipation when parallel processing allows voltage scaling.		CO2	BTL2	Understanding
23.	Assess the benefit of pipelining in terms of power–performance trade-off.		CO2	BTL2	Understanding
24.	Summarize the advantages of switched capacitance minimization approaches.		CO2	BTL2	Understanding
PART – B					
1.	Apply voltage scaling techniques to reduce power dissipation in CMOS circuits and discuss their limitations.	(16)	CO2	BTL3	Applying
2.	Analyze the operation of VTCMOS circuits with suitable diagrams and explain their impact on leakage power.	(16)	CO2	BTL4	Analyzing

3.	Demonstrate how MTCMOS circuits achieve low standby power using high-Vth transistors.	(16)	CO2	BTL3	Applying
4.	Examine the advantages and drawbacks of MTCMOS techniques in deep-submicron technologies.	(16)	CO2	BTL4	Analyzing
5.	Implement voltage scaling in a low-power digital system and evaluate its effect on delay and power.	(16)	CO2	BTL3	Applying
6.	Compare VTCMOS and MTCMOS approaches in terms of power, performance, and design complexity.	(16)	CO2	BTL4	Analyzing
7.	Analyze the overall effectiveness of multi-level low-power design approaches in modern VLSI systems.	(16)	CO2	BTL3	Applying
8.	Investigate the power-delay trade-off involved in pipelined architectures.	(16)	CO2	BTL4	Analyzing
9.	Employ parallel processing techniques to achieve low-power operation in VLSI systems.	(16)	CO2	BTL3	Applying
10.	Differentiate between pipelining and parallel processing with respect to power optimization.	(16)	CO2	BTL4	Analyzing
11.	Illustrate how switched capacitance minimization can be achieved at the system level.	(16)	CO2	BTL3	Applying
12.	Assess the effectiveness of system-level power reduction measures in low-power VLSI design.	(16)	CO2	BTL4	Analyzing
13.	Design circuit-level techniques for minimizing switched capacitance in CMOS logic.	(16)	CO2	BTL3	Applying
14.	Construct a low-power design strategy combining voltage scaling and switched capacitance minimization.	(16)	CO2	BTL3	Applying
15.	Optimize logic styles to reduce switched capacitance at the circuit level.	(16)	CO2	BTL3	Applying
16.	Evaluate different circuit-level power minimization techniques for low-power applications.	(16)	CO2	BTL4	Analyzing
17.	Apply mask-level measures to reduce parasitic capacitances in CMOS layouts.	(16)	CO2	BTL3	Applying

UNIT III - LOW-VOLTAGE LOW-POWER ADDERS				
Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low Voltage Low Power Design Techniques –Trends of Technology and Power Supply Voltage, Low Voltage Low-Power Logic Styles.				
PART – A				
Q. No	**Questions**	**CO**	**BTL**	**Competence**
1.	Define low-voltage low-power adder design.	CO3	BTL1	Remembering
2.	Explain the need for low-power adders in modern VLSI systems.	CO3	BTL2	Understanding
3.	List the different types of CMOS adder architectures.	CO3	BTL1	Remembering
4.	Describe the operation of a standard full adder cell.	CO3	BTL2	Understanding
5.	Identify the basic components of a ripple carry adder.	CO3	BTL1	Remembering
6.	Discuss the carry propagation mechanism in ripple carry adders.	CO3	BTL2	Understanding
7.	State the principle behind carry look-ahead adders.	CO3	BTL1	Remembering
8.	Differentiate between ripple carry adders and carry look-ahead adders.	CO3	BTL2	Understanding
9.	Outline the structure of a carry select adder.	CO3	BTL1	Remembering

10.	Illustrate how carry select adders reduce delay compared to ripple carry adders.		CO3	BTL2	Understanding
11.	Mention the application of carry save adders in arithmetic circuits.		CO3	BTL1	Remembering
12.	Interpret the role of carry save adders in multi-operand addition.		CO3	BTL2	Understanding
13.	Parallel processing allows an adder to operate at half the original frequency while maintaining throughput. If the original power dissipation is 8 mW, estimate the new power dissipation (ignore leakage).		CO3	BTL2	Understanding
14.	Clarify the relationship between supply voltage scaling and power consumption.		CO3	BTL2	Understanding
15.	Specify the factors influencing power dissipation in CMOS adders.		CO3	BTL1	Remembering
16.	Relate logic style selection to low-voltage low-power operation.		CO3	BTL2	Understanding
17.	Compute the dynamic power of a 1-bit adder operating at 1.2 V, 20 MHz, and load capacitance of 5 pF.		CO3	BTL2	Understanding
18.	Estimate the reduction in power when the supply voltage of an adder is reduced from 1.8 V to 1.2 V.		CO3	BTL2	Understanding
19.	Calculate the power dissipation of an adder if the switching activity factor is reduced by half.		CO3	BTL2	Understanding
20.	Predict the effect of technology scaling on adder power consumption.		CO3	BTL2	Understanding
21.	Assess the suitability of carry look-ahead adders for low-voltage applications.		CO3	BTL1	Remembering
22.	Summarize the advantages of low-voltage low-power logic styles.		CO3	BTL2	Understanding
23.	A 1-bit CMOS full adder drives a load capacitance of 6 pF and operates at a frequency of 25 MHz with a supply voltage of 1.2 V. Assume activity factor $\alpha = 1$. Calculate the dynamic power dissipation.		CO3	BTL2	Understanding
24.	An 8-bit ripple carry adder has a delay of 6.4 ns. If a carry look-ahead adder reduces delay by 50%, estimate its propagation delay.		CO3	BTL2	Understanding
PART-B					
1.	Apply standard adder cell concepts to design a low-power 1-bit full adder.	(16)	CO3	BTL3	Applying
2.	Analyze the power and delay characteristics of standard CMOS adder cells.	(16)	CO3	BTL4	Analyzing
3.	Demonstrate the working of a Ripple Carry Adder using CMOS logic.	(16)	CO3	BTL3	Applying
4.	Examine the limitations of Ripple Carry Adders in low-voltage operation.	(16)	CO3	BTL4	Analyzing
5.	Implement a Carry Look-Ahead Adder and explain how it improves speed.	(16)	CO3	BTL3	Applying
6.	Compare Ripple Carry and Carry Look-Ahead Adders with respect to power and performance.	(16)	CO3	BTL4	Analyzing
7.	Construct a Carry Select Adder for low-power arithmetic applications.	(16)	CO3	BTL3	Applying
8.	Evaluate the area-power trade-offs involved in Carry	(16)	CO3	BTL4	Analyzing

	Select Adder architectures.				
9.	Use Carry Save Adders to improve performance in multi-operand addition.	(16)	CO3	BTL3	Applying
10.	Differentiate Carry Save Adders from Carry Propagation Adders in terms of power dissipation.	(16)	CO3	BTL4	Analyzing
11.	Illustrate the impact of technology scaling on adder power consumption.	(16)	CO3	BTL3	Applying
12.	Assess the effect of reduced supply voltage on adder speed and reliability.	(16)	CO3	BTL4	Analyzing
13.	Design a low-voltage CMOS adder using suitable power-reduction techniques.	(16)	CO3	BTL3	Applying
14.	Investigate the challenges of low-voltage operation in CMOS adders.	(16)	CO3	BTL4	Analyzing
15.	Optimize adder architectures for minimum power under voltage scaling.	(16)	CO3	BTL3	Applying
16.	Inspect the influence of switching activity on adder power dissipation.	(16)	CO3	BTL4	Analyzing
17.	Formulate a design approach combining architectural and circuit-level power reduction for adders.	(16)	CO3	BTL3	Applying

UNIT IV - LOW-VOLTAGE LOW-POWER MULTIPLIERS

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

PART-A

Q. No	Questions	CO	BTL	Competence
1.	Define low-voltage low-power multiplier.	CO4	BTL1	Remembering
2.	Explain the need for low-power multiplier circuits.	CO4	BTL2	Understanding
3.	List the types of multiplier architectures used in VLSI.	CO4	BTL1	Remembering
4.	Describe the operation of a Braun multiplier.	CO4	BTL2	Understanding
5.	Identify the main advantage of the Baugh-Wooley multiplier for signed multiplication.	CO4	BTL1	Remembering
6.	Discuss how the Booth multiplier reduces partial products.	CO4	BTL2	Understanding
7.	State the purpose of Wallace tree multipliers.	CO4	BTL1	Remembering
8.	Differentiate between Braun and Baugh-Wooley multipliers.	CO4	BTL2	Understanding
9.	Outline the steps involved in Booth multiplication.	CO4	BTL1	Remembering
10.	Illustrate how Wallace tree multiplier achieves faster addition of partial products.	CO4	BTL2	Understanding
11.	Mention the key characteristics of low-voltage multiplier design.	CO4	BTL1	Remembering
12.	Interpret the effect of reducing supply voltage on multiplier power consumption.	CO4	BTL2	Understanding
13.	Recall the method for generating partial products in a Braun multiplier.	CO4	BTL1	Remembering
14.	Clarify the mechanism used in Baugh-Wooley multipliers to handle sign bits.	CO4	BTL2	Understanding

15.	Specify the advantage of Booth encoding in reducing switching activity.		CO4	BTL1	Remembering
16.	Analyze the difference in delay between ripple-based multipliers and Wallace tree multipliers.		CO4	BTL2	Understanding
17.	Write the expression for dynamic power dissipation in a multiplier circuit.		CO4	BTL1	Remembering
18.	Relate multiplier architecture choice to low-power performance.		CO4	BTL2	Understanding
19.	Compute the dynamic power of an 8×8 CMOS multiplier operating at 1.2 V, 20 MHz, and load capacitance of 15 pF.		CO4	BTL2	Understanding
20.	Estimate the reduction in power when supply voltage is scaled from 1.8 V to 1.2 V.		CO4	BTL2	Understanding
21.	Calculate the number of partial products in an 8×8 Braun multiplier.		CO4	BTL2	Understanding
22.	Predict the effect of using Booth encoding on the number of partial products for an 8×8 multiplier.		CO4	BTL2	Understanding
23.	Assess the suitability of Wallace tree multipliers for high-speed low-power applications.		CO4	BTL2	Understanding
24.	For an 8×8 multiplier, determine the number of partial products after Booth encoding.		CO4	BTL2	Understanding
	PART-B				
1.	Apply the basic principles of binary multiplication to explain the operation of digital multipliers.	(16)	CO4	BTL3	Applying
2.	Analyze the sources of power consumption in CMOS multiplier circuits.	(16)	CO4	BTL4	Analyzing
3.	Design a Braun multiplier and explain its suitability for low-power applications.	(16)	CO4	BTL3	Applying
4.	Examine the limitations of Braun multipliers in low-voltage operation.	(16)	CO4	BTL4	Analyzing
5.	Implement a Baugh Wooley multiplier for signed multiplication using CMOS logic.	(16)	CO4	BTL3	Applying
6.	Compare Braun and Baugh Wooley multipliers in terms of power, area, and speed.	(16)	CO4	BTL4	Analyzing
7.	Construct a Booth multiplier and explain how it reduces the number of partial products.	(16)	CO4	BTL3	Applying
8.	Evaluate the impact of Booth encoding on power dissipation and performance.	(16)	CO4	BTL4	Analyzing
9.	Demonstrate the working principle of different multiplier architectures with suitable block diagrams.	(16)	CO4	BTL3	Applying
10.	Differentiate between array multipliers and tree-based multipliers with respect to low-power design.	(16)	CO4	BTL4	Analyzing
11.	Develop a low-voltage multiplier design using architectural power reduction techniques.	(16)	CO4	BTL3	Applying
12.	Assess the effect of voltage scaling on multiplier speed and reliability.	(16)	CO4	BTL4	Analyzing
13.	Illustrate the structure and operation of a Wallace Tree multiplier.	(16)	CO4	BTL3	Applying
14.	Investigate the advantages of Wallace Tree multipliers for	(16)	CO4	BTL4	Analyzing

	high-speed low-power applications.				
15.	Employ low-power logic styles in the implementation of multiplier circuits.	(16)	CO4	BTL3	Applying
16.	Inspect the role of partial product reduction in minimizing power consumption.	(16)	CO4	BTL4	Analyzing
17.	Formulate a design strategy for a low-power multiplier combining circuit- and architectural-level techniques.	(16)	CO4	BTL3	Applying

UNIT V - LOW-VOLTAGE LOW-POWER MEMORIES

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

PART-A

Q. No	Questions	CO	BT Level	Competence
1.	A ROM has 2048 words. Find the number of address lines required.	CO5	BTL 1	Remembering
2.	Define Read Only Memory (ROM).	CO5	BTL 1	Remembering
3.	Explain the importance of low-power ROM technology.	CO5	BTL 2	Understanding
4.	List the different types of ROM.	CO5	BTL 1	Remembering
5.	Illustrate the basic operation of a ROM.	CO5	BTL 2	Understanding
6.	Bit-line capacitance is 0.2 pF and voltage is 1 V. Find stored charge.	CO5	BTL 1	Remembering
7.	Interpret the need for low-voltage operation in memory circuits.	CO5	BTL 2	Understanding
8.	Identify the main features of Static Random Access Memory (SRAM).	CO5	BTL 1	Remembering
9.	Describe the working of an SRAM memory cell.	CO5	BTL 2	Understanding
10.	Name the components of a 6T SRAM cell.	CO5	BTL 1	Remembering
11.	A DRAM requires refresh every 64 ms for 4096 rows. Find refresh time per row.	CO5	BTL 1	Remembering
12.	State any two applications of ROM.	CO5	BTL 2	Understanding
13.	Analyze one low-power technique used in SRAM design.	CO5	BTL 1	Remembering
14.	Define Dynamic Random Access Memory (DRAM).	CO5	BTL 2	Understanding
15.	Explain why DRAM cells require refreshing.	CO5	BTL 1	Remembering
16.	Mention any two advantages of DRAM.	CO5	BTL 2	Understanding
17.	Summarize the working principle of a DRAM cell.	CO5	BTL 1	Remembering
18.	Differentiate between normal refresh and self-refresh in DRAM.	CO5	BTL 2	Understanding
19.	A DRAM cell loses 0.1 pC/ms. If initial charge is 2 pC, find time for 50% loss.	CO5	BTL 2	Understanding
20.	Define bit-line leakage current in low-power SRAMs.	CO5	BTL 1	Remembering
21.	List the factors influencing standby power in SRAM cells.	CO5	BTL 1	Remembering
22.	Interpret the impact of self-refresh modes on DRAM power consumption.	CO5	BTL 2	Understanding

23.	An SRAM spends 80% time in standby (5 mW) and 20% active (50 mW). Find average power.		CO5	BTL 2	Understanding
24.	Explain how equalization of bit lines improves sensing reliability in SRAM memories.		CO5	BTL 2	Understanding
PART-B					
1.	Apply the basic principles of ROM operation to explain its use in low-power systems.	(16)	CO5	BTL3	Applying
2.	Analyze the power dissipation mechanisms in conventional ROM circuits.	(16)	CO5	BTL4	Analyzing
3.	Design a low-power ROM architecture suitable for embedded applications.	(16)	CO5	BTL3	Applying
4.	Examine the limitations of ROM technology under aggressive voltage scaling.	(16)	CO5	BTL3	Applying
5.	Illustrate the structure and operation of a 6T SRAM memory cell.	(16)	CO5	BTL4	Analyzing
6.	Assess the impact of leakage currents on SRAM power consumption.	(16)	CO5	BTL4	Analyzing
7.	Demonstrate the working of precharge and equalization circuits in SRAM arrays.	(16)	CO5	BTL4	Analyzing
8.	Investigate how precharge and equalization affect read stability and power in SRAM.	(16)	CO5	BTL3	Applying
9.	Implement low-power SRAM techniques to reduce dynamic and static power.	(16)	CO5	BTL4	Analyzing
10.	Differentiate between conventional SRAM and low-power SRAM technologies.	(16)	CO5	BTL4	Analyzing
11.	Construct the basic DRAM cell and explain its read and write operations.	(16)	CO5	BTL3	Applying
12.	Inspect the causes of data loss in DRAM cells and their relation to power consumption.	(16)	CO5	BTL3	Applying
13.	Explain the operation of a self-refresh circuit used in low-power DRAMs.	(16)	CO5	BTL3	Applying
14.	Evaluate the effectiveness of self-refresh mechanisms in reducing standby power.	(16)	CO5	BTL3	Applying
15.	Employ voltage scaling techniques in memory design to achieve low-power operation.	(16)	CO5	BTL3	Applying
16.	Break down the challenges of low-voltage operation in SRAM and DRAM memories.	(16)	CO5	BTL3	Applying
17.	Formulate a memory design strategy combining circuit- and architectural-level power reduction methods.	(16)	CO5	BTL4	Analyzing